HIGH-SPEED
1K x 9 DUAL-PORT
STATIC RAM WITH BUSY

Integrated Device Technology, Inc.

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT7010/70104S
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - IDT7010/70104L
    Active: 400mW (typ.)
    Standby: 2mW (typ.)
- Fully asynchronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit.
- MASTER IDT7010 easily expands data bus width to 18 bits or more using SLAVE IDT70104 chip.
- On-chip port arbitration logic (IDT7010 only)
- $\overline{BUSY}$ output flag on MASTER; $\overline{BUSY}$ input on SLAVE
- Battery backup operation — 2V data retention
- TTL compatible, signal 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7010/IDT70104 are high-speed 1K X 9 dual-port static RAMs. The IDT7010 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70104 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

The devices utilize a 9-bit wide data path to allow for control/data and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200μW from a 2V battery.

The IDT7010/IDT70104 devices are packaged in 48-pin sidebrazed or plastic DIPs, 48-pin LCCs and 48-pin flatpacks. The military devices are processed 100% in compliance to test methods of MIL-STD-883, Method 5004.
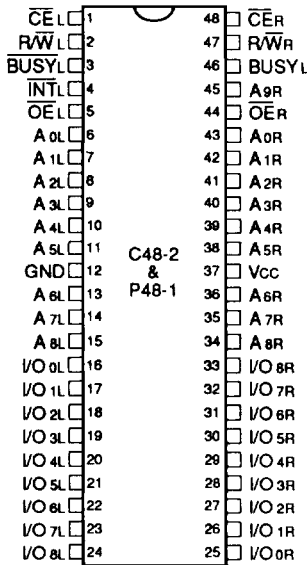
FUNCTIONAL BLOCK DIAGRAM
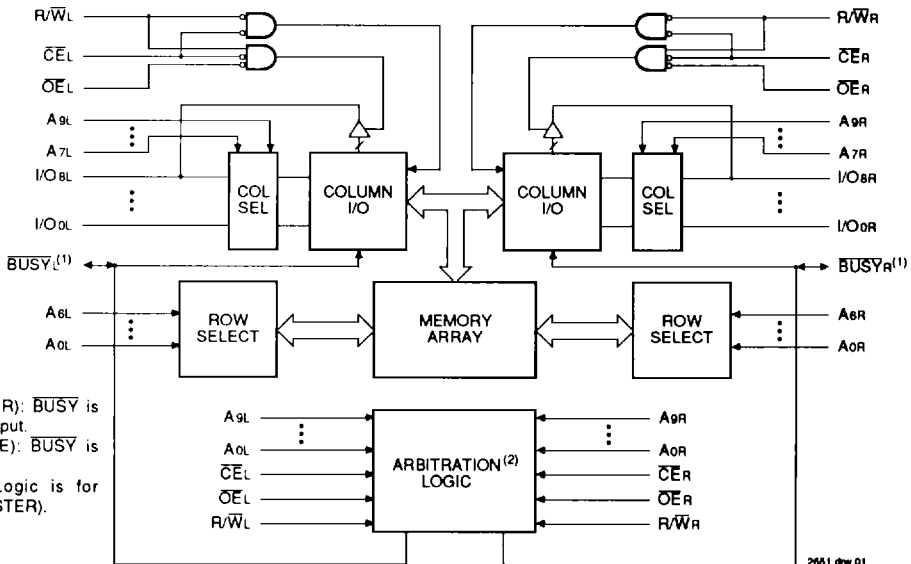
NOTE:
1. 7010 (MASTER): $\overline{BUSY}$ is totem-pole output.
   70104 (SLAVE): $\overline{BUSY}$ is input.
2. Arbitration Logic is for IDT7010 (MASTER).

2651 drw 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES
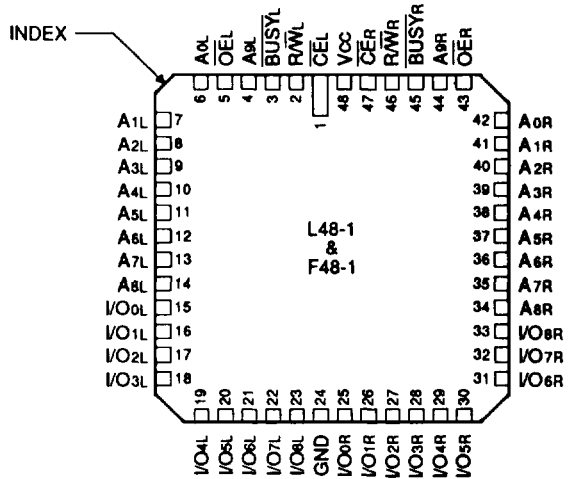
SEPTEMBER 1990

PIN CONFIGURATIONS

48-PIN DIP
TOP VIEW

2651 drw 02

48-PIN LCC/FLATPACK
TOP VIEW

2651 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2651 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

2651 tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2651 tbl 03

7

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7010S 70104S Min.	7010S 70104S Max.	7010L 70104L Min.	7010L 70104L Max.	Unit
|ILI|	Input Leakage Current	Vcc = 5.5V, VIN = 0V to Vcc	—	10	—	5	µA
|ILO|	Output Leakage Current	CE = VIH, VOUT = 0V to Vcc	—	10	—	5	µA
VOL	Output Low Voltage (I/Oo – I/O8), BUSY	IOL = 4mA	—	0.4	—	0.4	V
VOH	Output High Voltage (I/Oo – I/O8), BUSY	IOH = –4mA	2.4	—	2.4	—	V

2651 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7010 x 25[2] 70104 x 25[2] Typ.	Max.	7010 x 35 70104 x 35 Typ.	Max.	7010 x 45 70104 x 45 Typ.	Max.	7010 x 55 70104 x 55 Typ.	Max.	7010 x 70[3] 70104 x 70[3] Typ.	Max.	Unit
Icc	Dynamic Operating Current (Both Ports Active)	CE ≤ VIL Outputs Open f = fMAX[4]	Mil.	S	—	—	80	300	75	290	70	285	65	275	mA
				L	—	—	80	220	75	210	70	205	65	200	
			Com'l.	S	75	260	75	250	75	245	70	235	—	—	
				L	75	190	75	180	75	170	70	160	—	—	
ISB1	Standby Current (Both Ports — TTL Level Inputs)	CEL and CER ≥ VIH f = fMAX[4]	Mil.	S	—	—	25	80	25	80	25	80	25	65	mA
				L	—	—	25	60	25	60	25	60	25	55	
			Com'l.	S	25	65	25	65	25	65	25	65	—	—	
				L	25	45	25	45	25	45	25	45	—	—	
ISB2	Standby Current (Both Ports — TTL Level Inputs)	CEL or CER ≥ VIH Active Port Outputs Open, f = fMAX[4]	Mil.	S	—	—	50	190	45	170	40	170	40	165	mA
				L	—	—	50	145	45	140	40	140	40	135	
			Com'l.	S	50	175	46	160	45	150	40	140	—	—	
				L	50	125	46	115	45	105	40	95	—	—	
ISB3	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports CEL and CER ≥ Vcc – 0.2V VIN ≥ Vcc – 0.2V or VIN ≤ 0.2V, f = 0[5]	Mil.	S	—	—	1.2	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.4	10	0.2	10	0.2	10	0.2	10	
			Com'l.	S	1.2	15	1.0	15	1.0	15	1.0	15	—	—	
				L	0.4	5	0.4	5.0	0.2	5.0	0.2	5.0	—	—	
ISB4	Full Standby Current (One Port — All CMOS Level Inputs)	One Port CEL or CER ≥ Vcc – 0.2V, VIN ≥ Vcc – 0.2V or VIN ≤ 0.2V Active Port Outputs Open, f = fMAX[4]	Mil.	S	—	—	47	170	45	160	40	155	40	150	mA
				L	—	—	44	130	42	125	35	120	35	115	
			Com'l.	S	50	155	45	142	45	132	45	127	—	—	
				L	46	120	42	110	42	100	42	95	—	—	

NOTES: 2651 tbl 05
1. "x" in part numbers indicates power rating (S or L).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. At f = fMAX, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/tRC, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition		7010L/70104L			Unit
				Min.	Typ.[1]	Max.	
V_{DR}	Vcc for Data Retention	Vcc = 2.0V, $\overline{CE}$ ≥ Vcc – 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	μA
			Com'l.	—	100	1500	μA
t_{CDR}[3]	Chip Deselect to Data Retention Time	V_{IN} ≥ Vcc – 0.2V or V_{IN} ≤ 0.2V		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2651 tbl 06

NOTES:
1. Vcc = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM
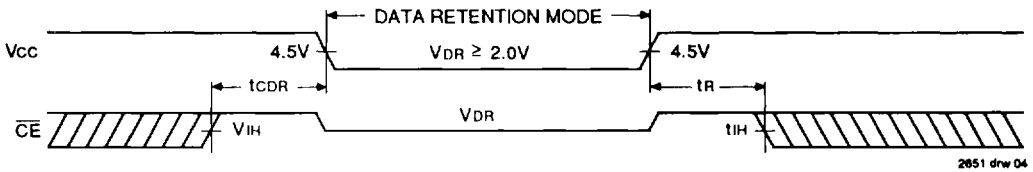
2651 drw 04

AC TEST CONDITIONS

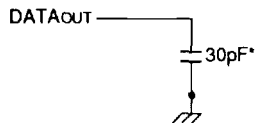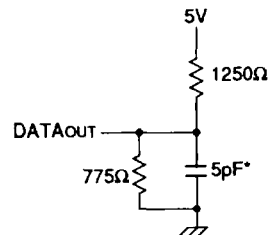|	
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2651 tbl 07

Figure 1. Output Load

2651 drw 05

2651 drw 06
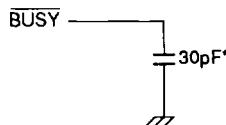
Figure 2. Output Load (for tHZ, tLZ, tWZ, and tOW)

2651 drw 07

Figure 3. BUSY Output Load

*Including scope and jig.

7

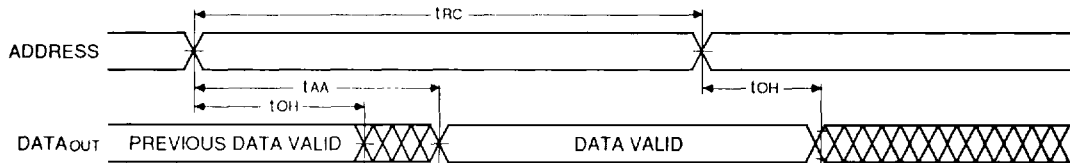## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7010 x 25[2] 70104 x 25[2] Min.	Max.	7010 x 35 70104 x 35 Min.	Max.	7010 x 45 70104 x 45 Min.	Max.	7010 x 55 70104 x 55 Min.	Max.	7010 x 70[3] 70104 x 70[3] Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 4]	0	—	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time[1, 4]	—	10	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

NOTES: 2651 tbl 08
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only
3. −55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
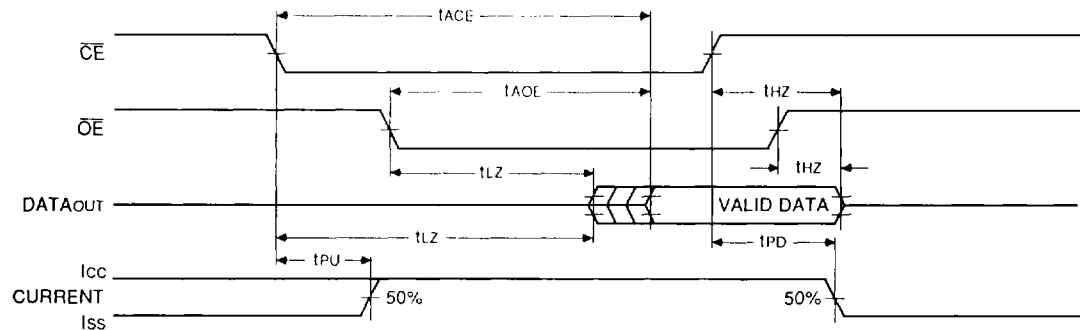5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]

2651 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]

2651 drw 10

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low
4. $\overline{OE}$ = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	7010 x 25[2] 70104 x 25[2]		7010 x 35 70104 x 35		7010 x 45 70104 x 45		7010 x 55 70104 x 55		7010 x 70[3] 70104 x 70[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time[5]	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	20	—	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	12	—	20	—	20	—	20	—	30	—	ns
tHZ	Output High Z Time[1, 4]	—	10	—	15	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1, 4]	—	10	—	15	—	20	—	30	—	35	ns
tOW	Output Active From End of Write[1, 4]	0	—	0	—	0	—	0	—	0	—	ns

2651 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part numbers indicates power rating (S or L).
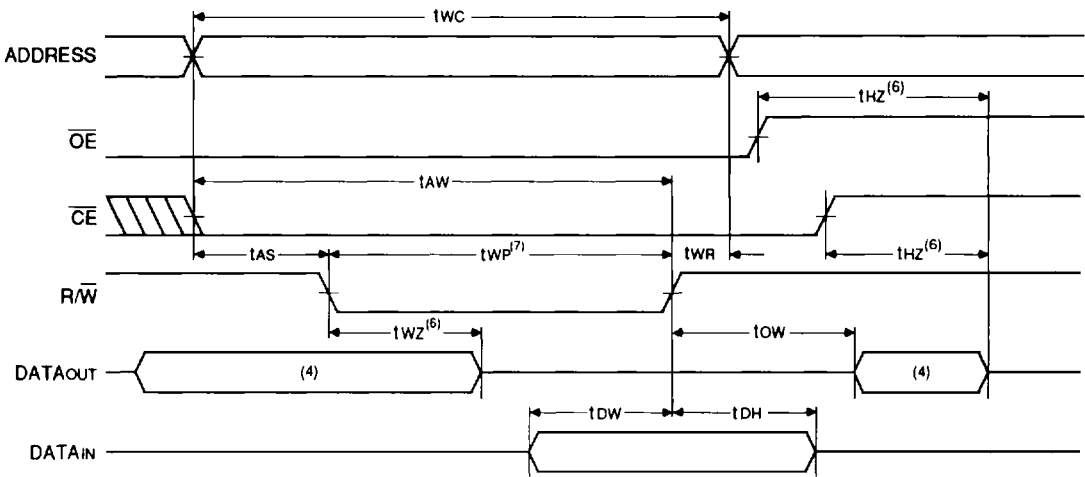
CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

2651 tbl 10

NOTE:
1. This parameter is determined by device characterization but is not production tested.
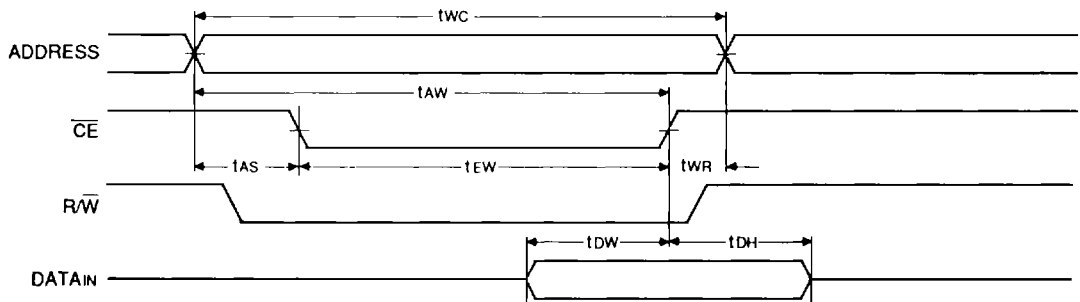
7

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)[1, 2, 3, 7]

2651 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)[1, 2, 3, 5]

2651 drw 12

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or t_{WZ} + t_{DW} to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during as R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	70101 x 25[1] 70105 x 25[1]		70101 x 35 70105 x 35		70101 x 45 70105 x 45		70101 x 55 70105 x 55		70101 x 70[2] 70105 x 70[2]		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Busy Timing (For Master IDT7010 Only)												
tBAA	BUSY Access Time to Address	—	25	—	35	—	35	—	45	—	45	ns
tBDA	BUSY Disable Time to Address	—	20	—	30	—	35	—	40	—	40	ns
tBAC	BUSY Access Time to Chip Enable	—	20	—	30	—	30	—	35	—	35	ns
tBDC	BUSY Disable Time to Chip Enable	—	20	—	25	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay[3]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	45	—	55	—	65	—	80	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT70104 Only)												
tWB	Write to BUSY Input[6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY[7]	15	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Date Delay[9]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	45	—	55	—	65	—	80	ns

NOTES:

2651 tbl 11

1. 0°C to +70°C temperature range only
2. –55°C to +125°C temperature range only
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With BUSY (For MASTER IDT7010 only)".
4. To ensure that the earlier of the two ports wins
5. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual)
6. To ensure that a write cycle is inhibited during contention
7. To ensure that a write cycle is completed after contention
8. "x" in part numbers indicates power rating (S or L)
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With BUSY Port-to-port Delay (For SLAVE IDT70104 only)"

7

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ [1, 2, 3]
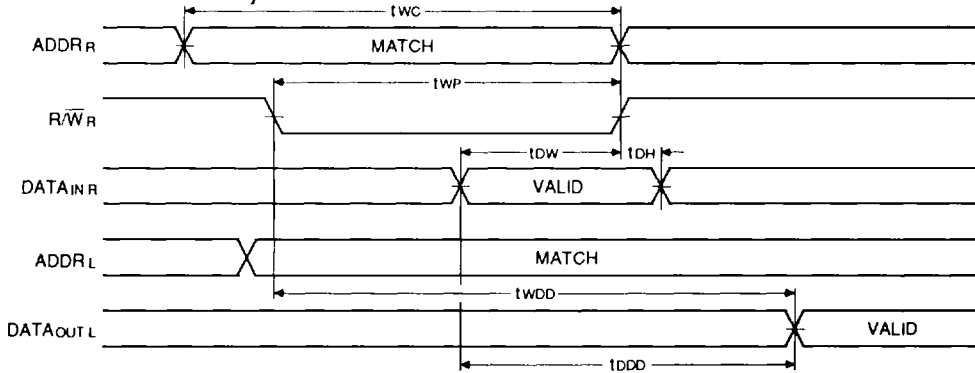## (FOR MASTER IDT7010 ONLY)
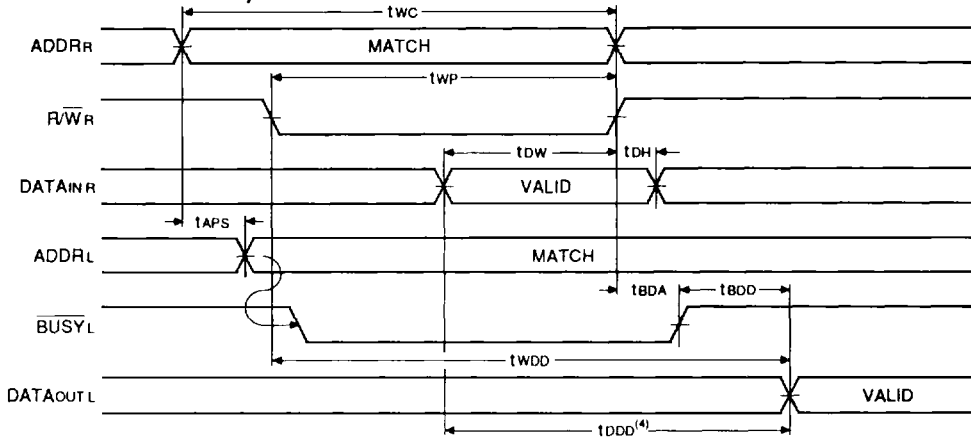
2651 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to, in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LOW for the reading port.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY [1, 2, 3]
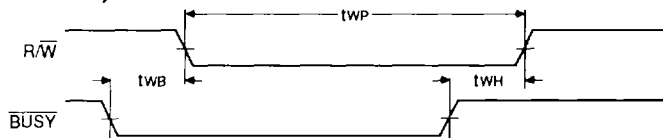## (FOR SLAVE IDT70104 ONLY)

2651 drw 14

NOTES:
1. Assume $\overline{BUSY}$ input at HIGH for the writing port, and $\overline{OE}$ at LOW for the reading port.
2. Write Cycle parameters should be adhered to, in order to ensure proper writing.
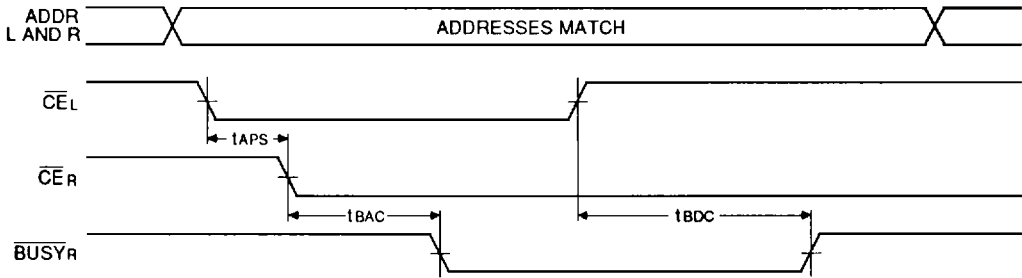3. Device is continuously enabled for both ports.

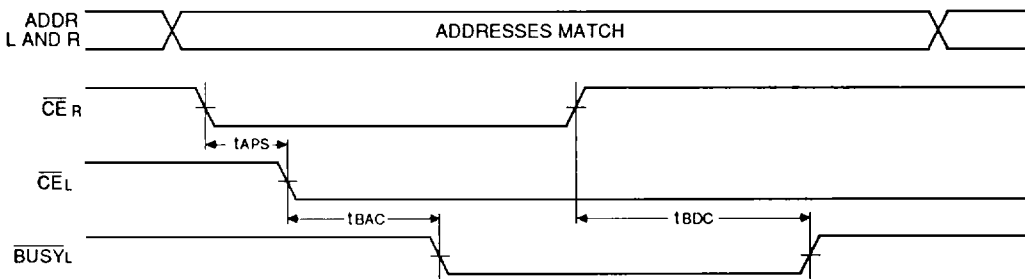## TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT
(FOR SLAVE IDT70104 ONLY)

2651 drw 15

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION
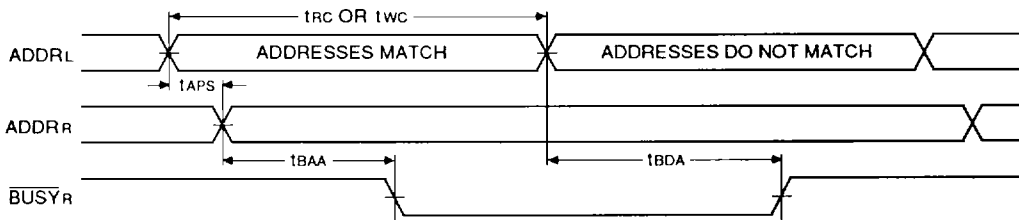
$\overline{CE}$L Valid First:

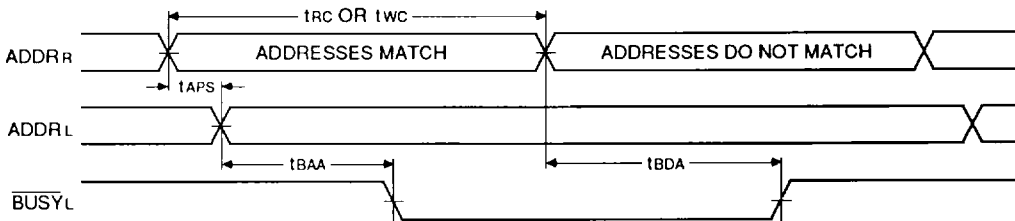$\overline{CE}$R Valid First:

2651 drw 16

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION[1]

Left Address Valid First:

2651 drw 17

Right Address Valid First:

2651 drw 18

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

FUNCTIONAL DESCRIPTION

The IDT7010/70104 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7010/70104 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

## DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to eighteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inherited due to $\overline{BUSY}$ from the MASTER.

18-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS
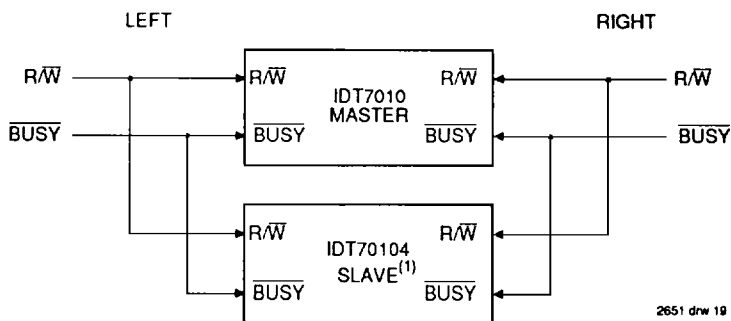
NOTE:
1. No arbitration in IDT70104 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT70104 (SLAVE).

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/W̅	C̅E̅	O̅E̅	D0–8	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	C̅E̅R = C̅E̅L = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATA$_{IN}$	Data on Port Written Into Memory[2]
H	L	L	DATA$_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

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NOTES:
1. $A_{0L} – A_{9L} \neq A_{0R} – A_{9R}$
2. If B̅U̅S̅Y̅ = L, data is not written.
3. If B̅U̅S̅Y̅ = L, data may not be valid, see twDD and tDDD timing.
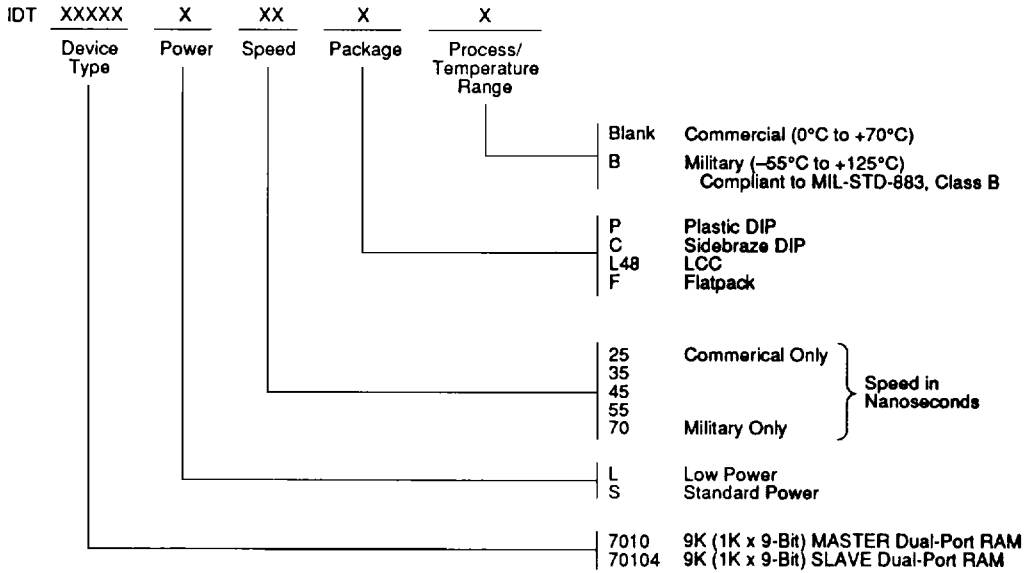4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II. ARBITRATION[1]

Left Port		Right Port		Flags		
C̅E̅L	$A_{0L} – A_{9L}$	C̅E̅R	$A_{0R} – A_{9R}$	B̅U̅S̅Y̅L	B̅U̅S̅Y̅R	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} – A_{9R}$	L	$\neq A_{0L} – A_{9L}$	H	H	No Contention
Address Arbitration With C̅E̅ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
C̅E̅ Arbitration With Address Match Before C̅E̅						
LL5R	= $A_{0R} – A_{9R}$	LL5R	= $A_{0L} – A_{9L}$	H	L	L-Port Wins
RL5L	= $A_{0R} – A_{9R}$	RL5L	= $A_{0L} – A_{9L}$	L	H	R-Port Wins
LW5R	= $A_{0R} – A_{9R}$	LW5R	= $A_{0L} – A_{9L}$	H	L	Arbitration Resolved
LW5R	= $A_{0R} – A_{9R}$	LW5R	= $A_{0L} – A_{9L}$	L	H	Arbitration Resolved

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NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
  LV5R = Left Address Valid ≥ 5ns before right address.
  RV5L = Right Address Valid ≥ 5ns before left address.

  Same = Left and Right Addresses match within 5ns of each other.
  LL5R = Left C̅E̅ = LOW > 5ns before Right C̅E̅.
  RL5L = Right C̅E̅ = LOW ≥ 5ns before Left C̅E̅.
  LW5R = Left and right C̅E̅ = LOW within 5ns of each other.

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ORDERING INFORMATION

```
IDT   XXXXX     X      XX      X          X
      Device   Power  Speed  Package  Process/
       Type                          Temperature
                                        Range
```

Blank	Commercial (0°C to +70°C)
B	Military (−55°C to +125°C) Compliant to MIL-STD-883, Class B
P	Plastic DIP
C	Sidebraze DIP
L48	LCC
F	Flatpack
25	Commerical Only
35	
45	Speed in Nanoseconds
55	
70	Military Only
L	Low Power
S	Standard Power
7010	9K (1K x 9-Bit) MASTER Dual-Port RAM
70104	9K (1K x 9-Bit) SLAVE Dual-Port RAM

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