S72WS-S based MCP Products

1.8 Volt-only x16 Flash Memory and SDRAM on Split Bus

Simultaneous Read/Write, Burst Mode MirrorBit® Eclipse™ NOR Flash on Bus 1 Mobile SDRAM on Bus 2

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S72WS-S_00 **Revision** 02 **Issue Date** August 12, 2008

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Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

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The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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Questions regarding these document designations may be directed to your local sales office.

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 1.7 to 1.95 V**
- **Flash access time: 100 ns for NOR Flash**
- **Flash burst frequency: 104 MHz, 133 MHz**
- **Mobile SDRAM burst frequency: 133 MHz (SDR), 166 MHz (DDR)**
- **Package:**
  - 13.0 x 11.0 mm MCP
- **Operating Temperature**
  - –25°C to +85°C (wireless)

The S72WS series is a product line of stacked packages and consists of:

- **One or two MirrorBit® Eclipse™ NOR flash memory die**
- **Separate bus for one or more Mobile SDRAM die**

The products covered by this document are listed in the table below.

Device	Eclipse Flash Density	NAND Flash Density
S72WS01GSF0YHMJ5	1 Gb	512 Mb (DDR)
S72WS01GSF0YHMJ3	1 Gb	512 Mb (DDR)
S72WS01GSF0YHM15	1 Gb	512 Mb (SDR)

Note:
For a full list of OPNs, please contact the local sales representative or refer to the Ordering Information valid combinations tables.

For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29WS-S	S29NS-S_00
512 Mb Mobile DDR-DRAM Type 5	DRAM_11
512 Mb Mobile SDR-DRAM Type 5	DRAM_12

Publication Number S72WS-S_00 **Revision** 02 **Issue Date** August 12, 2008

1. Product Selector Guide

1.1 NOR Flash + DRAM Products

Device	NOR Flash Density	NOR Flash Speed	DRAM Density	DRAM Speed	DRAM Supplier	Package
S72WS01GSF0YHMJ5	1 Gb	104 MHz	512 Mb	166 MHz (DDR)	Type 5	MCP 13 x 11 mm
S72WS01GSF0YHM15				133 MHz (SDR)		
S72WS01GSF0YHMJ3		133 MHz		166 MHz (DDR)		

2. MCP Block Diagrams

2.1 NOR Flash + DRAM Products

Figure 2.1 S72WS01GSF0YHMH5

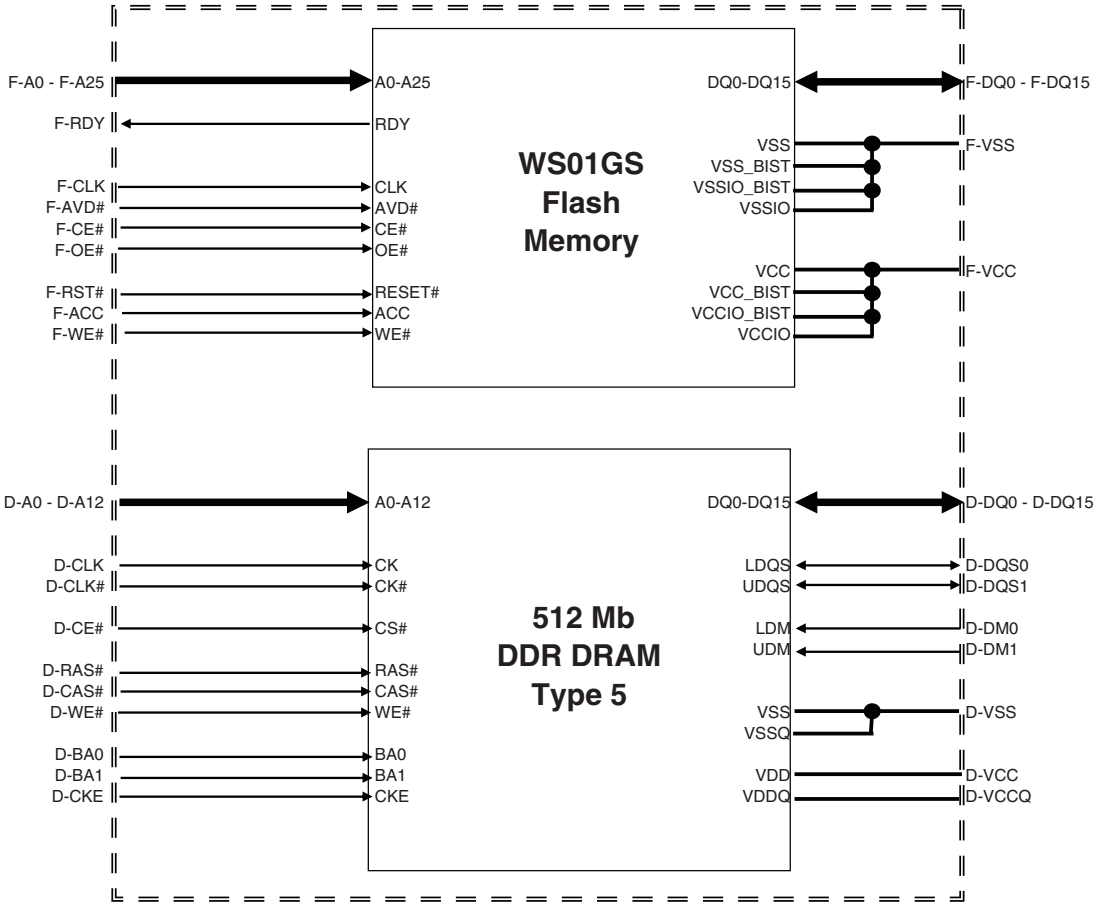
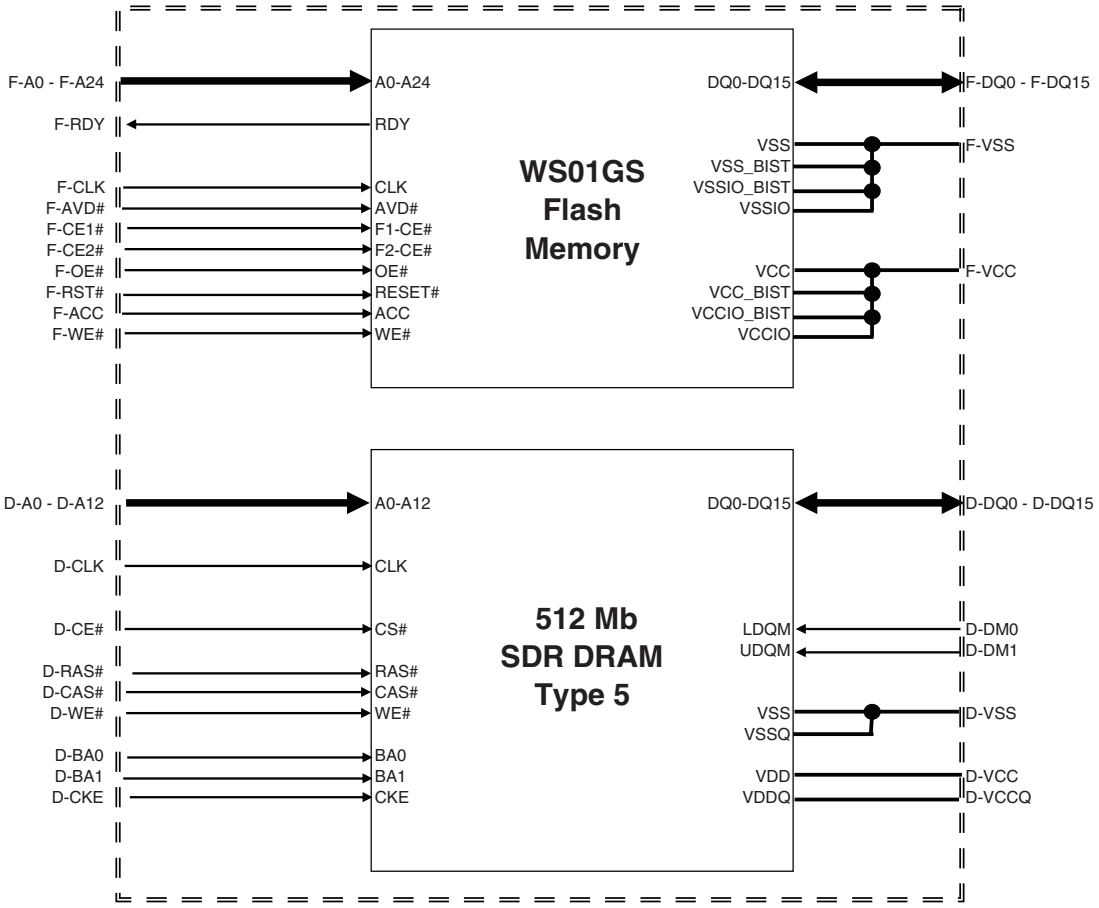


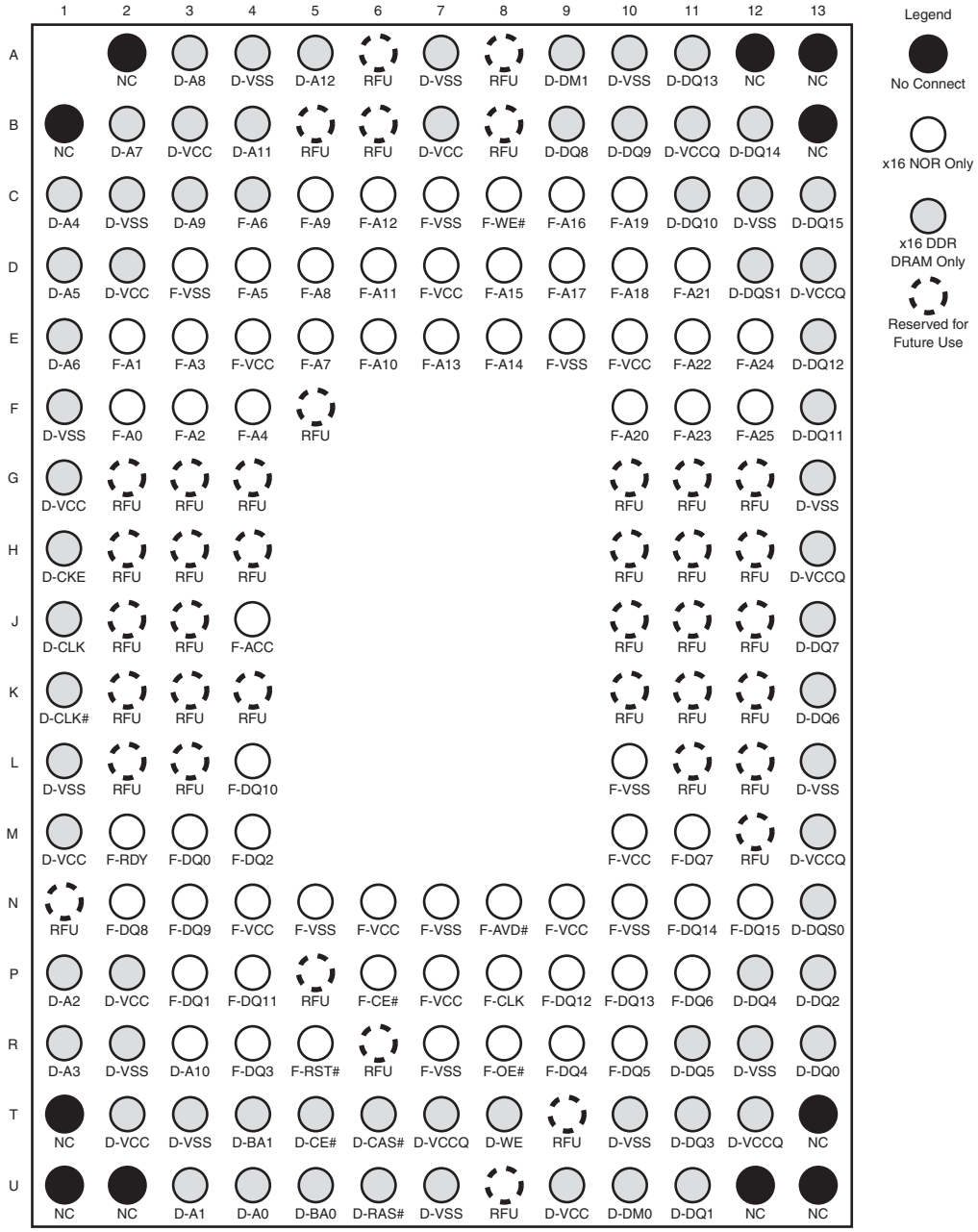
Figure 2.2 S72WS01GSF0YHM15



3. Connection Diagrams

3.1 S72WS01GSF0YHMJ3, S72WS01GSF0YHMJ5

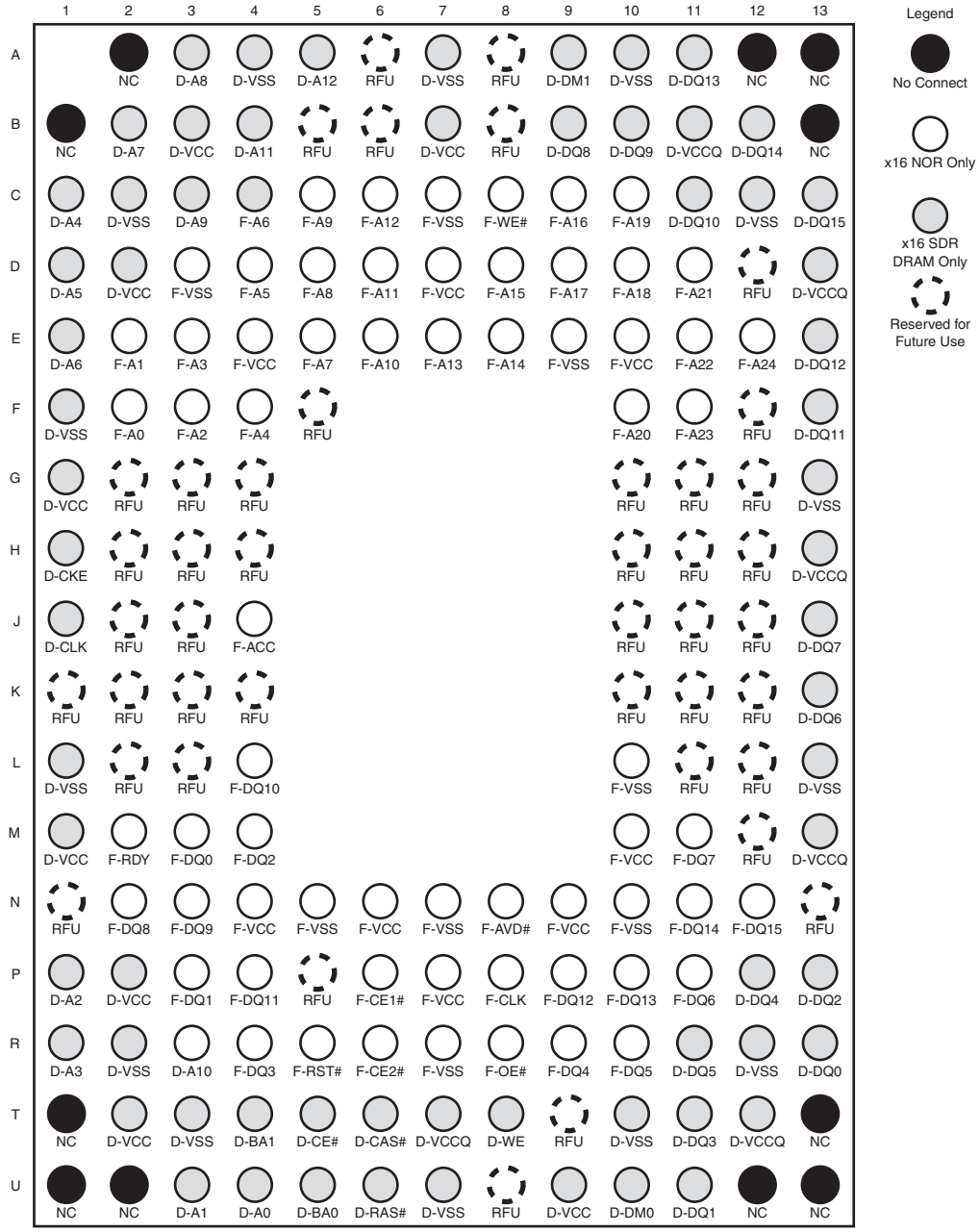
186-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Note:
DDR-only signals are RFUs in the case of the SDR DRAM-based solutions.

3.2 S72WS01GSF0YHM15

186-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



3.2.0.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

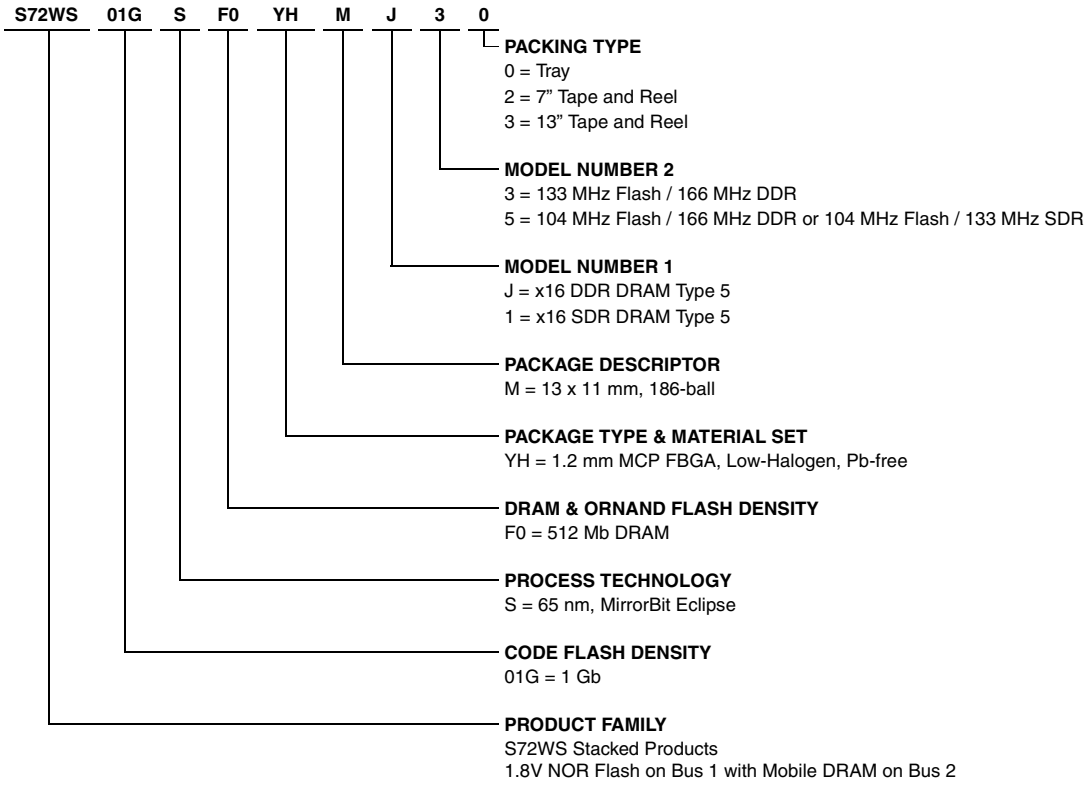
Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150×C for prolonged periods of time.

3.3 NOR Flash and DRAM Input/Output Descriptions

Signal	Description	Flash	DRAM
F-Amax-F-A0	NOR Flash Address inputs	X	
F-DQ15-F-DQ0	Flash Data input/output	X	
F-CE2#	NOR Flash Chip-enable input #2. Asynchronous relative to CLK for Burst Mode	X	
F-CE#	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.	X	
F-OE#	NOR Flash Output Enable input. Asynchronous relative to CLK for Burst mode.	X	
F-WE#	NOR Flash Write Enable input.	X	
F-V_{CC}	NOR Flash device power supply (1.7 V - 1.95V).	X	
F-V_{SS}	NOR Flash Ground	X	
RFU	Reserved for Future Use		
F-RDY	Flash ready output. Indicates the status of the Burst read. V_{OL} = data valid.	X	
F-CLK	NOR Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.	X	
F-AVD#	NOR Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs	X	
F-RST#	NOR Flash hardware reset input. V_{IL}= device resets and returns to reading array data	X	
F-ACC	NOR Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X	
D-Amax-D-A0	SDRAM Address inputs		X
D-DQ15-D-DQ0	SDRAM Data input/output		X
D-CLK	SDRAM System Clock		X
D-CE#	SDRAM Chip Select		X
D-CKE	SDRAM Clock Enable		X
D-BA1-BA0	SDRAM Bank Select		X
D-RAS#	SDRAM Row Address Strobe		X
D-CAS#	SDRAM Column Address Strobe		X
D-DM1-D-DM0	SDRAM Data Input/Output Mask		X
D-WE#	SDRAM Write Enable input		X
D-V_{SS}	SDRAM Ground		X
D-CLK#	DDR SDRAM Clock - in addition to D-CLK, this signal is available for DDRAMs that need CLK# for normal operations		X
D-V_{CCQ}	SDRAM Input/Output Buffer power supply		X
D-V_{CC}	SDRAM device power supply		X
D-DQS0 - D-DQS1	DDR SDRAM Data Strobe pins. DQS provides the read data strobes (as output) and the write data strobes (as input). Each DQS pin corresponds to eight DQ pins, respectively.		X

4. Ordering Information

The order number is formed by a valid combinations of the following:



4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

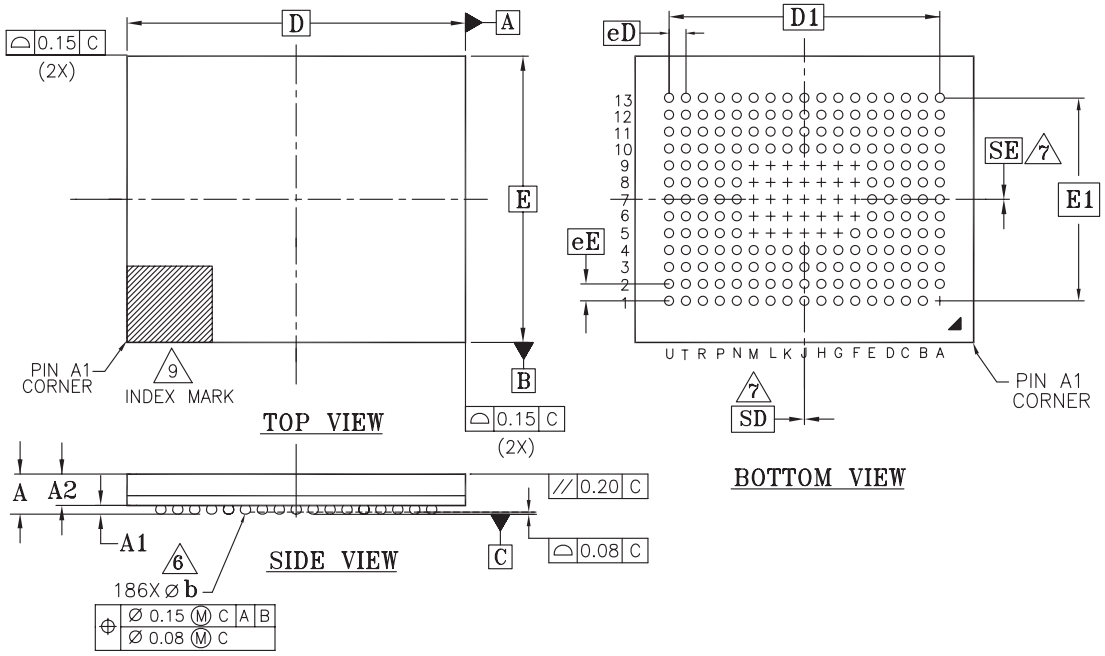
Base Ordering Number	NOR Flash Speed	DRAM Supplier	DRAM Speed	Package Type	Package Markings
S72WS01GSF0YHMJ5	104 MHz	Type 5	166 MHz (DDR)	13 x 11 mm (MCP)	(Note 2)
S72WS01GSF0YHM15			133 MHz (SDR)		
S72WS01GSF0YHMJ3	133 MHz		166 MHz (DDR)		

Notes

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading* S *and packing type designator from ordering part number.*

5. Physical Dimensions

5.1 ASG186—186-ball Fine-Pitch Ball Grid Array (FBGA) 11 x 13 mm Package



PACKAGE	ASG 186			
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.79	---	0.95	BODY THICKNESS
D		13.00 BSC		BODY SIZE
E		11.00 BSC		BODY SIZE
D1		10.40 BSC		MATRIX FOOTPRINT
E1		7.80 BSC		MATRIX FOOTPRINT
MD		17		MATRIX SIZE D DIRECTION
ME		13		MATRIX SIZE E DIRECTION
n		186		BALL COUNT
Ø b	0.325	0.375	0.425	BALL DIAMETER
eE		0.65 BSC		BALL PITCH
eD		0.65 BSC		BALL PITCH
SD SE		0.00 BSC		SOLDER BALL PLACEMENT
	A1,F6,F7,F8,F9,G5,G6,G7,G8,G9 H5,H6,H7,H8,H9,J5,J6,J7,J8,J9, K5,K6,K7,K8,K9,L5,L6,L7,L8,L9, M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3700 \ 16-038.24 \ 6.24.8

6. Revision History

Section	Description
Revision 01 (July 1, 2008)	
	Initial release
Revision 02 (August 12, 2008)	
Global	Added OPN S72WS01GSF0YHMJ3
Features	Changed Flash access time to 100 ns

Colophon

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