N-channel enhancement mode vertical D-MOS transistor

BSP107

FEATURES

- Direct interface to C-MOS, TTL, etc due to low threshold voltage
- High-speed switching
- No secondary breakdown.

DESCRIPTION

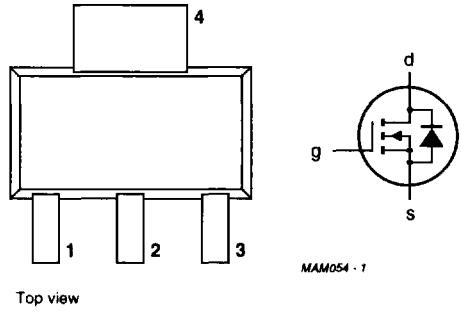
N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer driver switching.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	200	V
V_{GSth}	gate-source threshold voltage	2.4	V
I_D	drain current (DC)	200	mA
R_{DSon}	drain-source on-state resistance	28	Ω



Top view

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP107

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	200	mA
I_{DM}	drain current	peak	-	350	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Notes

1. Device mounted on an epoxy printed circuit board, 40 mm x 40 mm x 1.5 mm. Mounting pad for the drain lead minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP107

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	-	-	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	-	-	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	-	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	-	14	-	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	-	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 - 10 V	-	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 - 10 V	-	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSP107

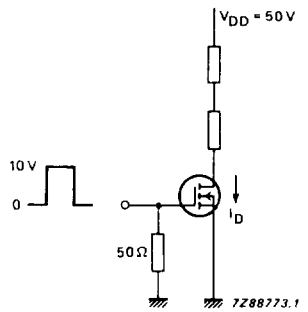


Fig.2 Switching time test circuit.

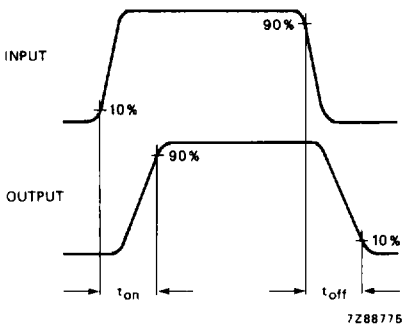


Fig.3 Input and output waveforms.

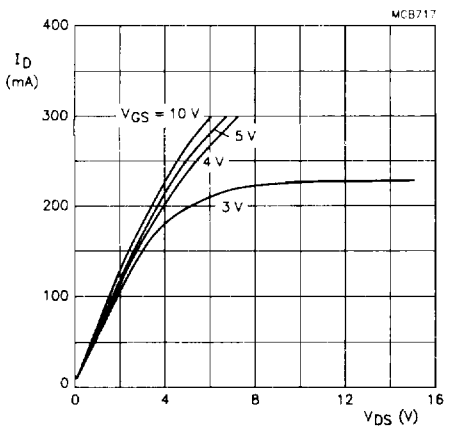


Fig.4 Typical output characteristics; T_j = 25° C.

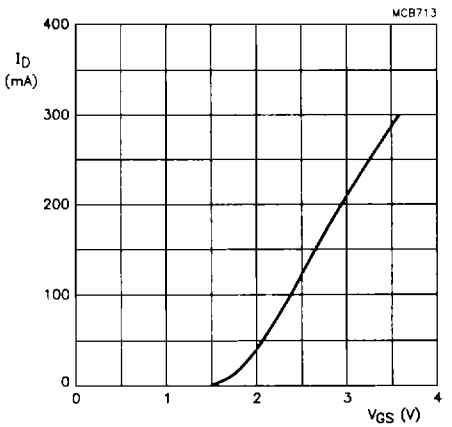


Fig.5 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25° C.

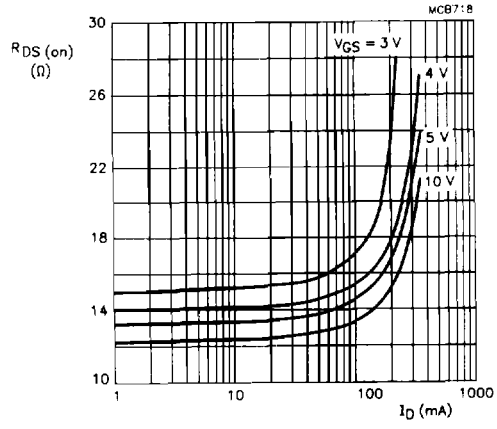


Fig.6 Typical on-resistance as a function of drain current; T_j = 25° C.

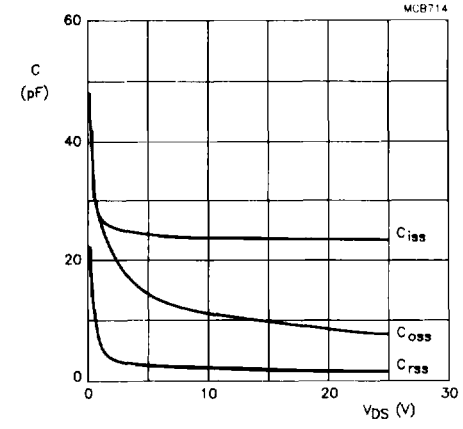


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25° C

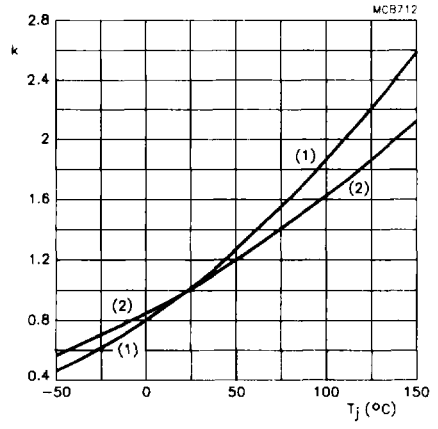


Fig.8 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25°\,C}$;

typical $R_{DS(on)}$ at 150 mA/10 V;

(1) I_D = 150 mA; V_{GS} = 10 V;
(2) I_D = 20 mA; V_{GS} = 2.6 V;

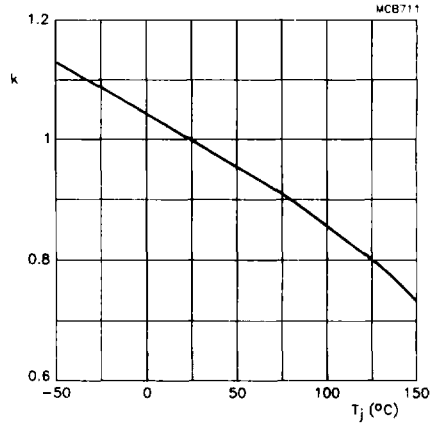


Fig.9 Temperature coefficient of gate-source threshold voltage;

$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25°\,C}$; typical $V_{Gs(th)}$ at 1 mA.

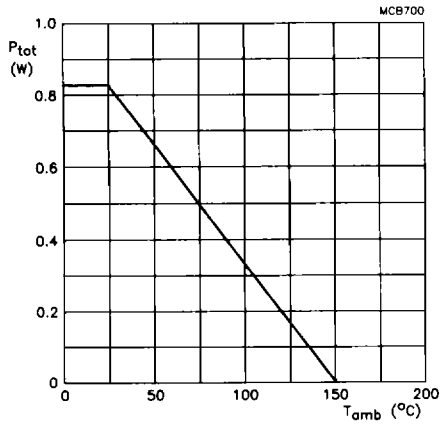


Fig.10 Power derating curve.