128Kx8 Static RAM CMOS, Monolithic

PRELIMINARY

The EDI88128C/LP/P* is a high performance, megabit density monolithic Static RAM organized as 128Kx8 bits, designed for use in systems where fast computation, low power, and board density are the main requirements. The military product has two low power versions, P and LP. The LP version offers a data retention function for battery back-up applications.

The EDI88128C/LP/P has eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

Military product compliant to MIL-STD-883, Paragraph 1.2.1 is available.

Features

128Kx8 bits Monolithic CMOS Static Random Access Memory

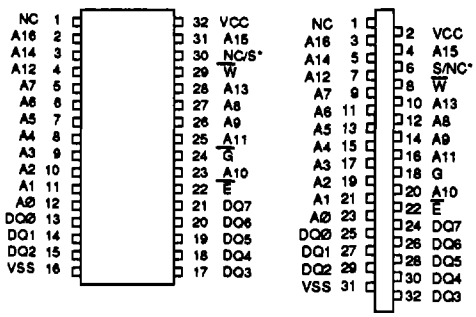
- One Megabit Density
- Fast Access Times of 35 thru 100ns
- Single (88128) or Dual (88130*) Chip Selects
- Battery Back-up Operation
  2V Data Retention (LP Version)
- Output Enable Function
- Inputs and Outputs Directly TTL Compatible

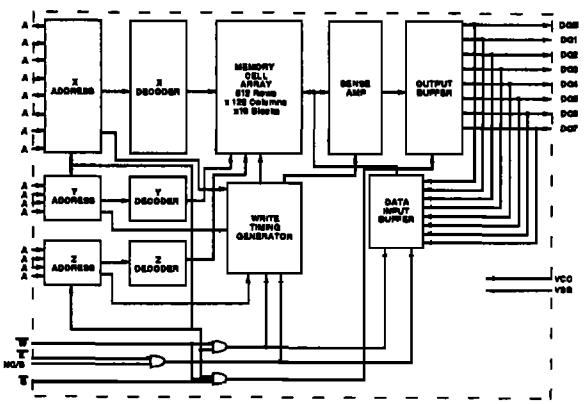
Six Ceramic Package Options, JEDEC Pinout

- 32 Pin Ceramic Dual-in-line Packages
  600 mils Wide Sidebrazed DIP, No. 9
  400 mils Wide Sidebrazed DIP, No. 102
- 32 Pin ZIP, No.100
- 32 Pad Ceramic LCC, No. 141
- 32 Lead CSOJ, No. 140
- 32 Lead Flatpack, No. 142

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram





Pin Names

AØ-A16	Address Inputs
$\overline{E}$	Chip Enables
$\overline{S}$*	Chip Select
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

* EDI88130 only

** **Note:** EDI88130C/LP/P is identical to the EDI88128C/LP/P, with an additional chip select line (S) which provides system memory security during power down in non battery backed up systems and memory banking in high speed battery backed systems where large multiple pages of memory are required. EDI88128C/LP/P and EDI88130C/LP/P are direct pin for pin replacements for EDI modules EDI8M8128C/LP/P and EDI8M8130C/LP/P, respectively.*

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial ..... -40°C to +85°C
Military ..... -55°C to +125°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA
Junction Temperature, TJ ..... 175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*		Max		Units
					35-55	70-100	35-55	70-100	
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, S = VIH, Min Cycle		--	80	80	150	95	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL VIN ≥ VIH		--			15	10	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V	C	--	1	1	10	5	mA
		VIN ≥ VCC-0.2V VIN ≤ 0.2V	LP/P				2	1	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	--	±5	±5	µA
Output Leakage Current	ILO	V I/O = 0V to VCC, $\overline{E}$ ≥ VIH		--	--	--	±10	±10	µA
Output High Voltage	VOH	IOH = -1.0mA (≤55ns=-4.0mA)		2.4	--	--	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA (≤55ns= 8.0mA)		--	--	--	0.4	0.4	V

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	S	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Output Deselect	High Z	ICC1
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		LCC	DIP, FP CSOJ	
Input Capacitance (Except DQ Pins)	CI	6	12	pF
Capacitance Control (DQ Pins)	CD/Q	8	14	pF

These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

Parameter	Symbol			35ns		45ns		55ns		Units
				Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV			35		45		55		ns
Address Access Time	TAVQV				35		45		55	ns
Chip Enable Access Time	TELQV	$\overline{E}$			35		45		55	ns
	TSHQV	S*			35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	$\overline{E}$		3		3		3		ns
	TSHQX	S*		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	$\overline{E}$			20		25		25	ns
	TSLQZ	S*			20		25		25	ns
Output Hold from Address Change	TAVQX			3		3		3		ns
Output Enable to Output Valid	TGLQV				20		25		25	ns
Output Enable to Output in Low Z (1)	TGLQX			0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ				20		25		25	ns

Note 1: Parameter guaranteed, but not tested.

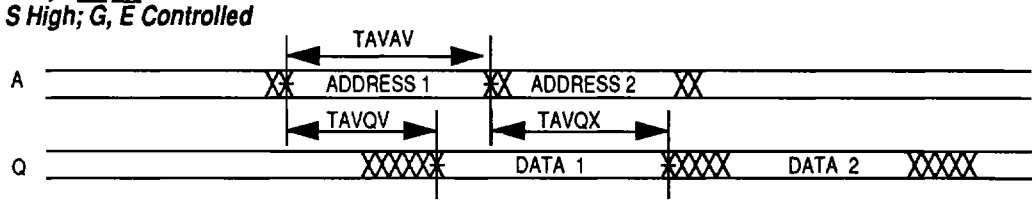
*EDI88130 Only

AC Characteristics
Read Cycle

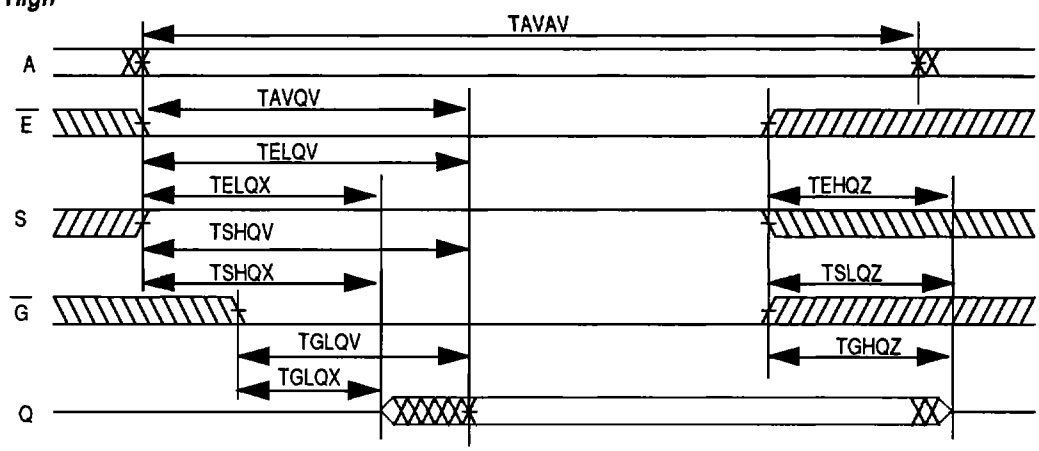
Parameter	Symbol			70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Read Cycle Time	TAVAV			70		85		100		ns
Address Access Time	TAVQV				70		85		100	ns
Chip Enable Access Time	TELQV	$\overline{E}$			70		85		100	ns
	TSHQV	S*			70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	$\overline{E}$		3		3		3		ns
	TSHQX	S*		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	$\overline{E}$		0	30	0	35	0	40	ns
	TSLQZ	S*		0	30	0	35	0	40	ns
Output Hold from Address Change	TAVQX			3		3		3		ns
Output Enable to Output Valid	TGLQV				35		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX			0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ			0	30	0	35	0	35	ns

Note 1: Parameter guaranteed, but not tested. *EDI88130 Only

Read Cycle 1
$\overline{W}$, S High; $\overline{G}$, $\overline{E}$ Controlled



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Write Cycle

Parameter	Symbol			35ns		45ns		55ns		Units
				Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV			35		45		55		ns
Chip Enable to End of Write	TELWH	$\overline{E}$		30		40		45		ns
	TELEH	$\overline{E}$		30		40		45		ns
	TSHWH	S*		30		40		45		ns
	TSHSL	S*		30		40		45		ns
Address Setup Time	TAVWL	$\overline{W}$		0		0		0		ns
	TAVEL	$\overline{E}$		0		0		0		ns
	TAVSH	S*		0		0		0		ns
Address Valid to End of Write	TAVWH			30		40		45		ns
Write Pulse Width	TWLWH	$\overline{W}$		30		40		45		ns
	TWLEH	$\overline{E}$		30		40		45		ns
	TWLSL	S*		30		40		45		ns
Write Recovery Time	TWHAX	$\overline{W}$		0		0		0		ns
	TEHAX	$\overline{E}$		0		0		0		ns
	TSLAX	S*		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$		0		0		0		ns
	TEHDX	$\overline{E}$		0		0		0		ns
	TSLDX	S*		0		0		0		ns
Write to Output in High Z (1)	TWLQZ			0	15	0	20	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$		20		25		25		ns
	TDVEH	$\overline{E}$		20		25		25		ns
	TDVSL	S*		20		25		25		ns
Output Active from End of Write (1)	TWHQX			3		3		3		ns

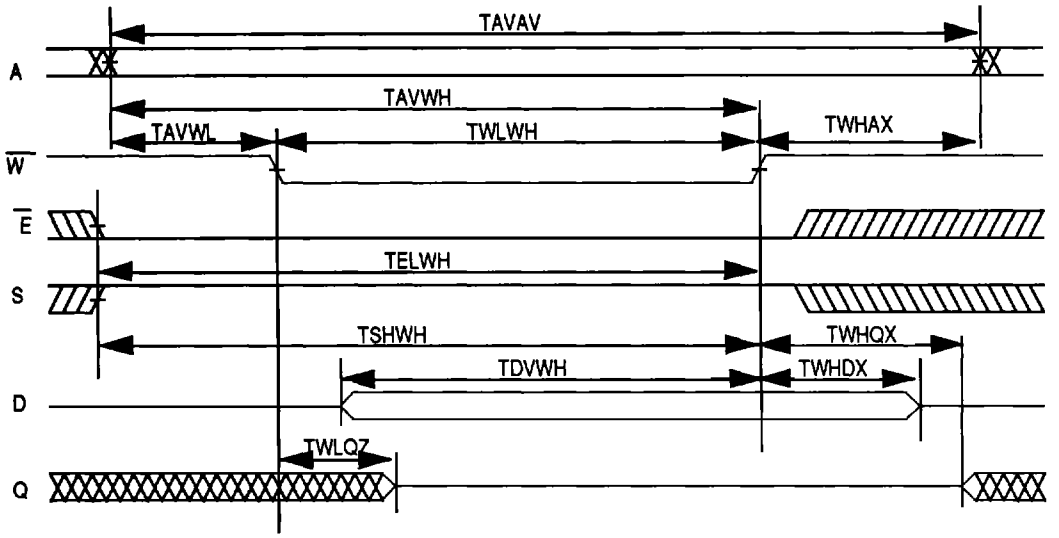
Note 1: Parameter guaranteed, but not tested. *EDI88130 Only.

AC Characteristics
Write Cycle

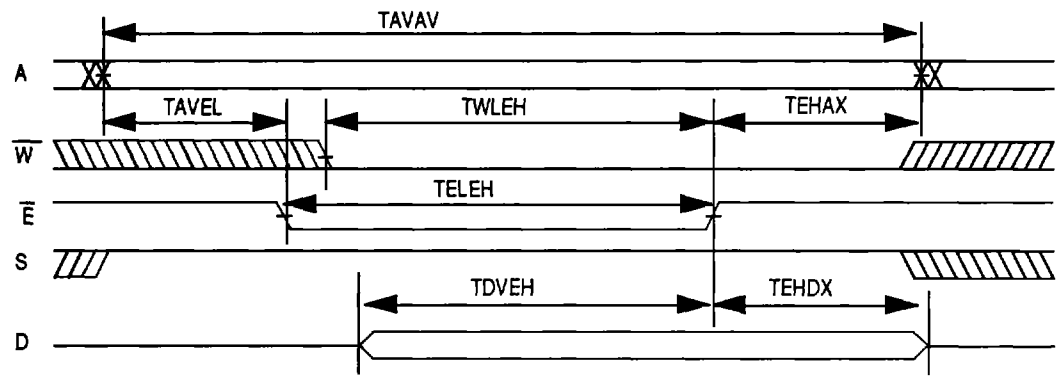
Parameter	Symbol			70ns		85ns		100ns		Units
				Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV			70		85		100		ns
Chip Enable to	TELWH	$\overline{E}$		65		70		80		ns
End of Write	TELEH	$\overline{E}$		65		70		80		ns
	TSHWH	S*		65		70		80		ns
	TSHSL	S*		65		70		80		ns
Address Setup Time	TAVWL	$\overline{W}$		0		0		0		ns
	TAVEL	$\overline{E}$		0		0		0		ns
	TAVSH	S*		0		0		0		ns
Address Valid to End of Write	TAVWH			65		70		80		ns
Write Pulse Width	TWLWH	$\overline{W}$		65		70		80		ns
	TWLEH	$\overline{E}$		65		70		80		ns
	TWLSL	S*		65		70		80		ns
Write Recovery Time	TWHAX	$\overline{W}$		0		0		0		ns
	TEHAX	$\overline{E}$		0		0		0		ns
	TSLAX	S*		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$		0		0		0		ns
	TEHDX	$\overline{E}$		0		0		0		ns
	TSLDX	S*		0		0		0		ns
Write to Output in High Z (1)	TWLQZ			0	30	0	35	0	40	ns
Data to Write Time	TDVWH	$\overline{W}$		30		35		40		ns
	TDVEH	$\overline{E}$		30		35		40		ns
	TDVSL	S*		30		35		40		ns
Output Active from End of Write (1)	TWHQX			5		5		5		ns

Note 1: Parameter guaranteed, but not tested. *EDI88130 Only.

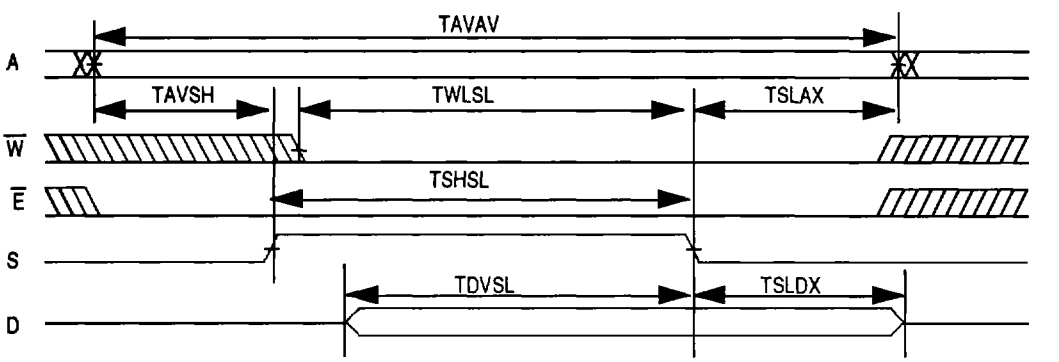
Write Cycle 1
Late Write, $\overline{W}$ Controlled



Write Cycle 2
Early Write, $\overline{E}$ Controlled



Write Cycle 3
Early Write, S Controlled



Data Retention Characteristics

(TA =-55°C to +125°C)

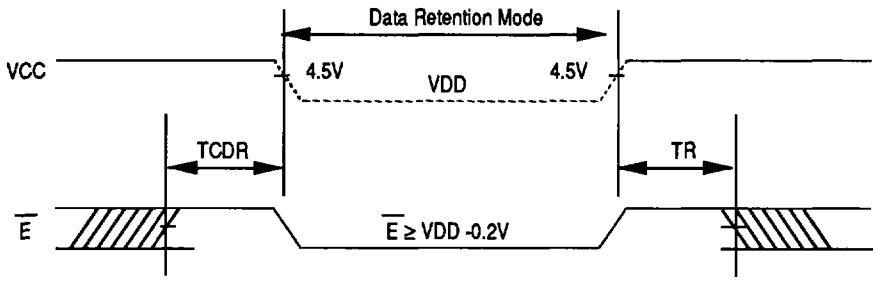
LP Versions Only

(EDI88128LP & EDI88130LP)

Characteristic	Sym	Test Conditions	Min	Typ	Max		Unit
					35-55	70-100	ns
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD -0.2V	--		750	400	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥ VDD -0.2V	0	--	--	--	ns
Operation Recovery Time	TR	or VIN ≤ 0.2V	TAVAV*	--	--	--	ns

*Read Cycle Time

Data Retention $\overline{E}$ Controlled



Data Retention S Controlled