STM8S20xxx

Performance line, 24 MHz. 8-bit MCU, up to 128 Kbytes Flash, integrated EEPROM,10-bit ADC, timers, 2 UARTs, SPI, I²C, CAN

Preliminary Data

Features

Core

- Max f_{CPU}: up to 24 MHz, 0 wait states @ $f_{CPU} \leq 16$ MHz
- Advanced STM8 core with Harvard architecture and 3-stage pipeline
- Extended instruction set
- Max. 20 MIPS @ 24 MHz

Memories

- Program memory: Up to 128 Kbytes Flash; data retention 20 years at 55°C after 10 kcycles
- Data memory: Up to 2 Kbytes true data EEPROM; endurance 300 kcycles
- RAM: Up to 6 Kbytes

Clock, reset and supply management

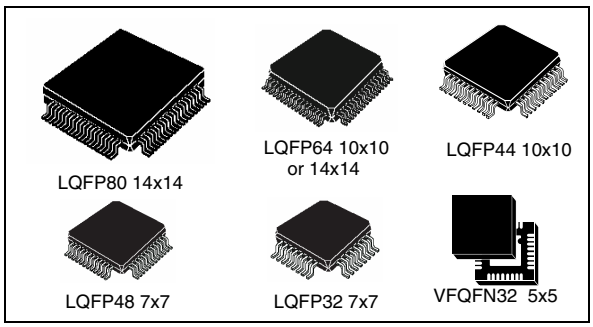
- 3.0 to 5.5 V operating voltage
- Flexible clock control, 4 master clock sources:
  - Low power crystal resonator oscillator
  - External clock input
  - Internal, user-trimmable 16 MHz RC
  - Internal low power 128 kHz RC
- Clock security system with clock monitor
- Power management:
  - Low power modes (Wait, Active-halt, Halt)
  - Switch-off peripheral clocks individually
- Permanently active, low consumption power-on and power-down reset

Interrupt management

- Nested interrupt controller with 32 interrupts
- Up to 37 external interrupts on 6 vectors

Timers

- 2x 16-bit general purpose timers, with 2+3 CAPCOM channels (IC, OC or PWM)
- Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
- 8-bit basic timer with 8-bit prescaler



- Auto wake-up timer
- Window watchdog and independent watchdog

Communications interfaces

- High speed 1 Mbit/s active CAN 2.0B interface
- UART with clock output for synchronous operation - LIN master mode
- UART with LIN 2.1 compliant, master/slave modes and automatic resynchronization
- SPI interface up to 10 Mbit/s
- I^2C interface up to 400 Kbit/s

Analog to digital converter (ADC)

- 10-bit, ±1 LSB ADC with up to 16 channels

I/Os

- Up to 68 I/Os on an 80-pin package including 11 high sink outputs
- Highly robust I/O design, immune against current injection

Development support

- Single Wire Interface Module (SWIM) and Debug Module (DM) for fast on-chip programming and non-intrusive debugging

Table 1. Device summary

Reference	Part number
STM8S207xx	STM8S207MB, STM8S207RB, STM8S207R8, STM8S207R6, STM8S207CB, STM8S207C8, STM8S207S8, STM8S207K6, STM8S207K4
STM8S208xx	STM8S208MB, STM8S208RB

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1 Introduction

This datasheet contains the description of the STM8S20x performance line features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016)
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051)
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470)
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044)

2 Description

The STM8S20x performance line 8-bit microcontrollers offer 32 Kbytes128 of program memory.

All devices of the STM8S20x performance line provide the following benefits:

- Reduced system cost
  - High system integration level with internal clock oscillators, watchdog and brown-out reset
- Performance and robustness
  - 20 MIPS at 24 MHz CPU clock frequency
  - Robust I/O, independent watchdogs with separate clock source
  - Clock security system
- Short development cycles
  - Applications scalability across a common family product architecture with compatible pinout, memory map and and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - A family of products for applications with 3.0 V to 5.5 V operating supply

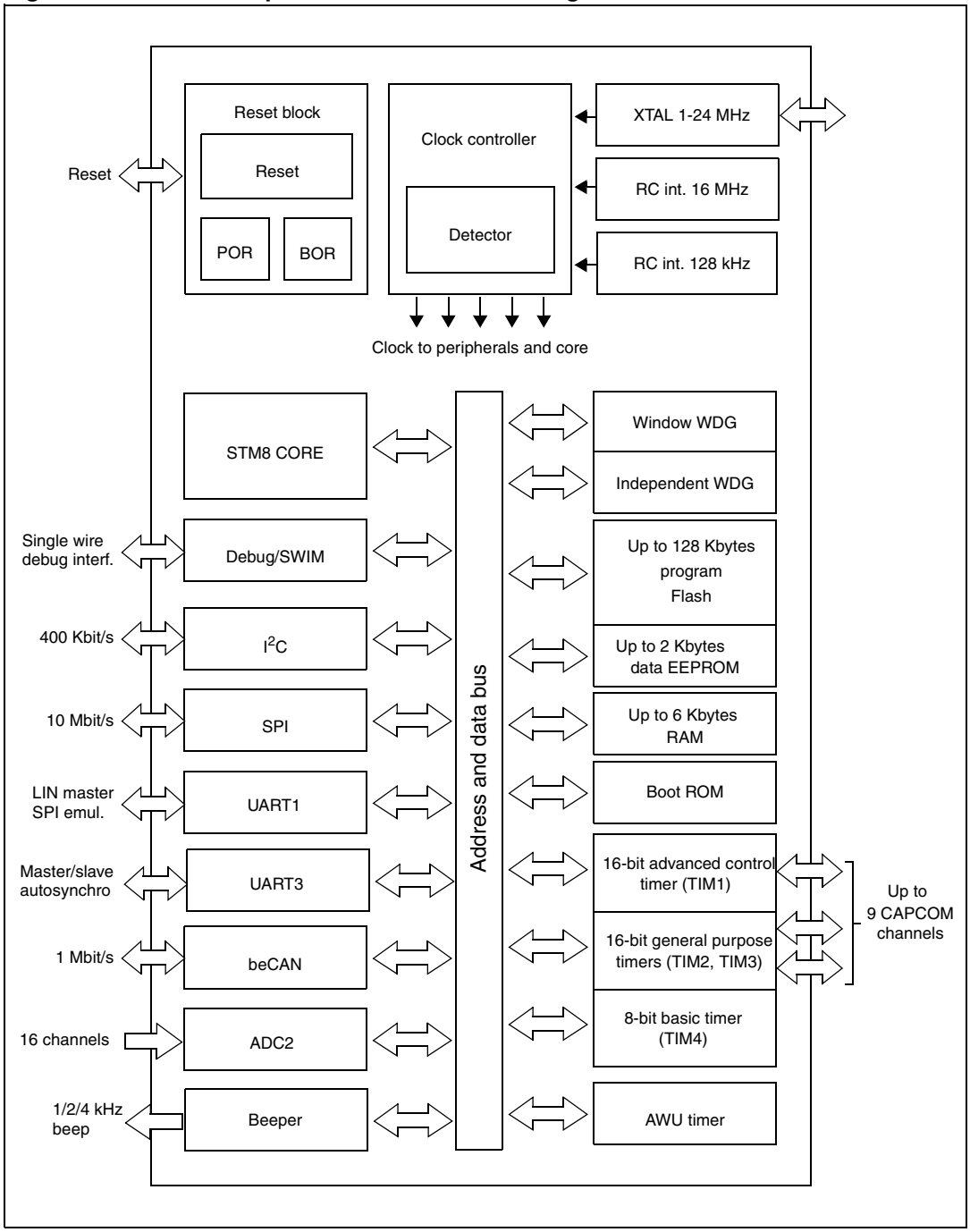
Table 2. STM8S20xxx performance line features

Device	Pin count	No. of maximum GPIO (I/O)	Ext. Interrupt pins	Timer CAPCOM channels	Timer PWM channels(1)	A/D Converter channels	Flash Program memory (bytes)	Data EEPROM (bytes)	RAM (bytes)	beCAN interface
STM8S207MB	80	68(2)	37	9	12	16	128K	2048	6K	
STM8S207R8	64	52(2)	37	9	12	16	64K	1536	4K	
STM8S207R6	64	52(2)	37	9	12	16	32K	1024	2K	
STM8S207RB	64	52(2)	37	9	12	16	128K	2048	6K	
STM8S207CB	48	38(3)	35	9	12	10	128K	2048	6K	-
STM8S207C8	48	38(3)	35	9	12	10	64K	1536	4K	
STM8S207S8	44	34(3)	31	8	11	9	64K	1536	4K	
STM8S207K6	32	25(3)	23	8	11	7	32	1024	2K	
STM8S207K4	32	25(3)	23	8	11	7	16	1024	2K	
STM8S208MB	80	68(2)	37	9	12	16	128K	2048	6K	Yes
STM8S208RB	64	52(2)	37	9	12	16	128K	2048	6K	

1. Including complementary outputs.
2. 11 high sink outputs (HS)
3. 9 high sink outputs (HS)

3 Block diagram

Figure 1. STM8S20x performance line block diagram



4 Product overview

The following section intends to give an overview of the basic features of the STM8S20x performance line functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module and permit non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- 2 advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 37 external interrupts on 6 vectors including TLI
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- Up to 128 Kbytes of program single voltage Flash memory
- Up to 2 K bytes true data EEPROM
- Read while write: Writing in data memory possible while executing code in program memory
- User option byte area

Write protection (WP)

Write protection of Flash and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (Memory Access Security System). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform In-Application Programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to *Figure 2.*

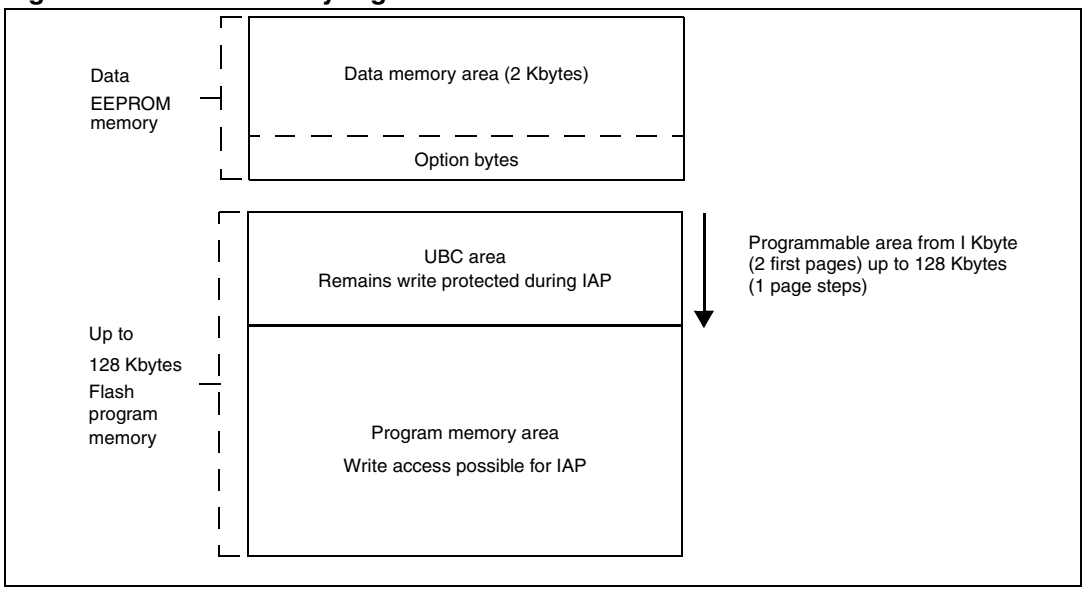
The size of the UBC is programmable through the UBC option byte (*Table 7.*), in increments of 1 page, by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in debug mode. Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** 4 different clock sources can be used to drive the master clock:
  - 1-24 MHz High Speed External crystal (HSE)
  - Up to 24 MHz High Speed user-external clock (HSE user-ext)
  - 16 MHz High Speed Internal RC oscillator (HSI)
  - 128 kHz Low Speed Internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

4.6 Power management

For efficent power management, the application can be put in one four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode**: in this mode, the CPU is stopped, but peripherals are kept running. The wake-up is performed by an internal or external interrupt or reset.
- **Fast active halt mode**: in this mode, the CPU and peripheral clocks are stopped. An internal wake-up is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is more than in slow active halt mode, but the wake-up time is faster. Wake-up is triggered by the internal AWU interrupt, external interrupt or reset.
- **Slow active halt mode**: this mode is the same as fast active halt except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode**: in this mode the microcontroller uses the least power, CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wake-up is triggered by external interrupt or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

The WDG timer activity is controlled by option bytes. Once activated the watchdog can not be disabled by the user program without reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower then the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHZ LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wake-up counter

- Used for auto wake-up from active halt mode
- Clock source: internal 128 kHz internal low frequency RC oscillator or external clock

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 4 independent capture/compare channels(CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signal
- Break input to force the timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchr-onization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM3	16	Any power of 2 from 1 to 32768	Up	2	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog/digital converter (ADC2)

- STM8S20x performance line products contain a 10-bit successive approximation A/D converter (ADC2) with up to 16 multiplexed input channels and the following main features:
  - Input voltage range: 0 to V_{DDA}
  - Dedicated voltage reference (VREF) pins available on 80 and 64-pin devices
  - Conversion time: 14 clock cycles
  - Single and continuous modes
  - External trigger input
  - Trigger from TIM1 TRGO
  - End of conversion (EOC) interrupt

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1:
  - Full feature UART, SPI emulation, LIN2.1 master capability, Smartcard mode, IrDA mode, single wire mode
- UART3:
  - Full feature UART, LIN2.1 master/slave capability.
- SPI - full and half-duplex, 10 Mbit/s
- I²C - up to 400 Kbit/s
- CAN (rev. 2.0A,B) - 3 Tx mailboxes - up to 1 Mbit/s

4.14.1 UART1

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of

following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- 2 receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit synch break frame
- Reception: Detects 11-bit break frame

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Max. speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

4.14.2 UART3

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- High precision baud rate generator

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- 2 receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit synch break frame
- Reception: Detects 11-bit break frame

LIN slave

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15 %
- Synch delimiter checking
- 11-bit LIN synch break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.14.3 SPI

- Maximum speed: 10 Mbit/s ($f_{MASTER}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

4.14.4 I^2C

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)

4.14.5 CAN

The beCAN3 controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It has been designed to manage a high number of incoming messages efficiently with a minimum CPU load.

For safety-critical applications the CAN controller provides all hardware functions to support the CAN time triggered communication option (TTCAN).

The maximum transmission speed is 1 Mbit.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request
- Time stamp on SOF transmission

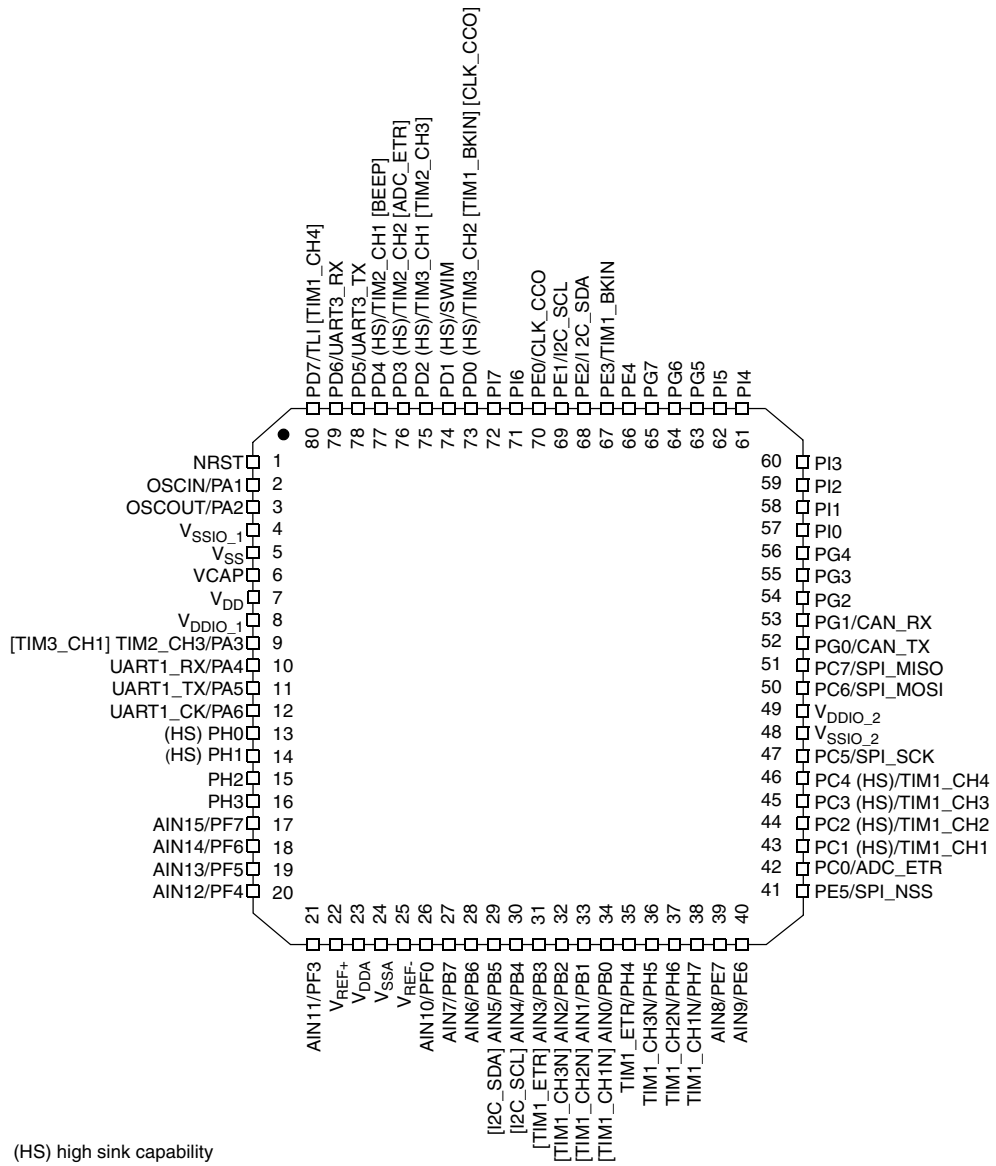
Reception

- 8-, 11- and 29-bit ID
- 1 receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message
- Configurable FIFO overrun
- Time stamp on SOF reception
- 6 filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID
- Filtering modes:
  - Mask mode permitting ID range filtering
  - ID list mode
- Time triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Configurable timer resolution
  - Time stamp sent in last two data bytes

5 Pinouts and pin description

5.1 Package pinouts

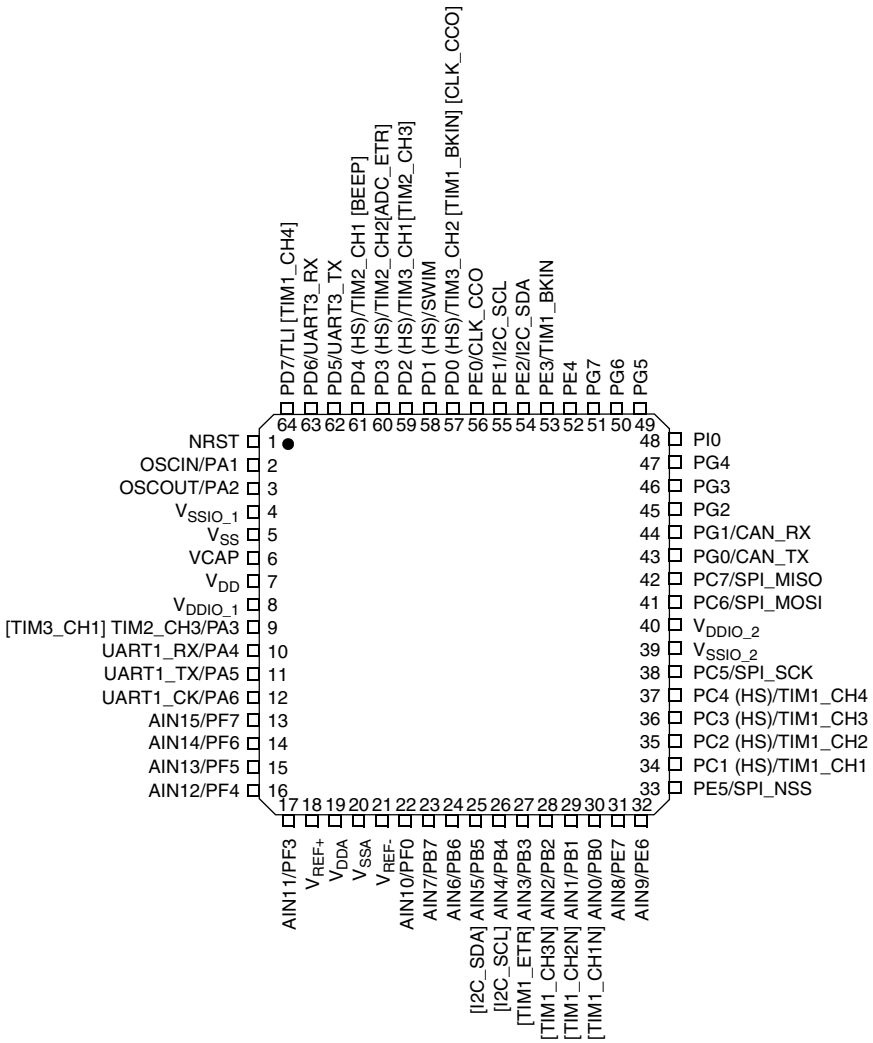
Figure 3. LQFP 80-pin pinout



(HS) high sink capability

[ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

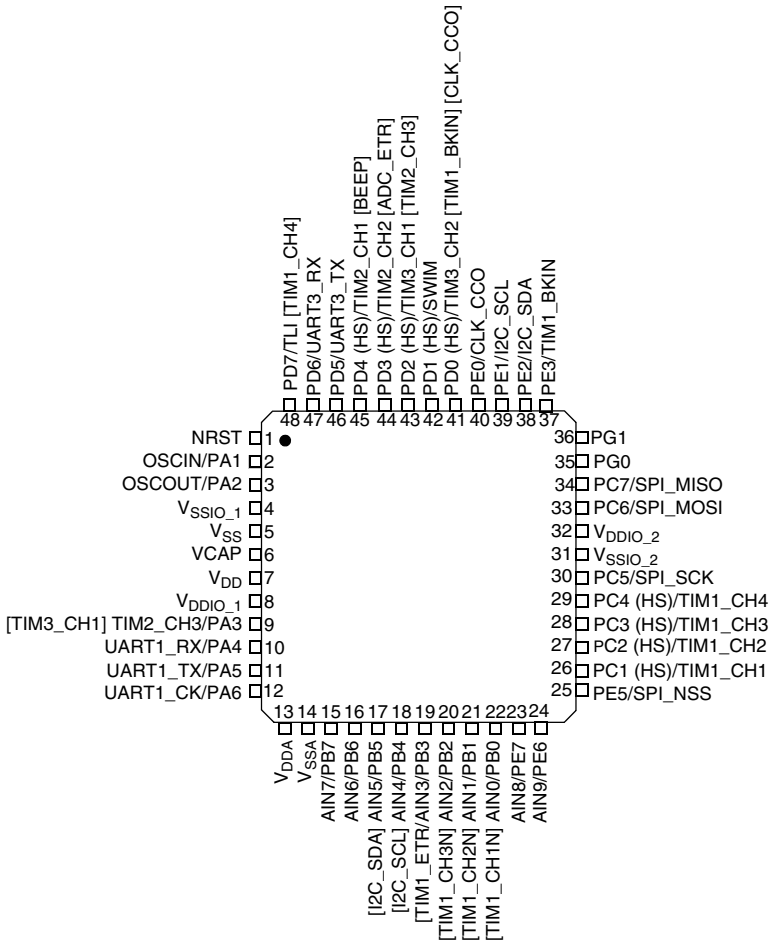
Figure 4. LQFP 64-pin pinout



(HS) high sink capability

[ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

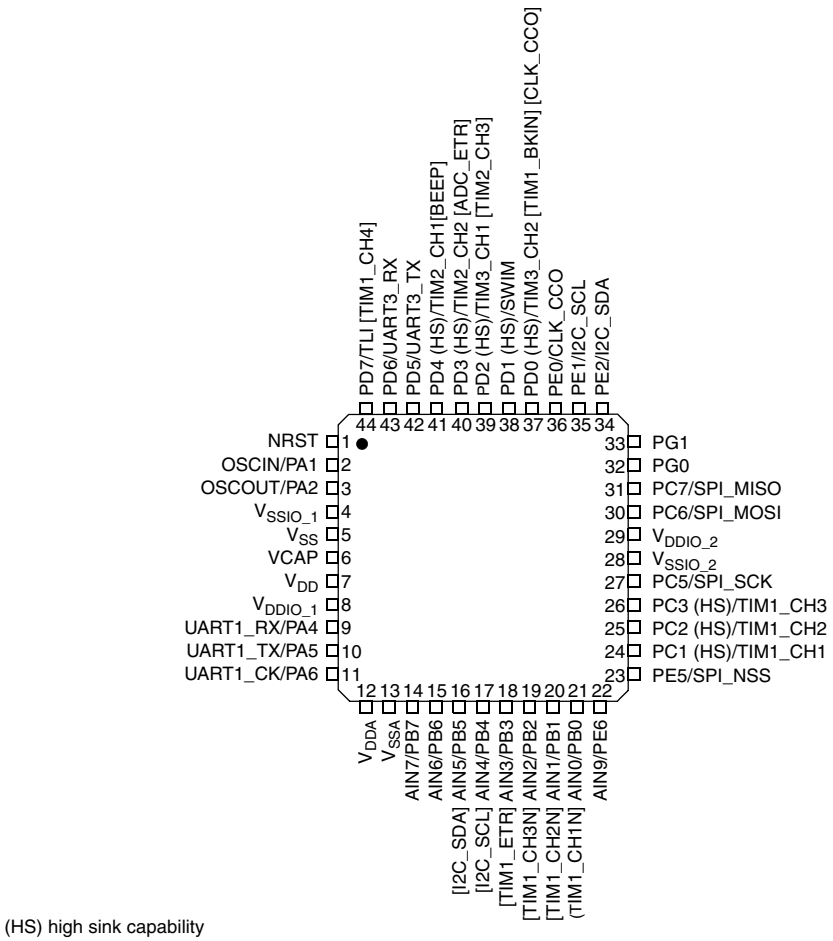
Figure 5. LQFP 48-pin pinout



(HS) high sink capability

[ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

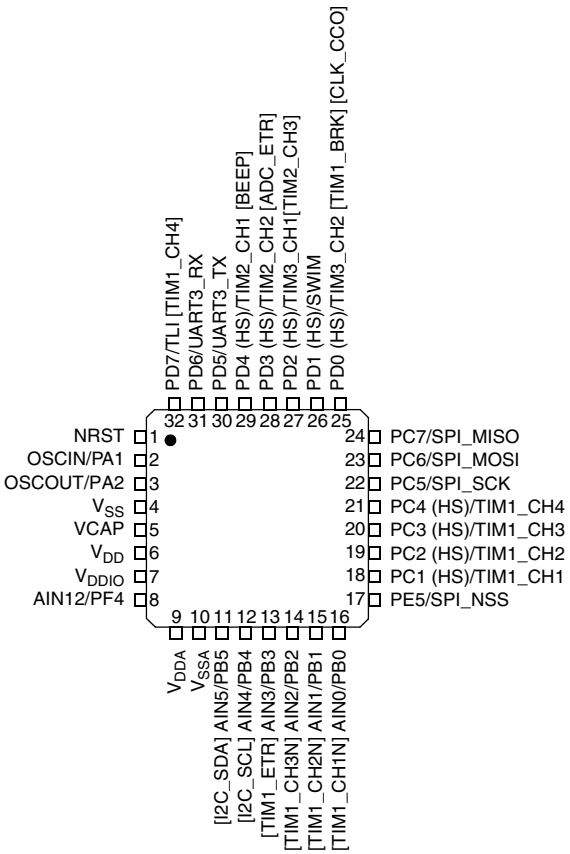
Figure 6. LQFP 44-pin pinout



(HS) high sink capability

[ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 7. VQFN32/LQFP 32-pin pinout



(HS) high sink capability

[ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 4. Legend/abbreviations

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull

Reset state is shown in **bold**.

Table 5. Pin description

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	VQFN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	1	1	NRST	I/O		**X**						Reset		
2	2	2	2	2	PA1/OSCIN	I/O	**X**	X			O1	X	X	**Port A1**	Resonator/ crystal in	
3	3	3	3	3	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/ crystal out	
4	4	4	4	-	V_{SSIO_1}	S								I/O ground		
5	5	5	5	4	V_{SS}	S								Digital ground		
6	6	6	6	5	VCAP	S								1.8 V regulator capacitor		
7	7	7	7	6	V_{DD}	S								Digital power supply		
8	8	8	8	7	V_{DDIO_1}	S								I/O power supply		
9	9	9	-	-	PA3/TIM2_CH3	I/O	**X**	X	X		O1	X	X	**Port A3**	Timer 2 - channel3	TIM3_CH1 [AFR1]
10	10	10	9	-	PA4/UART1_RX	I/O	**X**	X	X		O3	X	X	**Port A4**	UART1 receive	
11	11	11	10	-	PA5/UART1_TX	I/O	**X**	X	X		O3	X	X	**Port A5**	UART1 transmit	
12	12	12	11	-	PA6/UART1_CK	I/O	**X**	X	X		O3	X	X	**Port A6**	UART1 synchronous clock	
13	-	-	-	-	PH0	I/O	**X**	X		HS	O3	X	X	**Port H0**		
14	-	-	-	-	PH1	I/O	**X**	X		HS	O3	X	X	**Port H1**		
15	-	-	-	-	PH2	I/O	**X**	X			O1	X	X	**Port H2**		
16	-	-	-	-	PH3	I/O	**X**	X			O1	X	X	**Port H3**		
17	13	-	-	-	PF7/AIN15	I/O	**X**	X			O1	X	X	**Port F7**	Analog input 15	
18	14	-	-	-	PF6/AIN14	I/O	**X**	X			O1	X	X	**Port F6**	Analog input 14	
19	15	-	-	-	PF5/AIN13	I/O	**X**	X			O1	X	X	**Port F5**	Analog input 13	
20	16	-	-	8	PF4/AIN12	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12	
21	17	-	-	-	PF3/AIN11	I/O	**X**	X			O1	X	X	**Port F3**	Analog input 11	
22	18	-	-	-	V_{REF+}	S								ADC positive reference voltage		
23	19	13	12	9	V_{DDA}	S								Analog power supply		

Table 5. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	VQFN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24	20	14	13	10	V_{SSA}	S								Analog ground		
25	21	-	-	-	V_{REF-}	S								ADC negative reference voltage		
26	22	-	-	-	PF0/AIN10	I/O	**X**	X			O1	X	X	**Port F0**	Analog input 10	
27	23	15	14	-	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
28	24	16	15	-	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
29	25	17	16	11	PB5/AIN5	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	17	12	PB4/AIN4	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
31	27	19	18	13	PB3/AIN3	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	19	14	PB2/AIN2	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input	TIM1_ CH3N [AFR5]
33	29	21	20	15	PB1/AIN1	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_ CH2N [AFR5]
34	30	22	21	16	PB0/AIN0	I/O	**X**	X	X		O1	X	X	**Port B0**	Analog input 0	TIM1_ CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	**X**	X			O1	X	X	**Port H4**	Timer 1 - trigger input	
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	**X**	X			O1	X	X	**Port H5**	Timer 1 - inverted channel 3	
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	**X**	X			O1	X	X	**Port H6**	Timer 1 - inverted channel 2	
38	-	-	-	-	PH7/ TIM1_CH1N	I/O	**X**	X			O1	X	X	**Port H7**	Timer 1 - inverted channel 2	
39	31	23	-	-	PE7/AIN8	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 8	
40	32	24	22	-	PE6/AIN9	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 9	
41	33	25	23	17	PE5/SPI_NSS	I/O	**X**	X	X		O1	X	X	**Port E5**	SPI master/slave select	

Table 5. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	VQFN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
42	-	-	-	-	PC0/ADC_ETR	I/O	**X**	X	X		O1	X	X	**Port C0**	ADC trigger input	
43	34	26	24	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	
44	35	27	25	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	
45	36	28	26	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	
46	37	29	-	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	
47	38	30	27	22	PC5/SPI_SCK	I/O	**X**	X	X		O3	X	X	**Port C5**	SPI clock	
48	39	31	28	-	V_{SSIO_2}	S								I/O ground		
49	40	32	29	-	V_{DDIO_2}	S								I/O power supply		
50	41	33	30	23	PC6/SPI_MOSI	I/O	**X**	X	X		O3	X	X	**Port C6**	SPI master out/ slave in	
51	42	34	31	24	PC7/SPI_MISO	I/O	**X**	X	X		O3	X	X	**Port C7**	SPI master in/ slave out	
52	43	35	32	-	PG0/CAN_TX	I/O	**X**	X			O1	X	X	**Port G0**	CAN transmit	
53	44	36	33	-	PG1/CAN_RX	I/O	**X**	X			O1	X	X	**Port G1**	CAN receive	
54	45	-	-	-	PG2	I/O	**X**	X			O1	X	X	**Port G2**		
55	46	-	-	-	PG3	I/O	**X**	X			O1	X	X	**Port G3**		
56	47	-	-	-	PG4	I/O	**X**	X			O1	X	X	**Port G4**		
57	48	-	-	-	PI0	I/O	**X**	X			O1	X	X	**Port I0**		
58	-	-	-	-	PI1	I/O	**X**	X			O1	X	X	**Port I1**		
59	-	-	-	-	PI2	I/O	**X**	X			O1	X	X	**Port I2**		
60	-	-	-	-	PI3	I/O	**X**	X			O1	X	X	**Port I3**		
61	-	-	-	-	PI4	I/O	**X**	X			O1	X	X	**Port I4**		
62	-	-	-	-	PI5	I/O	**X**	X			O1	X	X	**Port I5**		
63	49	-	-	-	PG5	I/O	**X**	X			O1	X	X	**Port G5**		
64	50	-	-	-	PG6	I/O	**X**	X			O1	X	X	**Port G6**		
65	51	-	-	-	PG7	I/O	**X**	X			O1	X	X	**Port G7**		
66	52	-	-	-	PE4	I/O	**X**	X	X		O1	X	X	**Port E4**		

Table 5. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	VQFN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
67	53	37	-	-	PE3/TIM1_BKIN	I/O	**X**	X	X		O1	X	X	**Port E3**	Timer 1 - break input	
68	54	38	34	-	PE2/I²C_SDA	I/O	**X**	X	X		O1	T(1)	X	**Port E2**	I²C data	
69	55	39	35	-	PE1/I²C_SCL	I/O	**X**	X	X		O1	T(1)	X	**Port E1**	I²C clock	
70	56	40	36	-	PE0/CLK_CCO	I/O	**X**	X	X		O3	X	X	**Port E0**	Configurable clock output	
71	-	-	-	-	PI6	I/O	**X**	X			O1	X	X	**Port I6**		
72	-	-	-	-	PI7	I/O	**X**	X			O1	X	X	**Port I7**		
73	57	41	37	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	38	26	PD1/SWIM	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
75	59	43	39	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
76	60	44	40	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	41	29	PD4/TIM2_CH1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
78	62	46	42	30	PD5/ UART3_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	UART3 data transmit	
79	63	47	43	31	PD6/ UART3_RX	I/O	**X**	X	X		O1	X	X	**Port D6**	UART3 data receive	
80	64	48	44	32	PD7/TLI	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	TIM1_CH4 [AFR4]

1. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented)

5.1.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of 8 AFR (alternate function remap) option bits. Refer to *Section 6: Option bytes on page 31*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see GPIO section of the family reference manual, RM0016).

6 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 6: Option bytes* below. Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be toggled in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 6. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
4800h	Read-out protection (ROP)	OPT0	ROP[7:0]								00h
4801h	User boot code(UBC)	OPT1	UBC[7:0]								00h
4802h		NOPT1	NUBC[7:0]								FFh
4803h	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	00h
4804h		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	FFh
4805h	Watchdog option	OPT3	Reserved				LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	00h
4806h		NOPT3	Reserved				NLSI_EN	NIWDG_HW	NWWDG_HW	NWWDG_HALT	FFh
4807h	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	00h
4808h		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	FFh
4809h	HSE clock startup	OPT5	HSECNT[7:0]								00h
480Ah		NOPT5	NHSECNT[7:0]								FFh
480Bh	Reserved	OPT6	Reserved								00h
480Ch		NOPT6	Reserved								FFh
480Dh	Flash wait states	OPT7	Reserved							Wait state	00h
480Eh		NOPT7	Reserved							Nwait state	FFh
487Eh	Bootloader	OPTBL	BL[7:0]								00h
487Fh		NOPTBL	NBL[7:0]								FFh

Table 7. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** *Memory readout protection (ROP)* AAh: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** *User boot code area* 00h: no UBC, no write-protection 01h: Pages 0 to 1 defined as UBC, memory write-protected 02h: Pages 0 to 3 defined as UBC, memory write-protected 03h: Pages 0 to 4 defined as UBC, memory write-protected ... FEh: Pages 0 to 255 defined as UBC, memory write-protected FFh: Reserved *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7***Alternate function remapping option 7* 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6** *Alternate function remapping option 6* 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL **AFR5** *Alternate function remapping option 5* 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N **AFR4** *Alternate function remapping option 4* 0: Port D7 alternate function = TLI 1: Port D7 alternate function = TIM1_CH4 **AFR3** *Alternate function remapping option 3* 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2** *Alternate function remapping option 2* 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO Note: AFR2 option has priority over AFR3 if both are activated **AFR1** *Alternate function remapping option 1* 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3 **AFR0** *Alternate function remapping option 0* 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

Table 7. Option byte description (continued)

Option byte no.	Description
OPT3	**LSI_EN:** *Low speed internal clock enable* 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: *Independent watchdog* 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: *Window watchdog activation* 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: *Window watchdog reset on halt* 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK:** *External clock selection* 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: *Auto wake-up unit/clock* 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU
	PRSC[1:0] AWU clock prescaler 00: 24 MHz to 128 kHz prescaler 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* This configures the stabilisation time to 0, 16, 256, 4096 HSE cycles.
OPT6	Reserved
OPT7	**WAITSTATE** *Wait state configuration* This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory. 1 wait state is required if f_{CPU} > 16 MHz. 0: No wait state 1: 1 wait state
OPTBL	**BL[7:0]** *Bootloader option byte* This option is checked by the boot ROM code after reset. Depending on content of addresses 487Eh, 487Fh and 8000h (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to STM8S bootloader manual for more details.

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

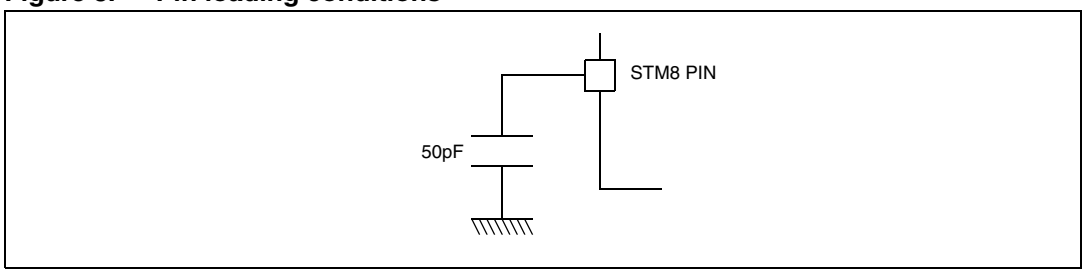
7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

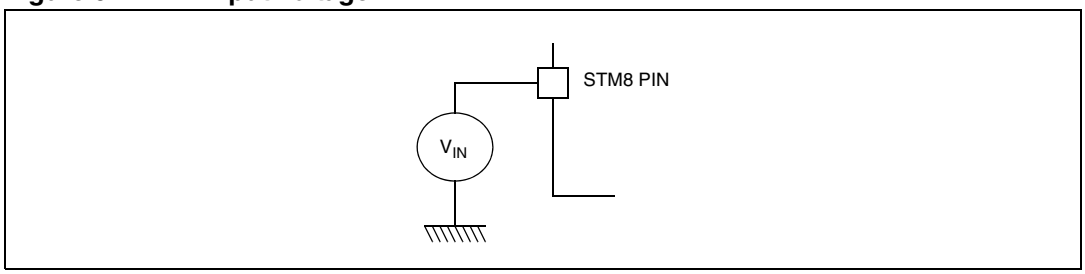
Figure 8. Pin loading conditions



7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 9. Pin input voltage



7.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{SS} \rvert$	Variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins		50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 65*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 9. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	60	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	60	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	- 20	
$I_{INJ(PIN)}$(2)(3)	Injected current on NRST pin	± 4	
	Injected current on OSCIN pin	± 4	
	Injected current on any other pin(4)	± 4	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(4)	± 20	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Negative injection disturbs the analog performance of the device. See note in *Section 7.3.10: 10-bit ADC characteristics on page 61*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 10. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	

7.3 Operating conditions

Table 11. General operating conditions(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	$T_A \leq 105$ °C	0	24	MHz
			0	16	MHz
V_{DD}/V_{DD_IO}	Standard operating voltage		3.0	5.5	V
P_D	Power dissipation at T_A= 85° C for suffix 6 or T_A= 125° C for suffix 3	LQFP80		TBD	mW
		LQFP64		TBD	
		LQFP48		TBD	
		LQFP44		TBD	
		LQFP32		TBD	
		VFQFN32		TBD	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation(2)	-40	105	°C
	Ambient temperature for 3 suffix version	Maximum power dissipation	-40	125	°C
		Low power dissipation (2)	-40	TBD	°C
T_J	Junction temperature range	6 suffix version	-40	105	°C
		3 suffix version	-40	TBD	°C

1. TBD = to be determined.
2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.4: Thermal characteristics on page 67*).

Figure 10. f_{CPUmax} Versus V_{DD}

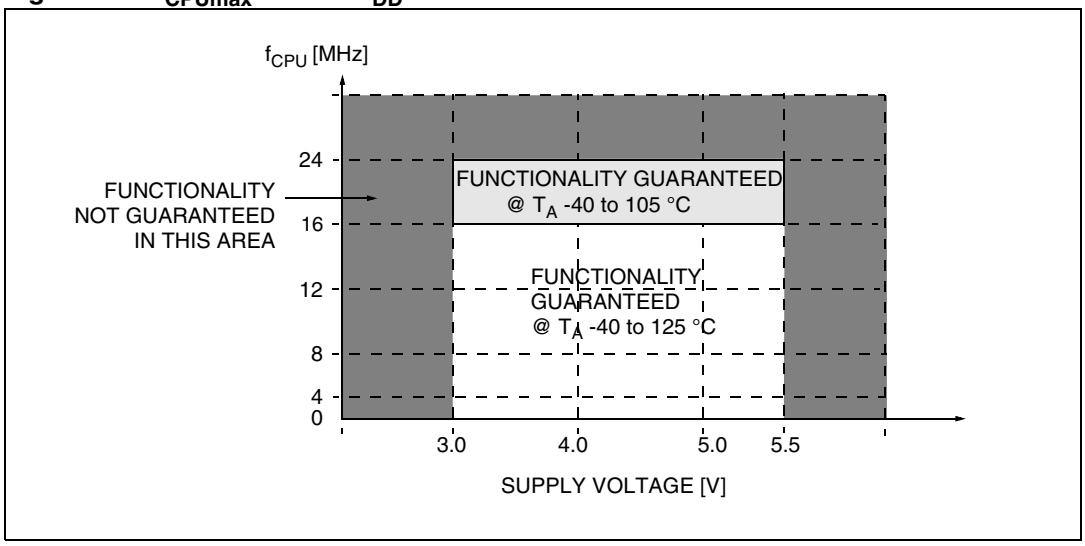


Table 12. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate		20(1)		∞	µs/V
	V_{DD} fall time rate(2)		20(1)		∞	
t_{TEMP}	Reset release delay	V_{DD} rising	TBD(1)	3		ms
	Reset generation delay(2)	V_{DD} falling	TBD(1)	3		µs
V_{IT+}	Power-on reset threshold		2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold		2.58	2.73	2.88	V
$V_{HYS(BOR)}$	Brown-out reset hysteresis			70		mV

1. Guaranteed by design. not tested in production.
2. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.

7.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 8 on page 34* and *Figure 9 on page 35*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 13. Total current consumption in run, wait and slow modes at V_{DD} = 5.0 V(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode	All peripherals off, code executed from RAM	HSE external clock/ $f_{CPU}=f_{MASTER}$=24 MHz	5.3	TBD(2)	mA
			HSE external clock/ $f_{CPU}=f_{MASTER}$=16 MHz	4.2	TBD	mA
			HSI internal RC/ $f_{CPU}=f_{MASTER}$=16 MHz	2.5	TBD	mA
		All peripherals off, code executed from Flash	HSE external clock/ $f_{CPU}=f_{MASTER}$=24 MHz	TBD	TBD(2)	mA
			HSE external clock/ $f_{CPU}=f_{MASTER}$=16 MHz	TBD	TBD	mA
			HSI internal RC/ $f_{CPU}=f_{MASTER}$=16 MHz	TBD	TBD	mA
$I_{DD(WFI)}$	Supply current in wait mode	CPU not clocked, all peripherals off	HSE external clock/ f_{MASTER}=24 MHz	3.3	TBD(2)	mA
			HSE external clock/ f_{MASTER}=16 MHz	2.9	TBD(2)	mA
			HSI internal RC/ f_{MASTER}=16 MHz	1.3	TBD(2)	mA
$I_{DD(SLOW)}$	Supply current in slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	HSE external clock/ $f_{CPU}=f_{MASTER}$=16 MHz/128	2.7	TBD(2)	mA
			HSI internal RC/ $f_{CPU}=f_{MASTER}$=16 MHz/128	1.0	TBD(2)	mA

1. TBD = to be determined.
2. Data based on characterization results, not tested in production

Table 14. Total current consumption and timing in halt, fast active halt and slow active halt modes at V_{DD} = 5.0 V(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(H)}$	Supply current in halt mode		5.5	TBD	µA
$I_{DD(FAH)}$	Supply current in fast active halt mode	HSE osc 16 MHz	600	TBD(2)	
		LSI RC 128 kHz	250	TBD(2)	
$I_{DD(SAH)}$	Supply current in slow active halt mode	HSE osc 16 MHz	490	TBD(2)	
		LSI RC 128 kHz	11.5	TBD(2)	
$t_{WU(FAH)}$	Wake-up time from fast active halt mode to run mode			2(2)	µs
$t_{WU(SAH)}$	Wake-up time from slow active halt mode to run mode			100(2)	µs

1. TBD = to be determined.
2. Data based on characterization results, not tested in production

Table 15. Total current consumption in run, wait and slow modes at V_{DD} = 3.3 V(1)

Symbol	Parameter	Conditions		Typ	Max (2)	Unit
$I_{DD(RUN)}$	Supply current in run mode	All peripherals off, code executed from RAM	HSE external clock/ $f_{CPU}=f_{MASTER}$=24 MHz	4.7	TBD	mA
			HSE external clock/ $f_{CPU}=f_{MASTER}$=16 MHz	3.6	TBD	mA
			HSI internal RC/ $f_{CPU}=f_{MASTER}$=16 MHz	2.6	TBD	mA
$I_{DD(WFI)}$	Supply current in wait mode	CPU not clocked, all peripherals off	HSE external clock/ f_{MASTER}=24 MHz	2.7	TBD	mA
			HSE external clock/ f_{MASTER}=16 MHz	2.3	TBD	mA
			HSI internal RC/ f_{MASTER}=16 MHz	1.3	TBD	mA
$I_{DD(SLOW)}$	Supply current in slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	HSE external clock/ $f_{CPU}=f_{MASTER}$=16 MHz/128	2.1	TBD	mA
			HSI internal RC/ $f_{CPU}=f_{MASTER}$=16 MHz/128	1.1	TBD	mA

1. TBD = to be determined.
2. Data based on characterisation results, not tested in production

Table 16. Total current consumption and timing in halt, fast active halt and slow active halt modes at V_{DD} = 3.3 V(1)

Symbol	Parameter	Conditions		Typ	Max(2)	Unit
$I_{DD(H)}$	Supply current in halt mode	All clocks off		4.0	TBD	µA
$I_{DD(FAH)}$	Supply current in fast active halt mode	Auto wake-up unit (AWU) active	HSE osc 16 MHz	560	TBD	
			LSI RC 128 kHz	145	TBD	
$I_{DD(SAH)}$	Supply current in slow active halt mode		HSE osc 16 MHz	430	TBD	
			LSI RC 128 kHz	9.5	TBD	
$t_{WU(FAH)}$	Wake-up time from fast active halt mode to run mode				2	µs
$t_{WU(SAH)}$	Wake-up time from slow active halt mode to run mode				100	µs

1. TBD = to be determined.
2. Data based on characterization results, not tested in production

On-chip peripherals

Table 17. Peripheral current consumption(1)

Symbol	Parameter	Typ. V_{DD} = 3.3 V	Typ. V_{DD} = 5 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current (2)	TBD	TBD	mA
$I_{DD(TIM2)}$	TIM2 supply current (2)	TBD	TBD	
$I_{DD(TIM3)}$	TIM3 timer supply current (2)	TBD	TBD	
$I_{DD(TIM4)}$	TIM4 timer supply current (2)	TBD	TBD	
$I_{DD(UART1)}$	UART1 supply current (3)	TBD	TBD	
$I_{DD(UART3)}$	UART3 supply current (3)	TBD	TBD	
$I_{DD(SPI)}$	SPI supply current (3)	TBD	TBD	
$I_{DD(I^2C)}$	I^2C supply current (3)	TBD	TBD	
$I_{DD(CAN)}$	CAN supply current (4)	TBD	TBD	
$I_{DD(ADC2)}$	ADC2 supply current when converting (5)	TBD	TBD	

1. TBD = to be determined.
2. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
3. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling.
4. Data based on a differential IDD measurement between reset configuration (CAN disabled) and a permanent CAN data transmit sequence in loopback mode at 1MHz. This measurement does not include the pad toggling consumption.
5. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Current consumption curves

Figure 11 to *Figure 16* show typical current consumption measured with code executing in RAM.

Figure 11. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz

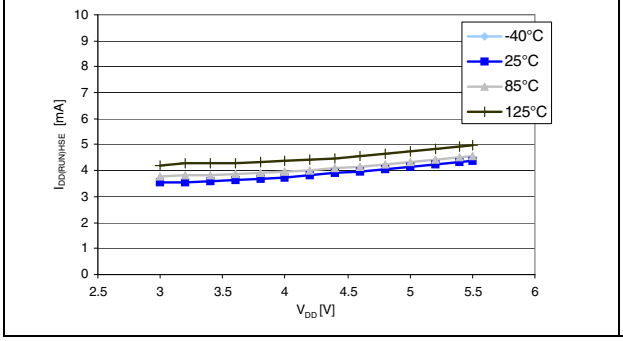


Figure 12. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V

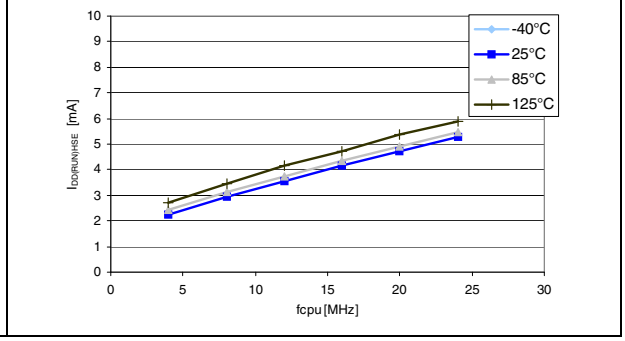


Figure 13. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz

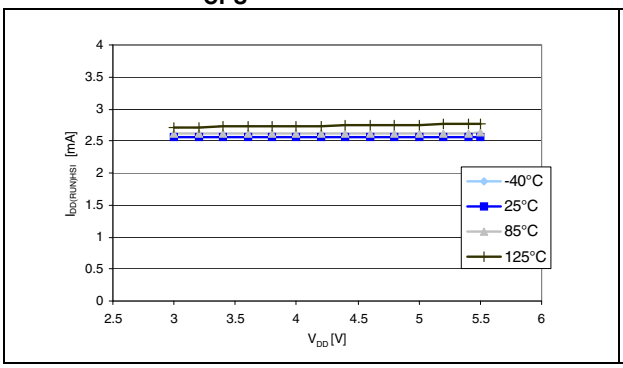


Figure 14. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz

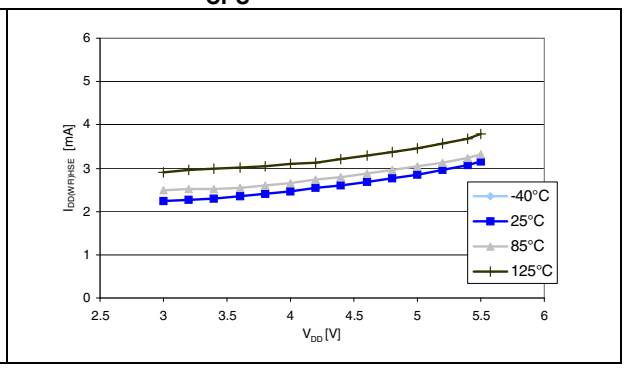


Figure 15. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V

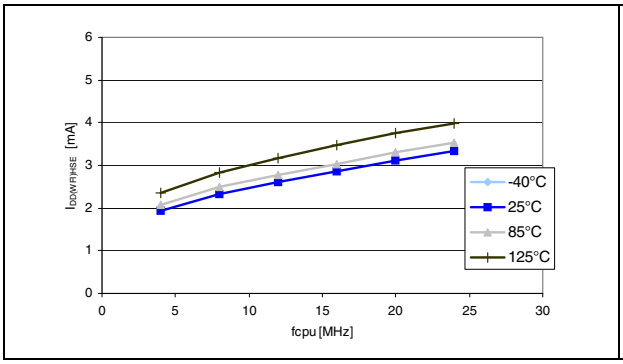
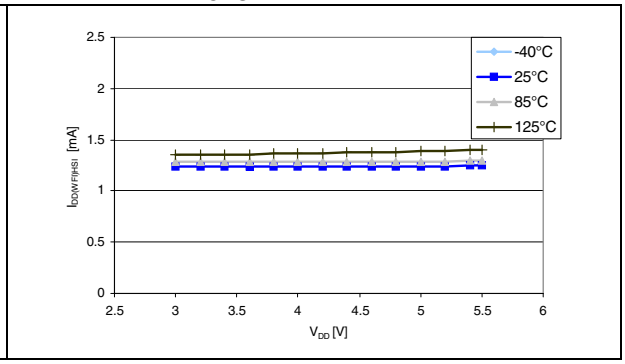


Figure 16. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz



7.3.2 External clock sources and timing characteristics

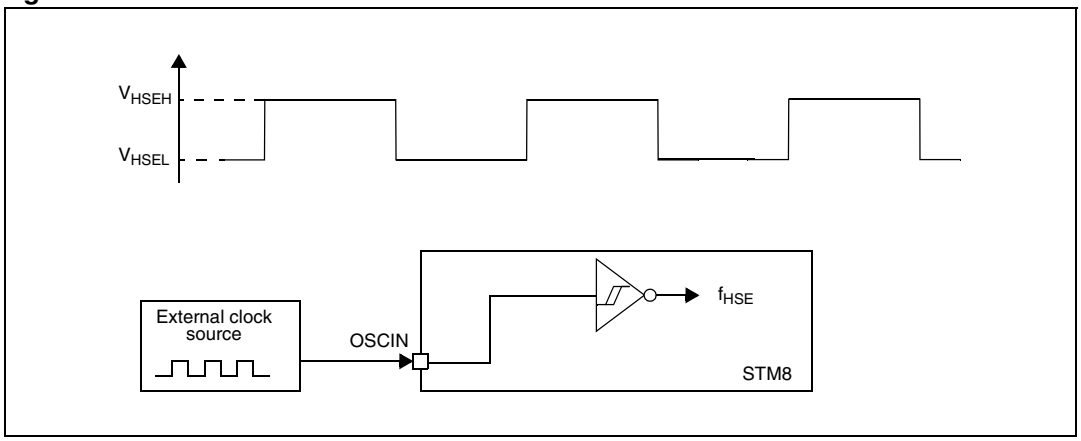
HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 18. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		0		24	MHz
V_{HSEH}	OSCIN input pin high level voltage		0.7 x V_{DD}		V_{DD}	V
V_{HSEL}	OSCIN input pin low level voltage		V_{SS}		0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1		+1	µA

Figure 17. HSE external clock source



HSE crystal/ceramic resonator oscillator

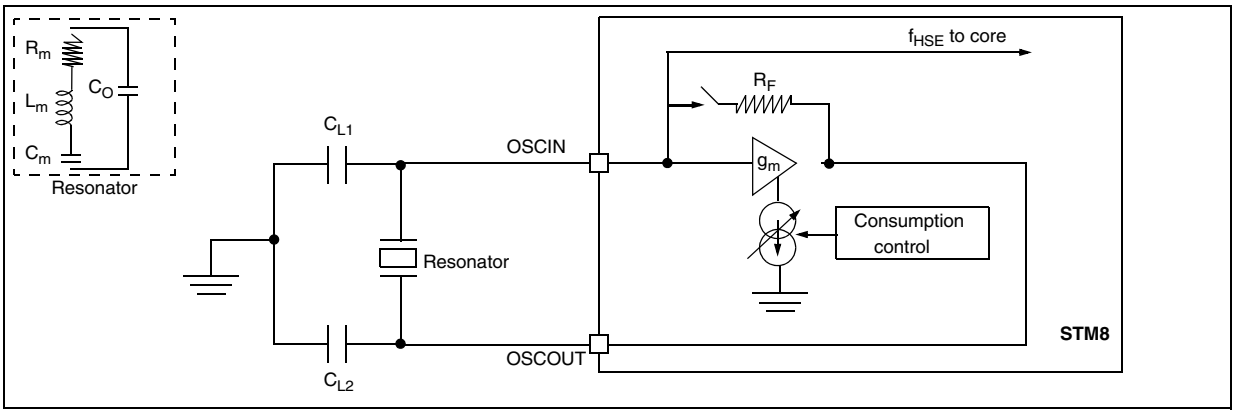
The HSE clock can be supplied with a 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 19. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor			220		kΩ
C(1)	Recommended load capacitance (2)				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF			6 (startup) 2 (stabilized)	mA
		C = 10 pF			6 (startup) 1.5 (stabilized)	
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}$ (3)	Startup time	V_{DD} is stabilized		1		ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
g_m >> g_{mcrit}

7.3.3 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

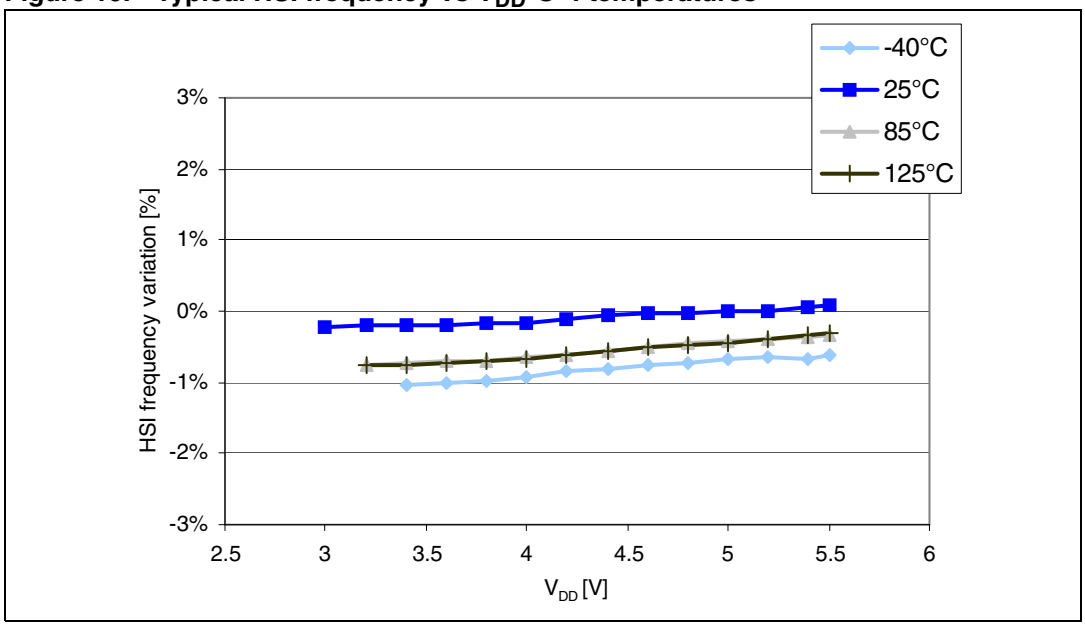
High speed internal RC oscillator (HSI)

Table 20. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HSI}	Accuracy of HSI oscillator	Trimmed by the application for given V_{DD} and T_A conditions	-1(2)		1(2)	%
	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 5.0 V, T_A = 25°C	-2		2	%
		V_{DD} = 5.0 V, 25 °C ≤ T_A ≤ 85 °C	TBD		TBD	%
		V_{DD} = 5.0 V, 25 °C ≤ T_A ≤ 125 °C	TBD		TBD	%
		V_{DD} = 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C	TBD(3)		TBD(3)	%
$t_{su(HSI)}$	HSI oscillator wake-up time including calibration			1	TBD(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			170	250(3)	µA

1. TBD = to be determined.
2. Guaranteeed by design. not tested in production.
3. Data based on characterization results, not tested in production

Figure 19. Typical HSI frequency vs V_{DD} @ 4 temperatures



Low speed internal RC oscillator (LSI)

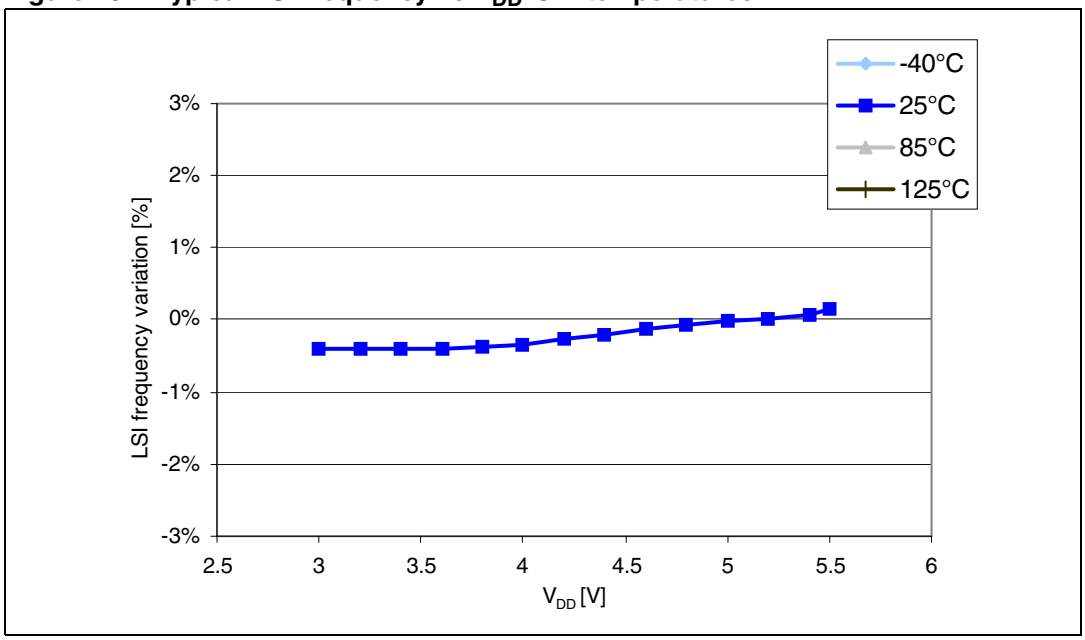
Subject to general operating conditions for V_{DD} and T_A.

Table 21. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency		TBD	128	TBD	kHz
$t_{su(LSI)}$	LSI oscillator wake-up time			7	TBD(2)	µs
$I_{DD(LSI)}$	LSI oscillator power consumption			5	TBD(2)	µA

1. TBD = to be determined.
2. Data based on characterization results, not tested in production.

Figure 20. Typical LSI frequency vs V_{DD} @ 4 temperatures



7.3.4 Memory characteristics

RAM and hardware registers

Table 22. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}			V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production. refer to *Table 12 on page 38* for the value of V_{IT-max}

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 125 °C.

Table 23. Flash program memory/data EEPROM memory(1)

Symbol	Parameter	Conditions	Min(2)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	$f_{CPU} \leq 24$ MHz	3.0		5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)			6	6.6	ms
	Fast programming time for 1 block (128 bytes)			3	3.3	ms
t_{erase}	Erase time for 1 block (128 bytes)			3	3.3	ms
N_{RW}	Erase/write cycles(3) (program memory)	T_A = +85 °C	10k			cycles
	Erase/write cycles (data memory)(3)	T_A = +125 °C	300k	1M		
t_{RET}	Data retention (program memory) after 10k erase/write cycles at T_A = +55 °C	T_{RET}=55°C	20			years
	Data retention (data memory) after 300k erase/write cycles at T_A = +125 °C	T_{RET}=85°C	1			
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 bytes)	V_{DD} = 3.3 V		TBD	TBD	mA
		V_{DD} = 5.0 V		TBD	TBD	

1. TBD = to be determined.
2. Guaranteed by characterization, not tested in production.
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

7.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 24. I/O static characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5.0 V	-0.3 V		TBD	V
V_{IH}	Input high level voltage		0.7 x V_{DD}		V_{DD} + 0.3 V	V
V_{hys}	Hysteresis(2)			700		mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN}=V_{SS}	30	45	60	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF			20 (3)	ns
		Standard and high sink I/Os Load = 50 pF			125 (3)	ns
I_{lkg}	Input leakage current, analog and digital	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1 (3)	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±250 (3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O(3)	Injection current ±4 mA			±1(3)	µA

1. TBD = to be determined.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 21. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

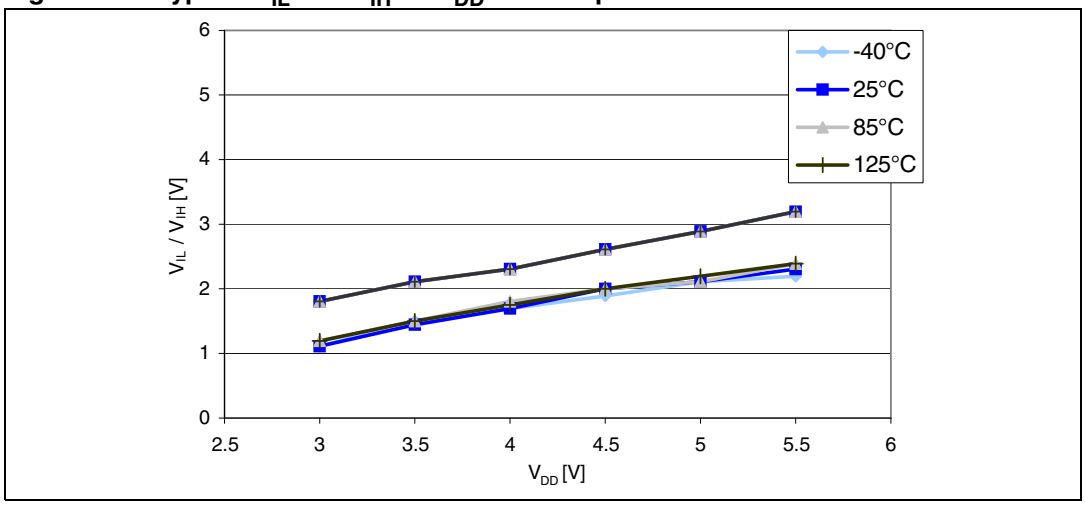


Figure 22. Typical pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

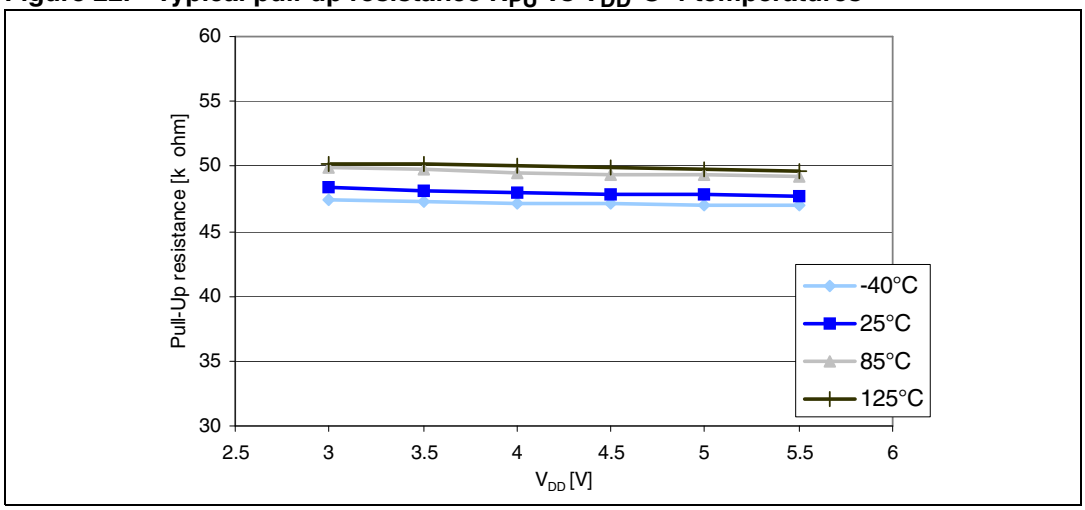
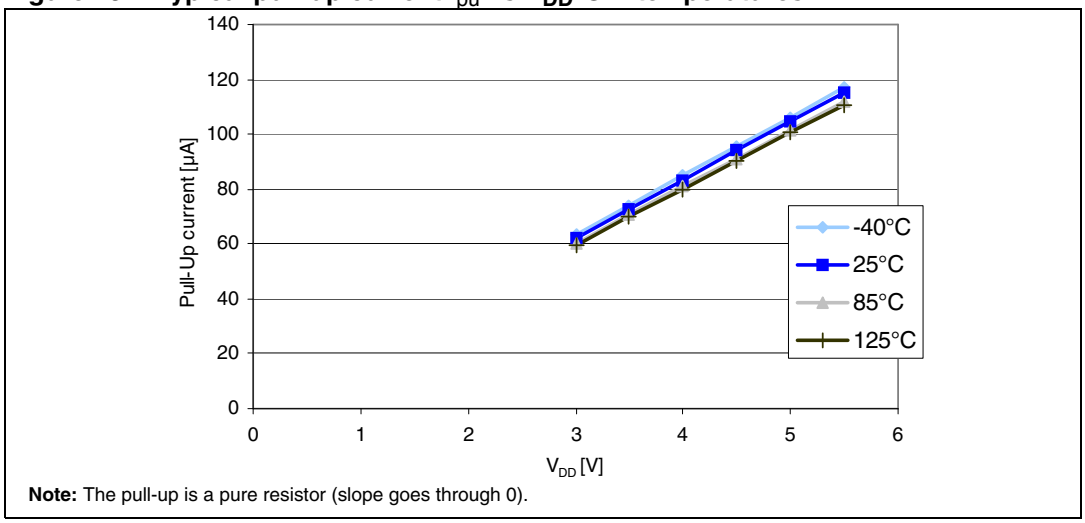


Figure 23. Typical pull-up current I_{pu} vs V_{DD} @ 4 temperatures



Note: The pull-up is a pure resistor (slope goes through 0).

Table 25. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 4 pins sunk	I_{IO} = 4 mA,V_{DD} = 3.3 V		1000(1)	mV
	Output low level with 8 pins sunk	I_{IO}= 10 mA,V_{DD} = 5.0 V		2000	
V_{OH}	Output high level with 4 pins sourced	I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)		V
	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5.0 V	2.8		

1. Data based on characterization results, not tested in production

Table 26. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V		1500(1)	mV
		I_{IO} = 10 mA, V_{DD} = 5.0 V		1000	
		I_{IO} = 20 mA, V_{DD} = 5.0 V		TBD(1)	

1. Data based on characterization results, not tested in production

Table 27. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 4 pins sunk	I_{IO} = 10 mA,V_{DD} = 3.3 V		1000(1)	mV
	Output low level with 8 pins sunk	I_{IO} = 10 mA,V_{DD} = 5.0 V		800	
	Output low level with 4 pins sunk	I_{IO} = 20 mA,V_{DD} = 5.0 V		1500(1)	
V_{OH}	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)		V
	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5.0 V	4.0		
	Output high level with 4 pins sourced	I_{IO} = 20 mA, V_{DD} = 5.0 V	3.3(1)		

1. Data based on characterization results, not tested in production

Typical output level curves

Figure 24 to *Figure 33* show typical output level curves measured with output on a single pin.

Figure 24. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

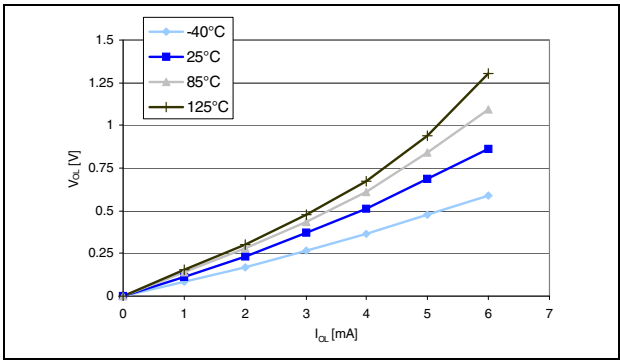


Figure 25. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

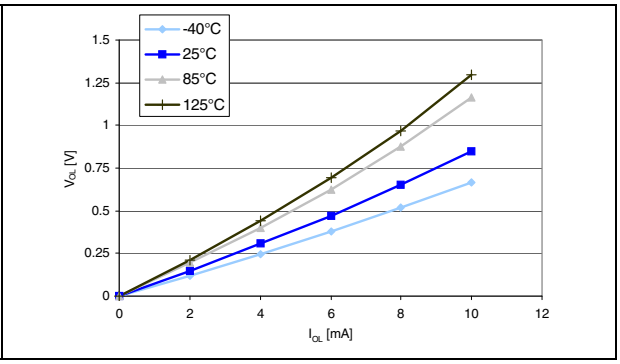


Figure 26. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

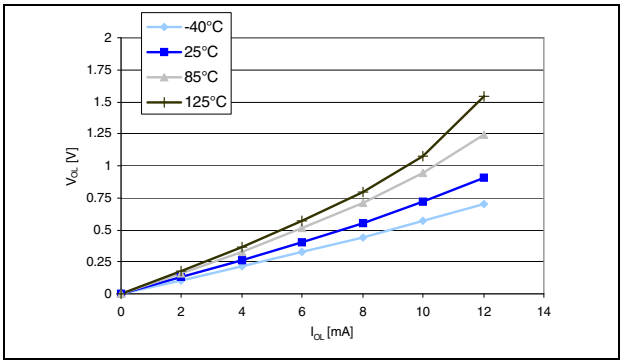


Figure 27. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

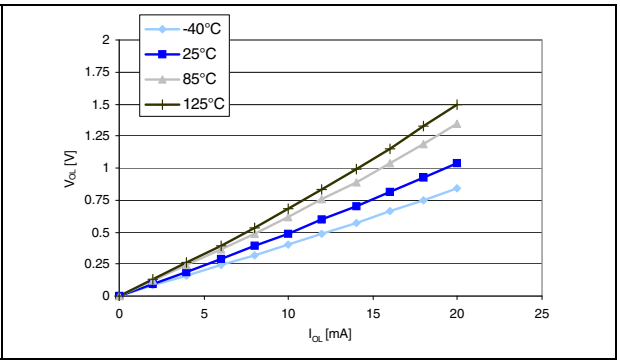


Figure 28. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

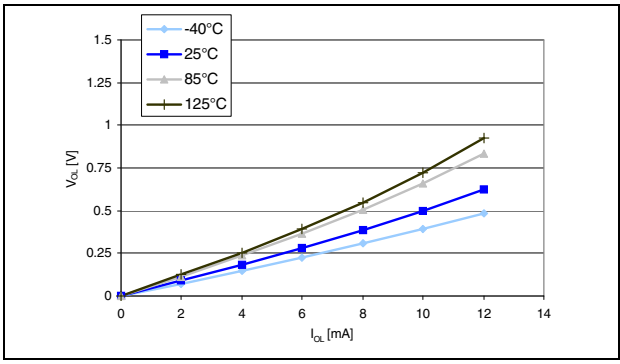


Figure 29. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

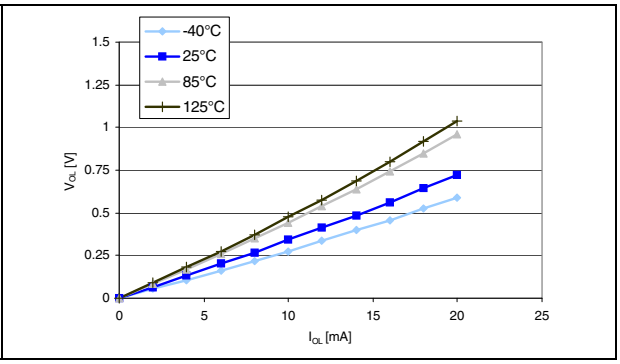


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

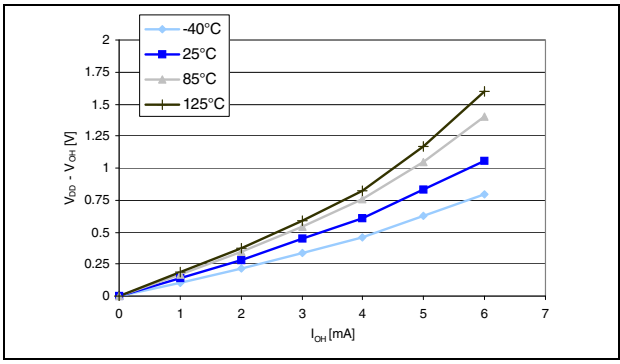


Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

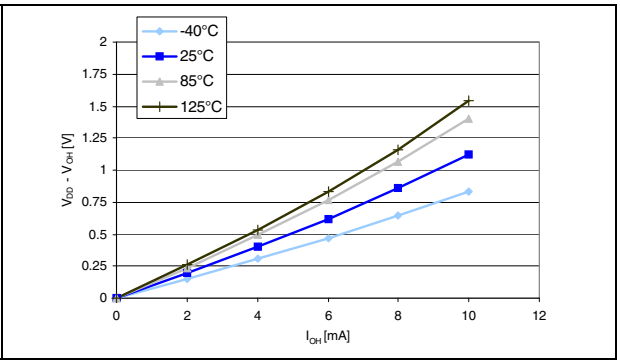


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

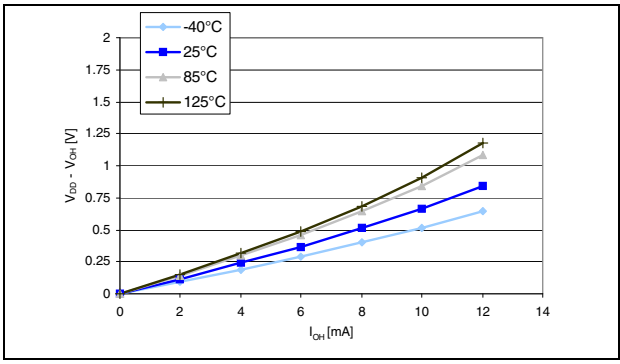
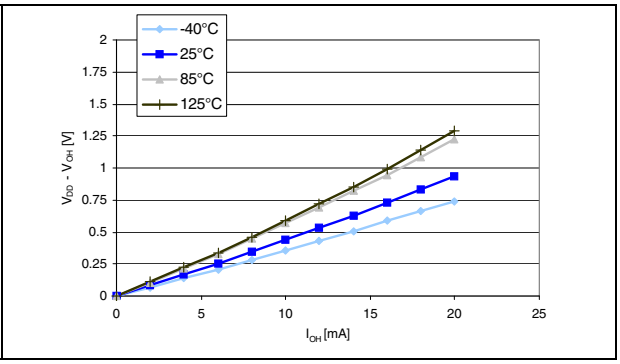


Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



7.3.6 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 28. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ 1)	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage (2)		V_{SS}		TBD	V
$V_{IH(NRST)}$	NRST Input high level voltage (2)		TBD		V_{DD}	
$V_{OL(NRST)}$	NRST Output low level voltage (2)	I_{OL}=TBD mA			TBD	
$R_{PU(NRST)}$	NRST Pull-up resistor (3)		30	40	60	kΩ
$V_{F(NRST)}$	NRST Input filtered pulse (4)			TBD		ns
$V_{NF(NRST)}$	NRST Input not filtered pulse (4)			TBD		µs

1. TBD = to be determined.
2. Data based on characterization results, not tested in production.
3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
4. Data guaranteed by design, not tested in production.

Figure 34. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

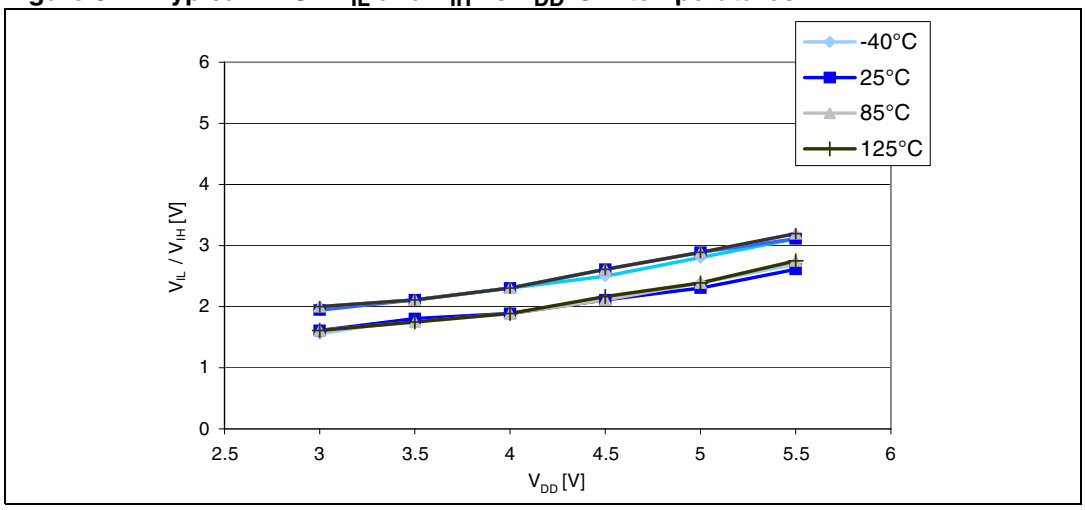


Figure 35. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

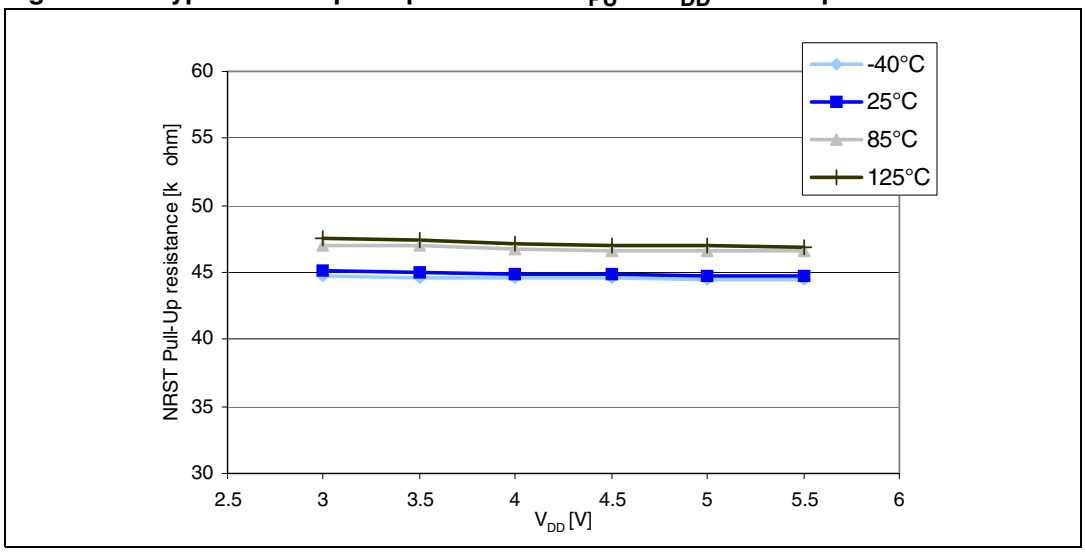
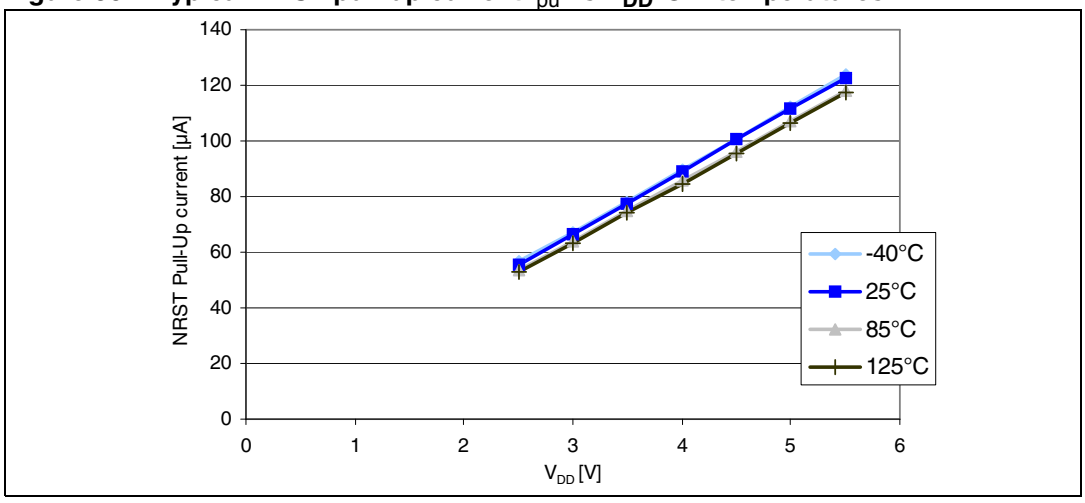
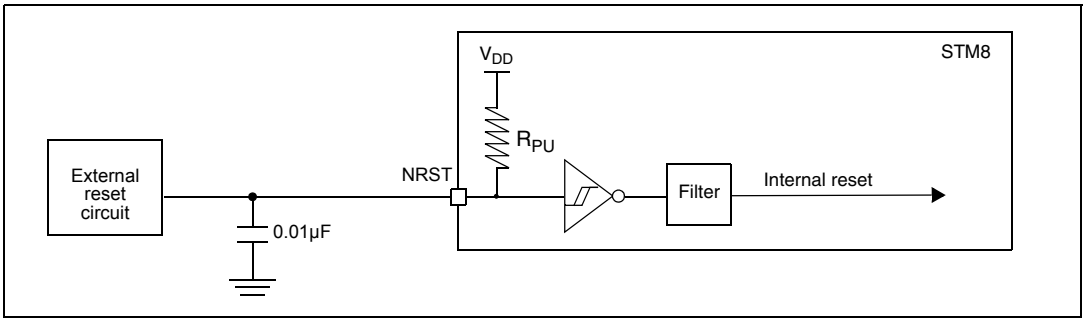


Figure 36. Typical NRST pull-up current I_{pu} vs V_{DD} @ 4 temperatures



The reset network shown in *Figure 37* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 24*. Otherwise the reset is not taken into account internally.

Figure 37. Recommended reset pin protection



7.3.7 TIM timer characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 29. TIM 1, 2, 3 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time(1)		2			t_{MASTER}
$t_{res(TIM)}$	Timer resolution time(1)		1			t_{MASTER}
f_{EXT}	Timer external clock frequency(1)				24	MHz
Res_{TIM}	Timer resolution(1)			16		bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected(1)			1		t_{MASTER}
t_{MAX_COUNT}	Maximum possible count(1)				65,536	t_{MASTER}

1. Guaranteed by design.

7.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 30* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 30. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	10	MHz
		Slave mode	0	10	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4*t_{MASTER}$		
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{MASTER} = 16 MHz, f_{SCK}= 8 MHz	110	140	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5		
		Slave mode	2		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode, f_{MASTER} = 16 MHz, f_{SCK}= 8 MHz	7		
		Slave mode, f_{MASTER} = 16 MHz, f_{SCK}= 8 MHz	3		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{MASTER} = 16 MHz, f_{SCK}= 8 MHz		400	
		Slave mode		$4*t_{MASTER}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge), f_{MASTER} = 16 MHz, f_{SCK}= 8 MHz		100	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge), f_{MASTER} = 16 MHz, f_{SCK}= 8 MHz		3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	100		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	6		

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 38. SPI timing diagram - slave mode and CPHA=0

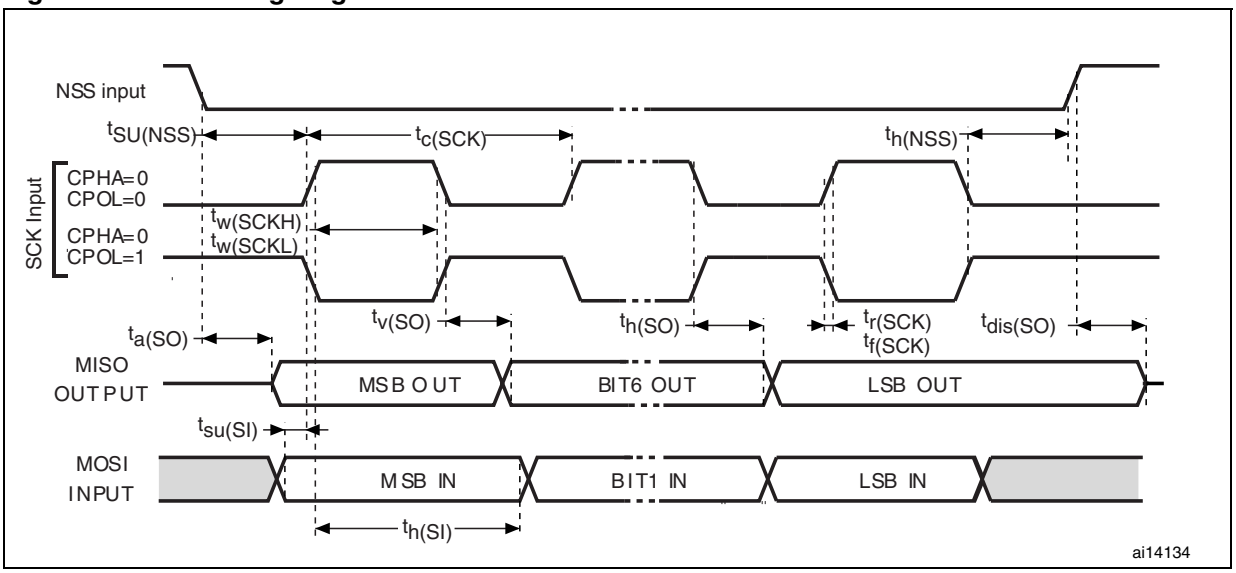
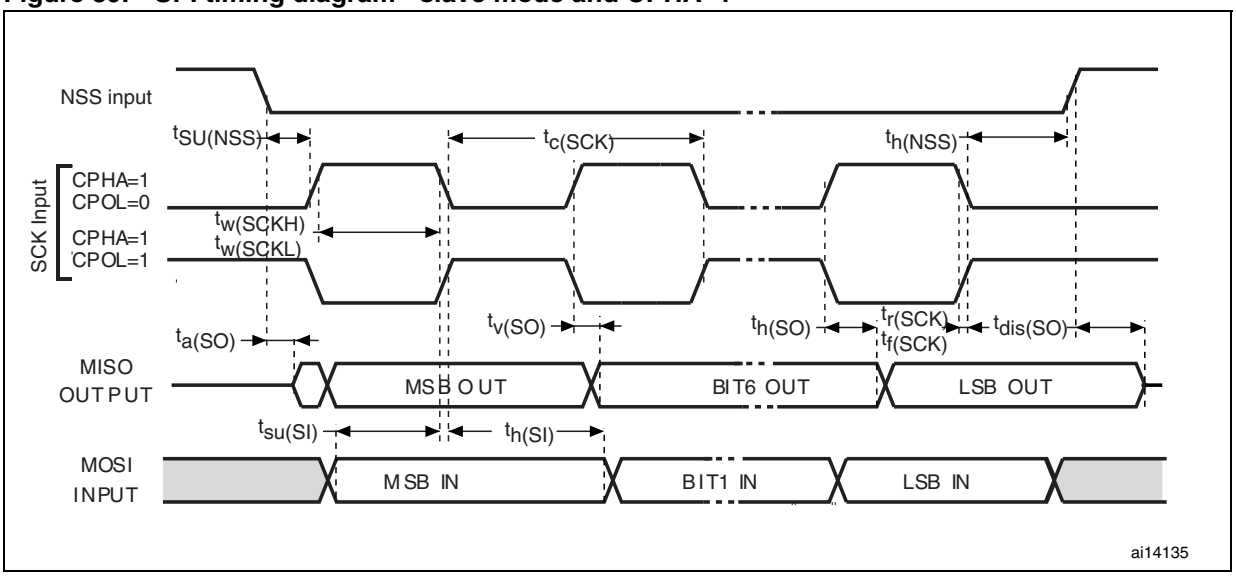
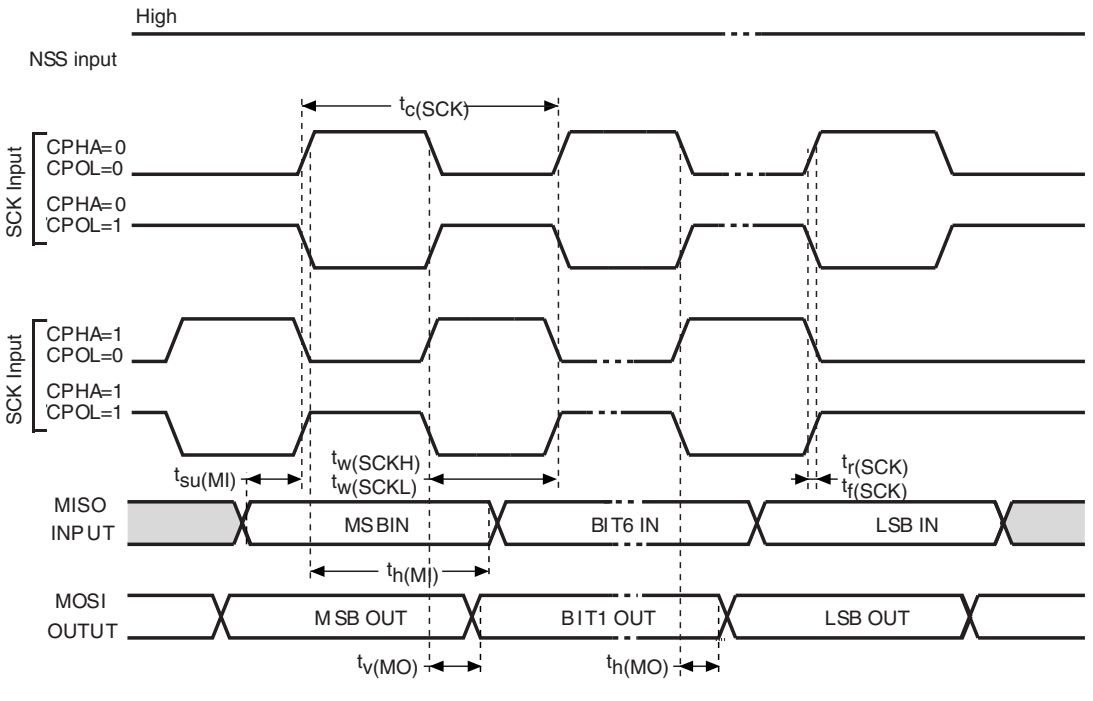


Figure 39. SPI timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 40. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

7.3.9 I2C interface characteristics

Table 31. I^2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I^2C speed (400kHz)
2. Data based on standard I^2C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

7.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 32. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DDA} = 3 to 5.5 V	1		4	MHz
		V_{DDA} = 4.5 to 5.5 V	1		6	
V_{DDA}	Analog supply		3		5.5	V
V_{REF+}	Positive reference voltage		2.75		V_{DDA}	V
V_{REF-}	Negative reference voltage		V_{SSA}		0.5	V
V_{AIN}	Conversion voltage range(1)		V_{SSA}		V_{DDA}	V
		Devices with external V_{REF+}/ V_{REF-} pins	V_{REF-}		V_{REF+}	V
C_{ADC}	Internal sample and hold capacitor			3		pF
t_S(1)	Minimum sampling time	f_{ADC} = 4 MHz		0.75		µs
		f_{ADC} = 6 MHz		0.5		
t_{STAB}	Wake-up time from standby			7		µs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz	3.5			µs
		f_{ADC} = 6 MHz	2.33			µs
			14			$1/f_{ADC}$

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 33. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DDA} = 3.3 V(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 3 MHz.	1.5	TBD	LSB
		f_{ADC} = 4 MHz.	2.2	TBD	
$\|E_O\|$	Offset error(2)	f_{ADC} = 3 MHz.	1.1	TBD	
		f_{ADC} = 4 MHz.	1.4	TBD	
$\|E_G\|$	Gain error(2)	f_{ADC} = 3 MHz.	-0.2/0.6	TBD	
		f_{ADC} = 4 MHz.	-0.1/1.1	TBD	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 3 MHz.	0.9	TBD	
		f_{ADC} = 4 MHz.	0.9	TBD	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 3 MHz.	1	TBD	
		f_{ADC} = 4 MHz.	1	TBD	

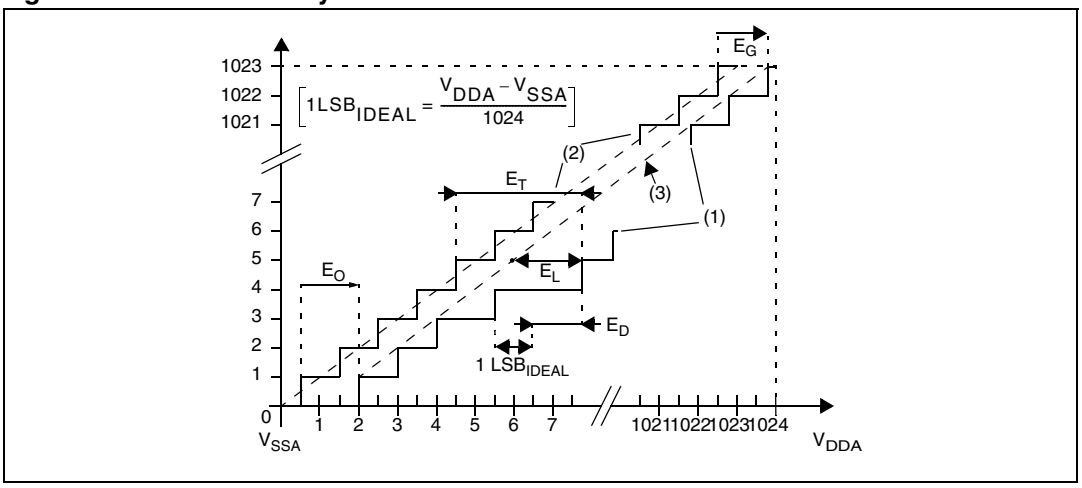
1. TBD = to be determined.

Table 34. ADC accuracy with R_{AIN} < 10 kΩ , V_{DDA} = 5 V(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error (2)	f_{ADC} = 2 MHz.	1	TBD	LSB
		f_{ADC} = 4 MHz.	1.7	TBD	
		f_{ADC} = 6 MHz.	2.2	TBD	
$\|E_O\|$	Offset error (2)	f_{ADC} = 2 MHz.	0.7	TBD	
		f_{ADC} = 4 MHz.	1	TBD	
		f_{ADC} = 6 MHz.	1.8	TBD	
$\|E_G\|$	Gain error (2)	f_{ADC} = 2 MHz.	-0.03	TBD	
		f_{ADC} = 4 MHz.	0.6	TBD	
		f_{ADC} = 6 MHz.	1.3	TBD	
$\|E_D\|$	Differential linearity error (2)	f_{ADC} = 2 MHz.	0.8	TBD	
		f_{ADC} = 4 MHz.	0.9	TBD	
		f_{ADC} = 6 MHz.	0.9	TBD	
$\|E_L\|$	Integral linearity error (2)	f_{ADC} = 2 MHz.	0.6	TBD	
		f_{ADC} = 4 MHz.	0.8	TBD	
		f_{ADC} = 6 MHz.	0.8	TBD	

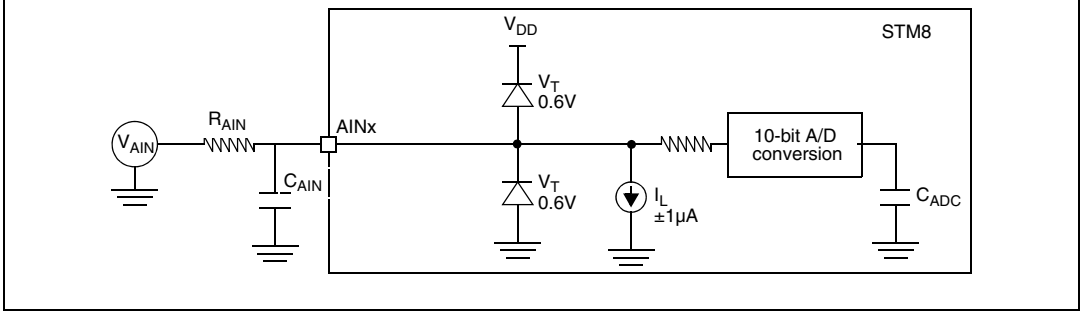
1. TBD = to be determined.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 7.3.5* does not affect the ADC accuracy.

Figure 41. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical application with ADC



7.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 35. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A=+25 °C, f_{MASTER} = 16 MHz (HSI clock), conforms to IEC 1000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A=+25 °C, f_{MASTER} = 16 MHz (HSI clock) conforms to IEC 1000-4-4	4A

Electromagnetic interference (EMI)

Emission tests conform to the SAE J 1752/3 standard for test software, board layout and pin loading.

Table 36. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)			
				8 MHz	16 MHz	24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = +25 °C, LQFP80 package conforming to SAE J 1752/3	0.1MHz to 30 MHz	15	17	22	dBµV
			30 MHz to 130 MHz	18	22	16	
			130 MHz to 1 GHz	-1	3	5	
	SAE EMI level			2	2.5	2.5	-

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 37. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = +25°C, conforming to JESD22-A114	A	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A=+25°C, conforming to JESD22-C101	IV	1000	V

1. Data based on characterization results, not tested in production

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 38. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = +25 °C	A
		T_A = +85 °C	A
		T_A = +125 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

7.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 11: General operating conditions on page 37*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 39. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 44 - 10 x 10 mm	54	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W
Θ_{JA}	Thermal resistance junction-ambient VFQFN 32 - 5 x 5 mm	21.6	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

7.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 50: STM8S207/208xx performance line ordering information scheme on page 79*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2), I_{DDmax} = 8 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

$$P_{INTmax} = 8 \text{ mA} \times 5 \text{ V} = 400 \text{ mW}$$

$$P_{IOmax} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} = 64 \text{ mW}$$

This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:

$$P_{Dmax} = 400 \text{ mW} + 64 \text{ mW}$$

Thus: P_{Dmax} = 464 mW

Using the values obtained in *Table 39: Thermal characteristics on page 67* T_{Jmax} is calculated as follows:

– For LQFP64 46°C/W

$$T_{Jmax} = 82° \text{ C} + (46° \text{ C/W} \times 464 \text{ mW}) = 82°\text{C} + 21°\text{C} = 103° \text{ C}$$

This is within the range of the suffix 6 version parts (-40 < T_J < 105° C).

In this case, parts must be ordered at least with the temperature range suffix 6.

8 Package characteristics

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at *www.st.com*.

8.1 Package mechanical data

8.1.1 LQFP package mechanical data

Figure 43. 80-pin low profile quad flat package (14 x 14)

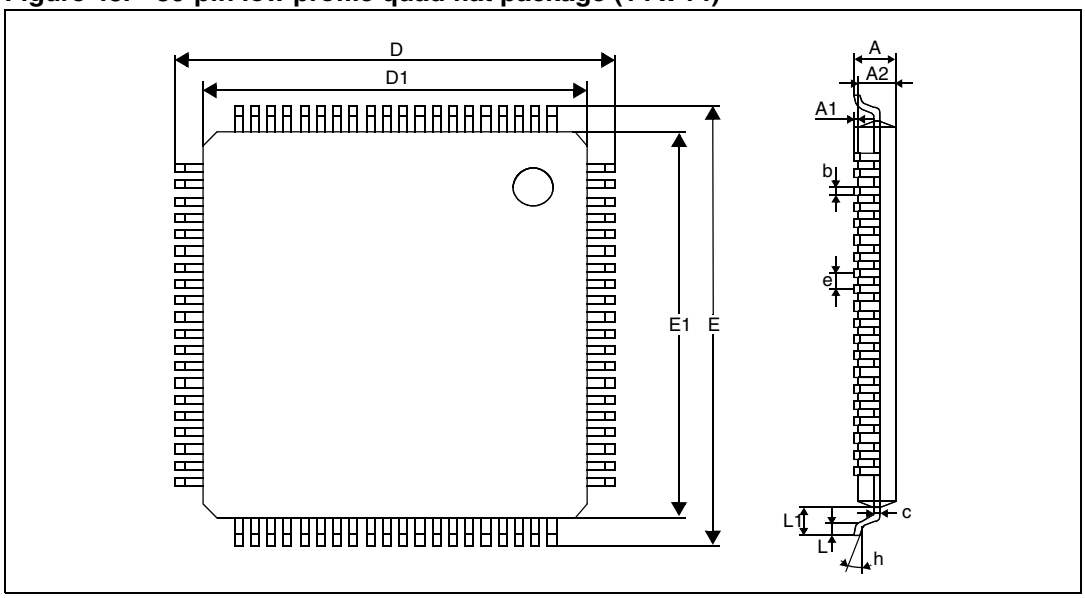


Table 40. 80-pin low profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.22	0.32	0.38	0.0087	0.0126	0.0150
C	0.09		0.20	0.0035		0.0079
D		16.00			0.6299	
D1		14.00			0.5512	
E		16.00			0.6299	
E1		14.00			0.5512	
e		0.65			0.0256	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 44. 64-pin low profile quad flat package (10 x 10)

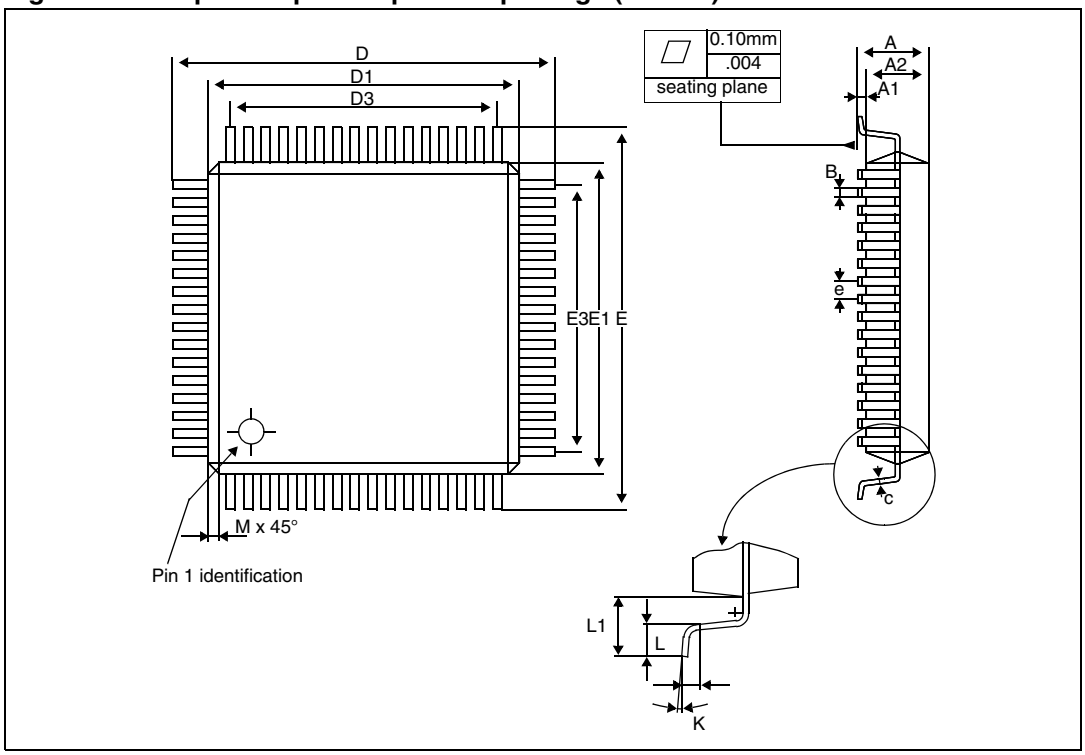


Table 41. 64-pin low profile quad flat package mechanical data (10 x 10)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 45. 64-pin low profile quad flat package (14 x14)

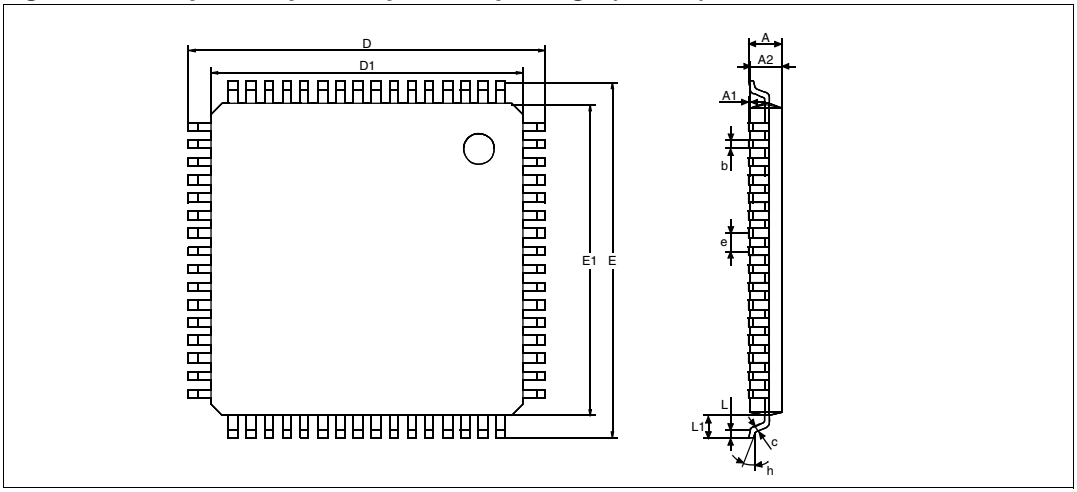


Table 42. 64-pin low profile quad flat package mechanical data (14 x14)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.012	0.015	0.018
c	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.80			0.031	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64					

1. Values in inches are converted from mm and rounded to 3 decimal digits

Figure 46. 48-pin low profile quad flat package (7 x 7)

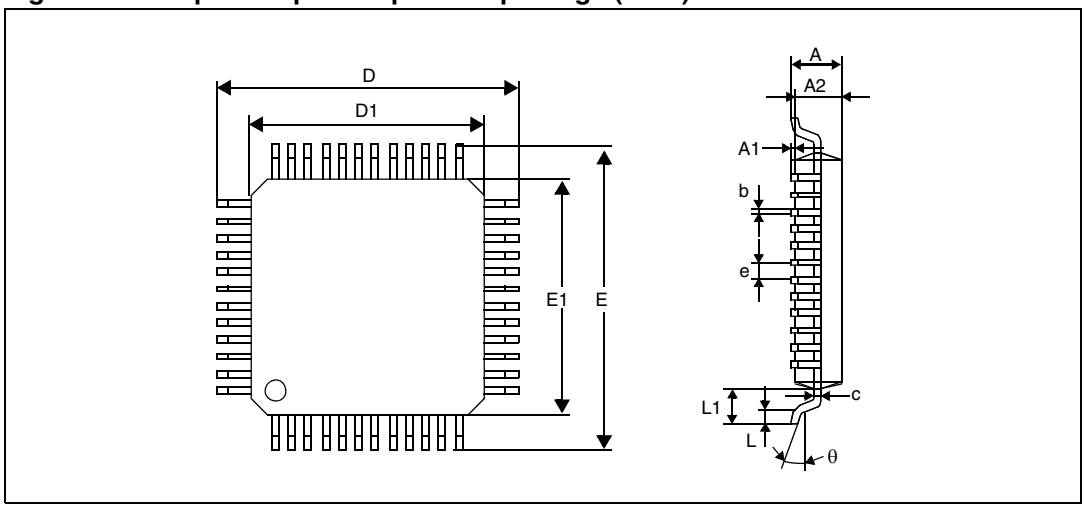


Table 43. 48-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.50			0.0197	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 47. 44-pin low profile quad flat package (10 x 10)

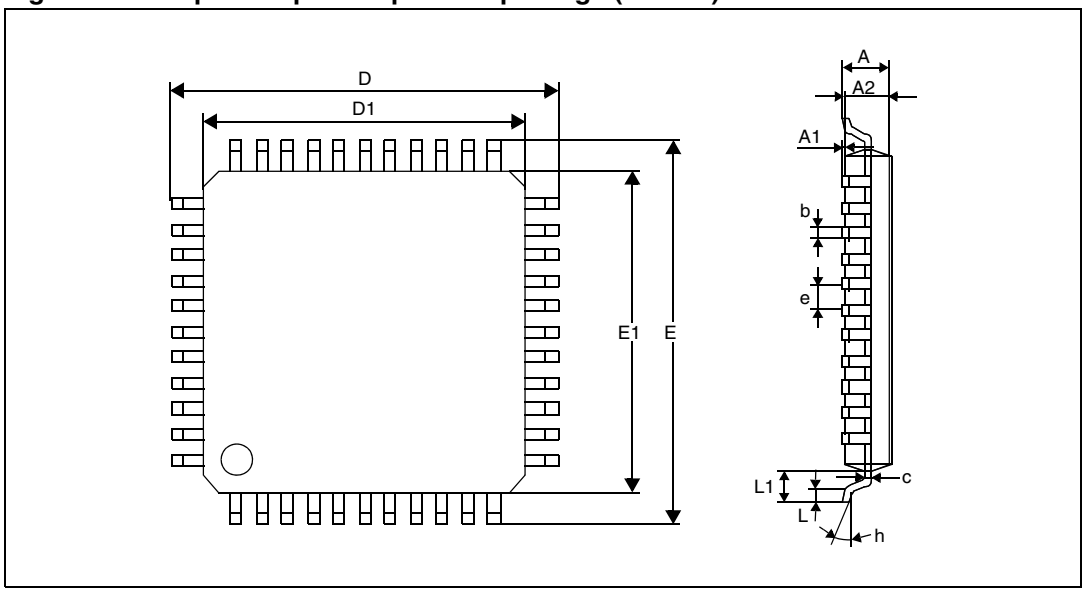


Table 44. 44-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.80			0.0315	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 48. 32-pin low profile quad flat package (7 x 7)

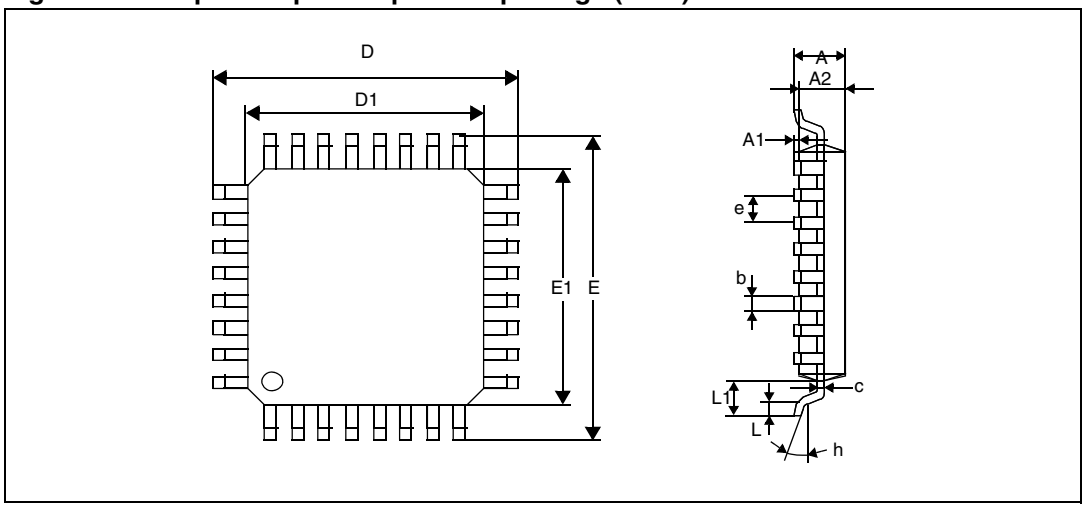


Table 45. 32-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.80			0.0315	
q	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

8.1.2 QFN package mechanical data

Figure 49. 32-lead very thin fine pitch quad flat no-lead package (5 x 5)

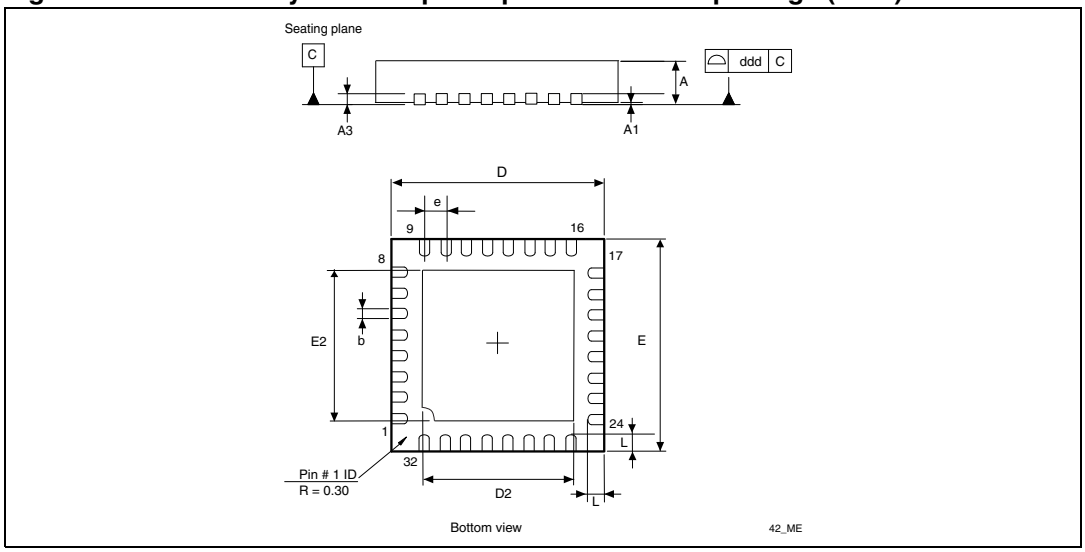


Table 46. 32-lead very thin fine pitch quad flat no-lead package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05		0.0008	0.0020
A3		0.20			0.0079	
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D	4.85	5.00	5.15	0.1909	0.1969	0.2028
D2	3.20	3.45	3.70	0.1260		0.1457
E	4.85	5.00	5.15	0.1909	0.1969	0.2028
E2	3.20	3.45	3.70	0.1260	0.1358	0.1457
e		0.50			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd			0.08			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits

1. TBD = to be determined.

9 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

9.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the full-featured STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 K records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8

9.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the cosmic C compiler for STM8, which is available in a free version that outputs up to 16 Kbytes of code.

9.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com/mcu. This package includes:

ST visual develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8 microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

9.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

- **Cosmic C compiler for STM8** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.
- **Raisonance C compiler for STM8** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.raisonance.com.
- **ST7/STM8 assembler linker** – Free assembly toolchain included in the STVD toolset, which allows you to assemble and link your application source code.

9.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on your application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming your STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

10 Ordering information

Figure 50. STM8S207/208xx performance line ordering information scheme

Example: STM8 S 208 M B T 6 B

Product class
STM8 microcontroller

Family type
S = Standard

Sub-family type
208 = full peripheral set
207 = intermediate peripheral set

Pin count
K = 32 pins
S = 44 pins
C = 48 pins
R = 64 pins
M = 80 pins

Program memory size
4 = 16K
6 = 32K
8 = 64K
B = 128K

Package type
T = LQFP
U = VFQFPN

Temperature range
3 = -40 °C to 125 °C
6 = -40 °C to 85 °C

Package pitch
no character = 0.5 mm
B = 0.65 mm
C = 0.8 mm

Packing
no character = tray or tube
TR = tape and reel

For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to www.st.com or contact the ST Sales Office nearest to you.

11 Revision history

Table 47. Document revision history

Date	Revision	Changes
23-May-2008	1	Initial release.
05-Jun-2008	2	Added part numbers on page 1 and in *Table 2 on page 10*. Updated *Section 4: Product overview* Updated *Section 7: Electrical characteristics*
22-Jun-2008	3	Added part numbers on page 1 and in *Table 2 on page 10*.
12-Aug-2008	4	Added 32 pin device pinout and ordering information. Updated UBC option description in *Table 7 on page 32* USART renamed UART1, LINUART renamed UART3. Max. ADC frequency increased to 6 MHz.

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