PLL Frequency Synthesizer

ADF4108S

1.0. SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aeroinfo

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/ADF4108.

2.0. Part Number: The complete part number(s) of this specification follows:

Part Number	Description
ADF4108L703F	Radiation tested to 50Krads, 1 to 7 GHz PLL Frequency Synthesizer

3.0. Case Outline

The case outline(s) are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP4-F16	16 lead	Bottom Brazed Flat Pack

Package: F			
Pin Number	Terminal Symbol	Pin Type	Pin Description
1	Rset	Analog Input	Bias for charge pump. Connecting a resistor between this pin and CPGND set the maximum charge pump current to: Icp max = 25.5 / Rset. The nominal output voltage is 0.66V
2	CP	Analog Output	Charge Pump Output. When enabled, this pin provides ±Icp to the external loop filter, which in turn drives the external VCO.
3	CPGND	Ground	Charge Pump Ground. Connect to low impedance ground.
4	AGND	Ground	Analog Ground. Connect to low impedance ground.
5	RFinB	Analog Input	Complementary Input to the RF Prescaler. This pin must be decoupled to ground plane with a small bypass capacitor, typically 100pF.
6	RFinA	Analog Input	Input to the RF Prescaler. This pin must be ac-coupled to external VCO.
7	AVdd	Power	Analog supply voltage. 3.2V to 3.6V. AVdd and DVdd should be tied together externally and properly bypassed.
8	REFin	Analog Input	Reference Input. This is a CMOS input with a nominal threshold of Vdd/2 and a equivalent input resistance of 100kΩ.
9	DGND	Ground	Digital Ground. Connect to low impedance ground.
10	CE	Digital Input	Chip Enable. High impedance CMOS input. A logic low on this pin powers down the part and puts the charge pump output into three-state mode.
11	CLK	Digital Input	Serial Clock input. High impedance CMOS input. Used to clock in serial data to registers.
12	DATA	Digital Input	Serial Data Input. High impedance CMOS input. Data loaded MSB first with the 2 LSBs being the control bits.
13	LE	Digital Input	Load Enable. High impedance CMOS input. When LE rises, shift register data is loaded into one of four latches selected using the control bits.
14	MUXOUT	Digital Output	Muxtiplexer Output. Allows either lock detect, or frequency divided RF or REF to accessed externally.
15	DVdd	Power	Digital Supply Voltage. 3.2V to 3.6V. AVdd and DVdd should be tied together externally and properly bypassed.
16	Vp	Power	Charge Pump Power Supply. Must be greater than or equal to Vdd and less than 5.5V.

Figure 1 - Terminal connections.

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4.0. Specifications

4.1. Absolute maximum ratings 1/

AVdd to GND .....-0.3V to +3.9 V
AVdd to DVdd.....-0.3V to +0.3 V
Vp to GND .....-0.3V to +5.8 V
Vp to AVdd.....-0.3V to +5.8 V
Digital I/O Voltage to GND .....-0.3V to Vdd + 0.3 V
Analog I/O Voltage to GND .....-0.3V to Vp +0.3 V
REFin, RFinA, RFinB to GND .....-0.3V to Vdd +0.3 V
RFinA to RFinB ..... +/- 600 mV
Operating Temperature Range .....-55 ºC to +125 ºC
Storage Temperature Range..... –65°C to +150 °C
Maximum Junction Temperature (T_J).....150 °C
Lead Temperature (Soldering 60 Sec).....+300 °C
Thermal resistance, junction-to-case (θ_{JC}).....31 °C/W 2/
Thermal resistance, junction-to-ambient (θ_{JA}).....36 °C/W 2/

4.2. Recommended operating conditions

AVdd = DVdd .....3.2 V to 3.6 V
Vp .....Vdd to 5.5 V
Ambient Operating Temperature Range ..... -55 ºC to +125 ºC

4.3. Nominal operating performance characteristics (TA = 25°C, AV_{DD} = DV_{DD} = 3.3V, GND = AGND = DGND = CPGND = 0V, V_{CP} = 5V, R_{SET} = 5.1kΩ, RFinB cap coupled to ground, unless otherwise noted)

RF Frequency..... 1.0 GHz to 7.0 GHz
REF Frequency..... 20 MHz to 250 MHz

Phase Detector
Max sampling Frequency ..... 104 MHz

Logic In
Max Input Capacitance ..... 10 pF

REFin
Max Input Capacitance ..... 10 pF

Noise Characteristics
Normalized Phase Noise Floor (PN_{SYNTH})..... -223 dBc/Hz 3/
Normalized 1/f Noise (PN1_f) ..... -122 dBc/Hz 4/
Phase Noise Performance 7900 MHz Output..... -81 dBc/Hz 5/
Spurious Signals 7900 MHz Output..... -82 dBc 5/

NOTES

1/ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2/ Measurement taken under absolute worst case condition and represents data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package Theta JC numbers.

3/ PLL loop B/W = 500 kHz, measured at 100 kHz offset. The synthesizers phase noise is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10log F_{PFD}. So PN_{SYNTH} = PN_{TOT} – 10 log F_{PFD} - 20 log N.
4/ 10 kHz offset; normalized to 1 GHz. The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF} and at a frequency offset, f, is given by PN = PN1_f + 10 log(10 kHz/f) – 10log(f_{RF}/ 1GHz).

5/ At VCO output and 1 kHz offset. f_{REFIN} = 10MHz, f_{PFD} = 1MHz, f_{RF} = 7900MHz, N = 7900; Loop B/W = 30kHZ, VCO = ZComm CRO8000Z with +10 dB RF Amp so that the PLL RFin = +5dBm.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub-Group	Limit Min	Limit Max	Units
RFin Charateristics, pin RFinA, RFinB						
RFin Input Frequency	RFfreq	Tested at Vdd/Vcp = 3.6/3.6; 3.6/5.5; 3.2/3.2	4	1	5	GHz
			5,6	1	5	
		M,D,P,L	4	1	5	
RFin Input Frequency	RFfreq	2/	4	5	7	GHz
			5,6	5	7	
RFin Input Sensitivity	RFlvl		4	-5	5	dBm
			5,6	-5	5	
		M,D,P,L	4	-5	5	
Maximum Allowable Prescaler Output Frequency	Fpresc	3/ PreScaler = 8, Tested at Vdd/Vcp = 3.6/5.5; 3.2/3.2	4		300	MHz
			5,6		300	
		M,D,P,L	4		300	
REFin Charateristics, pin REFin						
REFin Input Frequency	REFfreq		4	20	250	MHz
			5,6	20	250	
		M,D,P,L	4	20	250	
REFin Input Sensitivity	REFlvl	AC coupling ensures bias = $AV_{DD/2}$	4	0.8	V_{DD}	Vp-p
			5,6	0.8	V_{DD}	
		M,D,P,L	4	0.8	V_{DD}	
REFin Input High/Low Current	REF_Iin		4	-100	100	µA
			5,6	-100	100	
		M,D,P,L	4	-100	100	
Charge Pump, pin CP						
Icp Sink/Source High Value	$I_{cp}8$	With Rset = 5.1KΩ	1	2.5	7.5	mA
			2,3	2.5	7.5	
		M,D,P,L	1	2.5	7.5	
Icp Sink/Source Low Value	$I_{cp}1$	With Rset = 5.1KΩ	1	0.125	1.250	mA
			2,3	0.125	1.250	
		M,D,P,L	1	0.125	1.250	
Icp Sink/Source Absolute Accuracy	$Icp8_{AbsAcc}$		1	-10	10	%
			2,3	-10	10	
		M,D,P,L	1	-10	10	
Icp Sink/Source Rset Range	$Rset_{Rng}$	2/	1	3.0	11.0	kΩ
			2,3	3.0	11.0	
Icp Three-State Leakage	I_{CP}_Ikg		1	-15	15	nA
			-2,3	-15	15	
		M,D,P,L	1	-20	20	

See footnotes at end of table.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub-Group	Limit Min	Limit Max	Units
Charge Pump – continued						
Icp Sink/Source Current matching	$I_{CP\_}m$	Icp1- Icp8, With Rset = 5.1KΩ,	1	-10	10	%
			2,3	-10	10	
		M,D,P,L	1	-10	10	
Icp Vs. Vcp	$I_{CP\_}V_{CP}$	With Rset = 5.1KΩ, $0.5\ v \le Vcp \le Vp - 0.5\ V$	1	-8	8	%
			2,3	-8	8	
		M,D,P,L	1	-8	8	
Icp Vs. temperature	$I_{CP\_}T$	2/ With Rset = 5.1KΩ, $Vcp = Vp / 2$	1	-5	5	%
			2,3	-5	5	
Rset Output Voltage	Vrset	With Rset = 5.1KΩ,	1	0.5	0.7	V
			2,3	0.5	0.7	
		M,D,P,L	1	0.5	0.7	
Logic Inputs, pins CE, LE, CLOCK, DATA						
Input High Voltage	V_{iH}		1	1.4	Vdd	V
			2,3	1.4	Vdd	
		M,D,P,L	1	1.4	Vdd	
Input Low Voltage	V_{iL}		1	0	0.6	V
			2,3	0	0.6	
		M,D,P,L	1	0	0.6	
Input High/Low Current	I_{InH} , I_{InL}	V of I_{InH} = 3.2 V, V of I_{InL} = 0.1 V	1	-1	1	µA
			2,3	-1	1	
		M,D,P,L	1	-1	1	
Logic Outputs, pin MUXOUT						
N-channel Output High Voltage	V_{OH}	1 kΩ pull-up resistor to 1.8V	1	1.4		V
			2,3	1.4		
		M,D,P,L	1	1.4		
CMOS Output High Voltage	V_{OH}	I_{OH} = 500µA	1	Vdd – 0.4		V
			2,3	Vdd – 0.4		
		M,D,P,L	1	Vdd – 0.4		
Output Low Voltage	V_{OL}	I_{OL} = 500µA	1		0.4	V
			2,3		0.4	
		M,D,P,L	1		0.4	
Output High/ Low Leakage Current	I_{OH} , I_{OL}	V of I_{OH} = 3.2 V, V of I_{OL} = 0.1 V, MUXOUT tri-stated	1	-100	100	µA
			2,3	-100	100	
		M,D,P,L	1	-100	100	

See footnotes at end of table.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub- Group	Limit Min	Limit Max	Units
Timing						
Data to Clock setup time	t_1		9	10		nS
			10,11	10		
		M,D,P,L	9	10		
Data to Clock hold time	t_2		9	10		nS
			10,11	10		
		M,D,P,L	9	10		
Clock high time	t_3		9	25		nS
			10,11	25		
		M,D,P,L	9	25		
Clock low time	t_4		9	25		nS
			10,11	25		
		M,D,P,L	9	25		
Data to LE setup time	t_5		9	10		nS
			10,11	10		
		M,D,P,L	9	10		
LE pulse width	t_6		9	20		nS
			10,11	20		
		M,D,P,L	9	20		

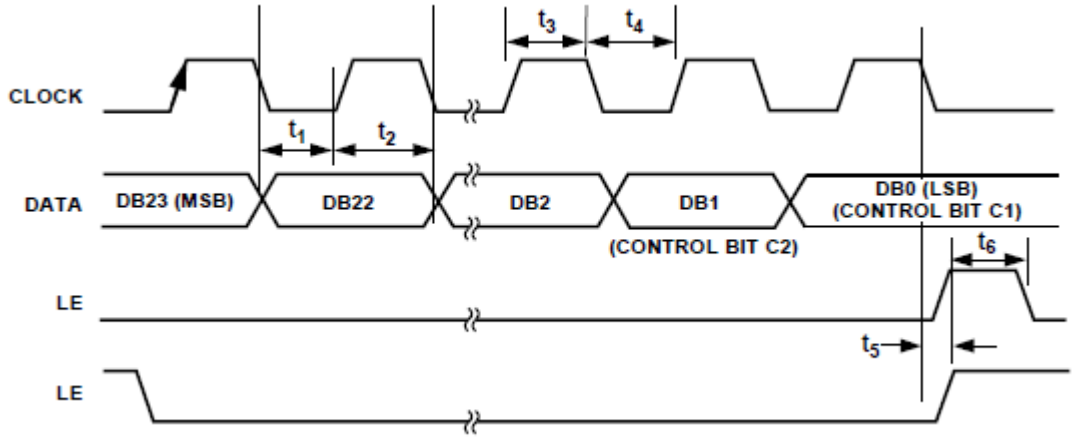

Figure 2 – Timing Diagram.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub-Group	Limit Min	Limit Max	Units
Power Supplies						
AVdd , DVdd Supply Voltage	V_{DD}	Pin AVdd, DVdd, with Avdd = DVdd	1	3.2	3.6	V
			2,3	3.2	3.6	
		M,D,P,L	1	3.2	3.6	
Vcp Supply Voltage	V_{CP}	Pin Vp	1	Vdd	5.5	V
			2,3	Vdd	5.5	
		M,D,P,L	1	Vdd	5.5	
Idd Supply Current	I_{DD}	6/ pin Avdd, DVdd Tested over supply range I_{DD} = AIdd + DIdd, RF = 5GHz	1		17	mA
			2,3		17	
		M,D,P,L	1		17	
Ip Supply Current	I_{CP}	6/ Pin Vp Tested over supply range	1		0.4	mA
			2,3		0.4	
		M,D,P,L	1		0.4	
Idd power down Current	I_{DIS}	6/ 4/ AIdd + DIdd power down, Vcp power down	1		10	µA
			2,3		10	
		M,D,P,L	1		15	

TABLE I NOTES:
1/ T_A Min = -55C, T_A Max = 125C. AVDD = DVDD = 3.3V, GND = AGND = DGND = CPGND = 0V, VCP = 5V, RSET = 5.1kΩ, RF level = 0 dBm, REF level = 0.8 Vpp, RFinB cap coupled to ground unless otherwise noted. Values are relative to 50 Ω.

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots. Parameter not tested post radiation.

3/ This specification is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.

4/ I_{DIS} tested under four conditions:
A. Initial power reset
B. CE = 0.2V
C. CE = 3.0 and Function latch bit DB21/DB3 = 01
D. CE = 3.0 and Function latch bit DB21/DB3 = 11.

5/ Digital pins tested with spec levels during digital pin testing (VIH, VIL, VOH, VOL). Relaxed Digital levels applied for device programing during other testing (VIL = 0.2, VIH = 3.0, VOH > 1.6 with CMOS output, VOL < 0.8).

6/ P = 64/65, R = 50, A = 468, 48, f_{PFD} = 200kHz, REF = 10 MHz

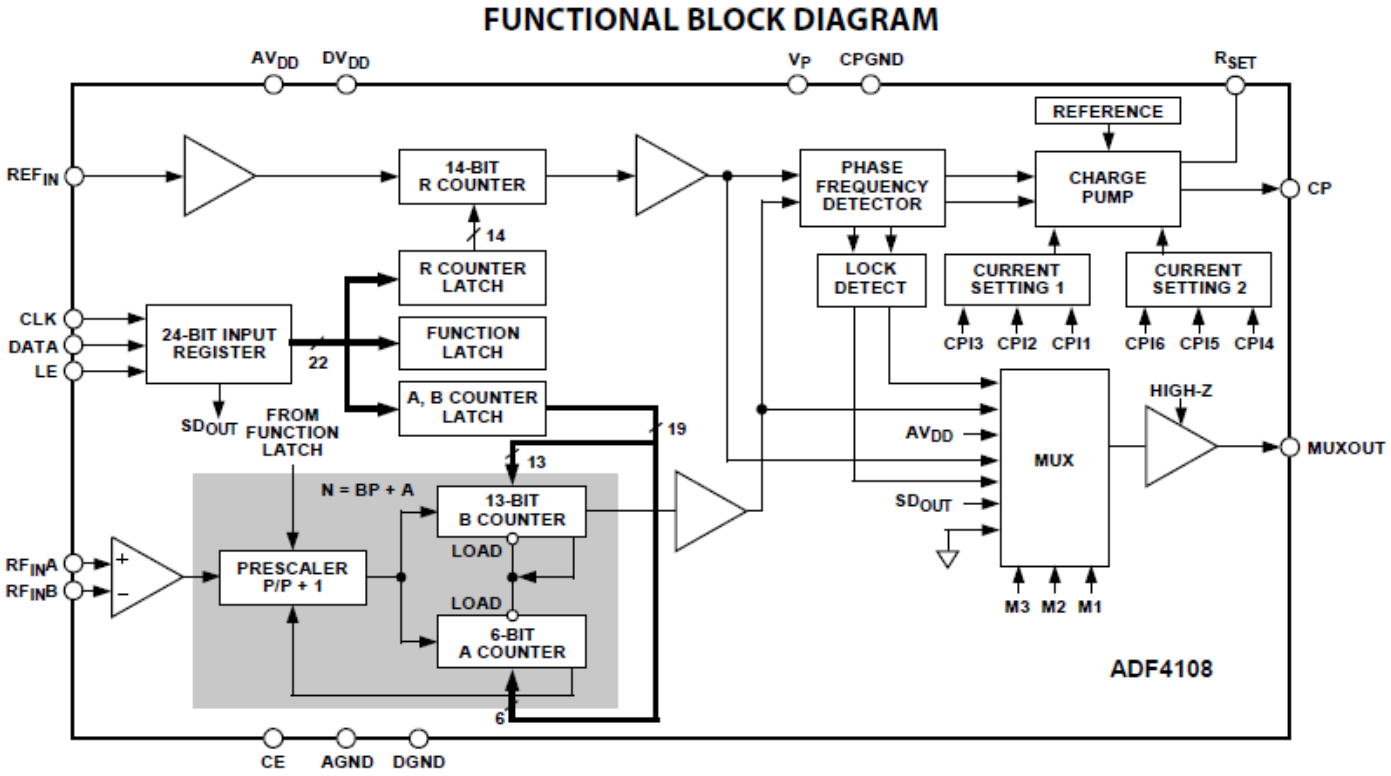

Figure 3 – Block Diagram.

TABLE IIA – ELECTRICAL TEST REQUIREMENTS:

Table IIA	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6 ,9,10,11 1/ 2/ 3/
Group A Test Requirements	1, 2, 3, 4, 5, 6 ,9,10,11
Group C end-point electrical parameters	1, 2, 3, 4, 5, 6 ,9,10,11 2/
Group D end-point electrical parameters	1, 2, 3, 4, 5, 6 ,9,10,11
Group E end-point electrical parameters	1, 4, 9

Table IIA Notes:
1/ PDA apply to subgroup 1 only. Delta's are not excluded from PDA.
2/ See Table IIB for delta parameters.
3/ Parameters marked with note 2/ in Table I are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

TABLE IIB – BURN-IN/GROUP C DELTA LIMITS 1/

Parameters	Symbol	Condition	Delta limits	Units
IDD Supply Current	I_{DD}	V_{DD} = 3.6 V, V_{cp} = 5.5 V	+/- 0.4	mA
ICP Supply Current	I_{CP}	V_{DD} = 3.6 V, V_{cp} = 5.5 V	+/- 0.05	mA
Rset Vout	V_{RSET}	V_{DD} = 3.2 V, V_{cp} = 5.5 V	+/- 0.06	V
Vcp Current, max level	Icp8	V_{DD} = 3.3 V, V_{cp} = 5.5 V	+/- 0.35	mA
Vcp Current, min level	Icp1	V_{DD} = 3.3 V, V_{cp} = 5.5 V	+/- 0.08	mA

1/ Conditions match Table I unless otherwise noted.

5.0. BURN-IN, LIFE TEST, AND RADIATION

5.1. Burn-in test circuit, Life Test circuit

The test conditions and circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 test condition B & D of MIL-STD-883.

HTRB is not applicable for this drawing.

5.2. Radiation exposure circuit

The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A.

6.0. MIL-PRF-38535 QMLV EXCEPTIONS

6.1 Wafer Fabrication

Wafer fabrication occurs at MIL-PRF-38535 QML Class Q certified facility.

6.2 Wafer lot Acceptance (WLA).

Full WLA per MIL-STD-883 TM 5007 is not available for this product. SEM inspection only is available per MIL-STD-883, TM2018.

7.0. Application Notes

THEORY OF OPERATION

REFERENCE INPUT STAGE

The reference input stage is shown in Figure 4. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REFIN pin on power-down.

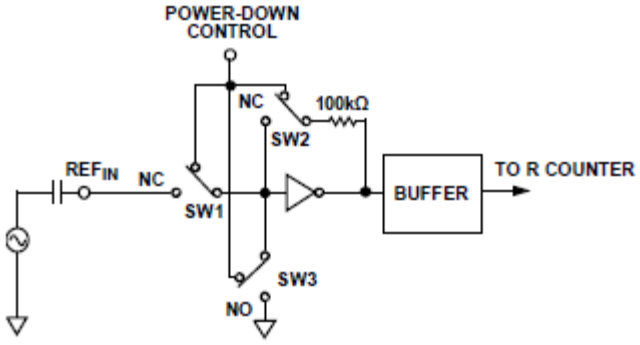

Figure 4. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 5. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

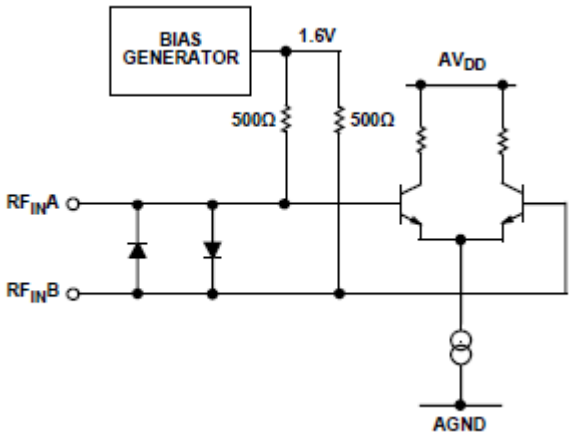

Figure 5. Reference Input Stage

PRESCALER (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. A minimum divide ratio is possible for contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by ($P^2 - P$).

A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN} / R$$

Where:

f_{VCO} is the output frequency of external voltage controlled oscillator (VCO).

P is the preset modulus of dual-modulus prescaler (8/9, 16/17, and so on.).

B is the preset divide ratio of binary 13-bit counter (3 to 8191). *A* is the preset divide ratio of binary 6-bit swallow counter (0 to 63).

f_{REFIN} is the external reference frequency oscillator.

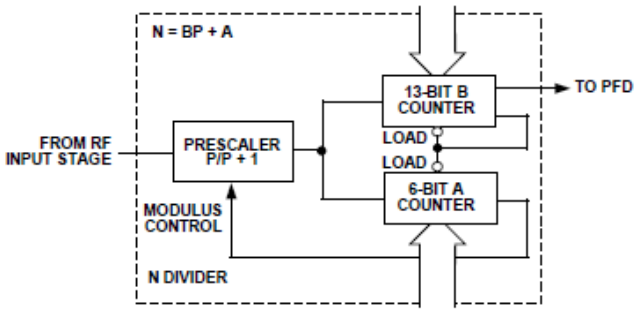

Figure 6. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR AND CHARGE PUMP

The phase frequency detector (PFD) takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 7 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse (see Figure 10). Use of the minimum antibacklash pulse width is not recommended.

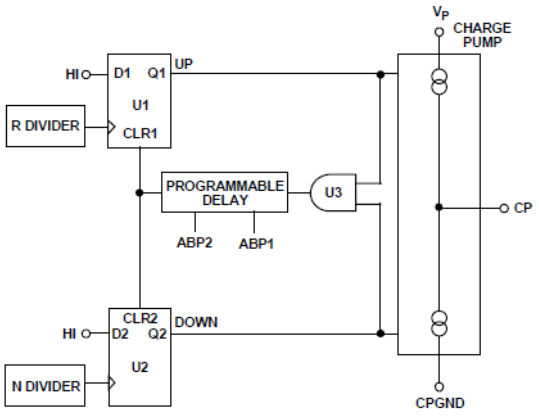

Figure 7. PFD Simplified Schematic and Timing (in Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4108 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 11 shows the full truth table. Figure 8 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.
Digital lock detect is active high. When the lock detect precision (LDP) bit in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.
The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output is high with narrow, low going pulses.

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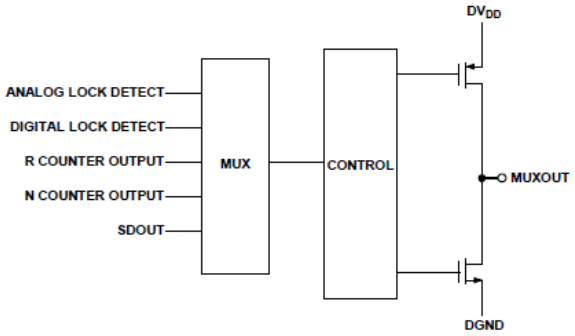

Figure 8. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4108 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the 2 LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table III.

Figure 9 shows a summary of how the latches are programmed.

Table III. C2 and C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R counter
0	1	N counter (A and B)
1	0	Function latch (including prescaler)
1	1	Initialization latch

LATCH SUMMARY

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

Figure 9. Latch Summary

REFERENCE COUNTER LATCH MAP

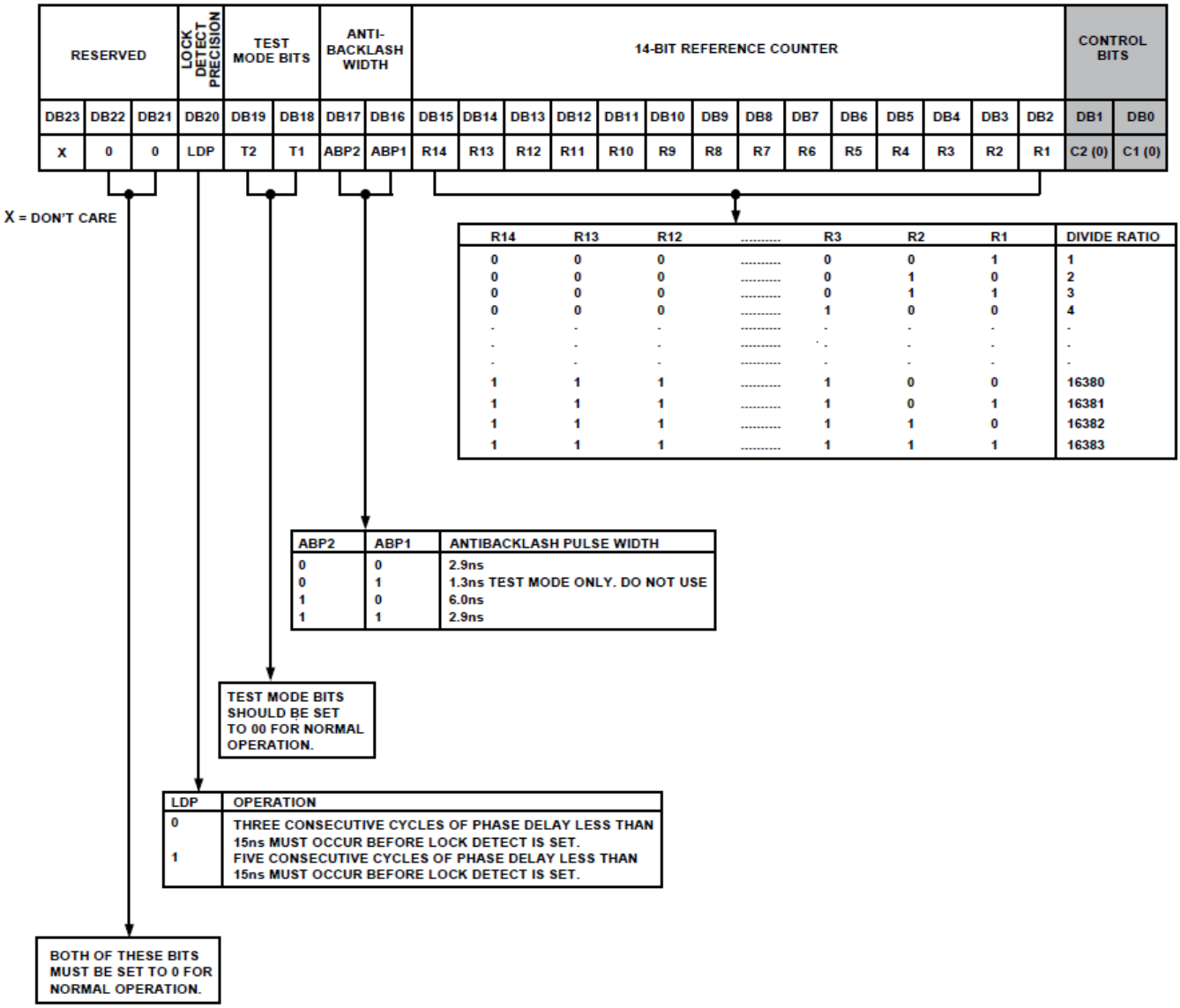

Figure 10. Reference Counter Latch Map

AB COUNTER LATCH MAP

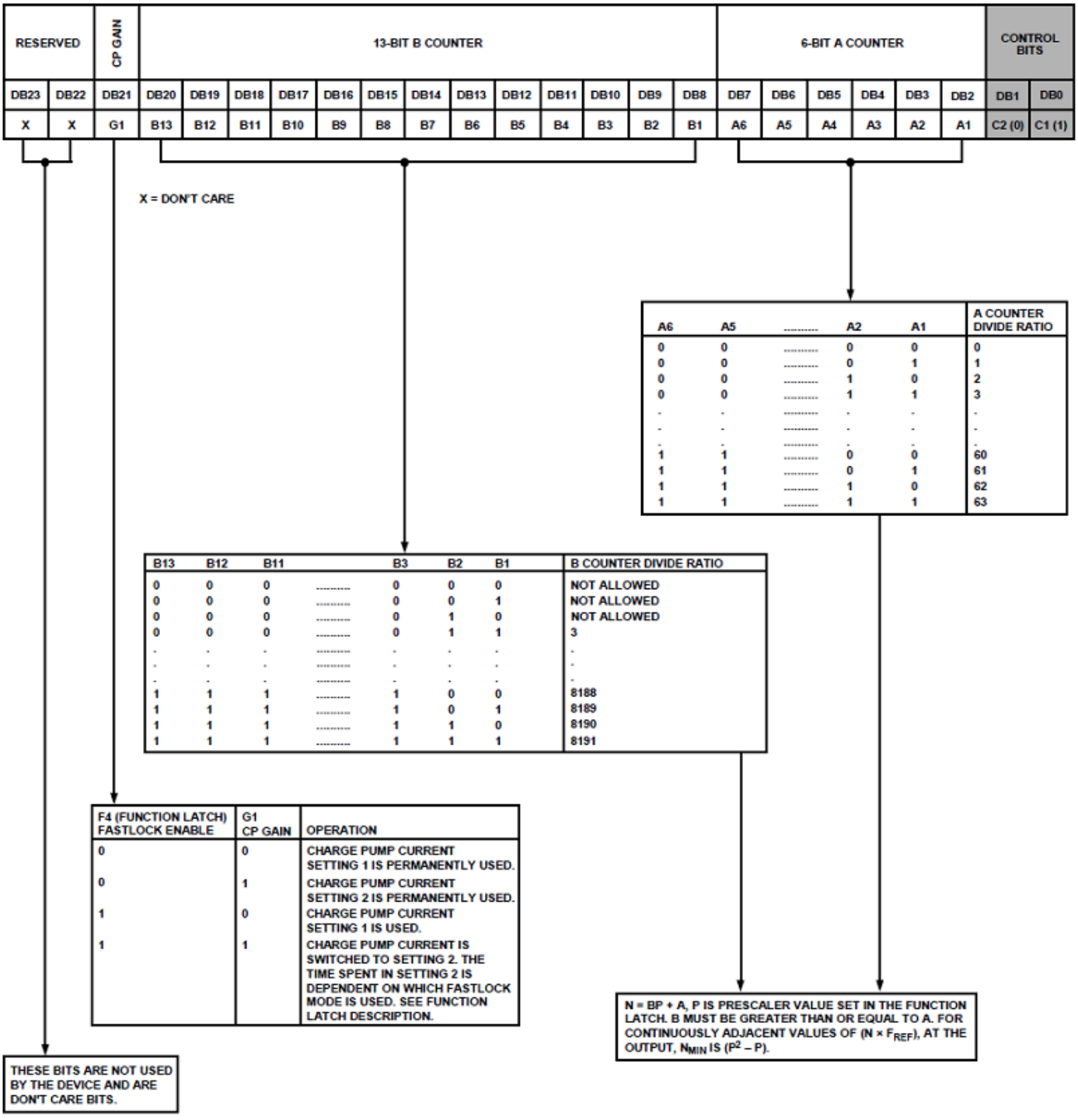

Figure 11. AB Counter Latch Map

FUNCTION LATCH MAP

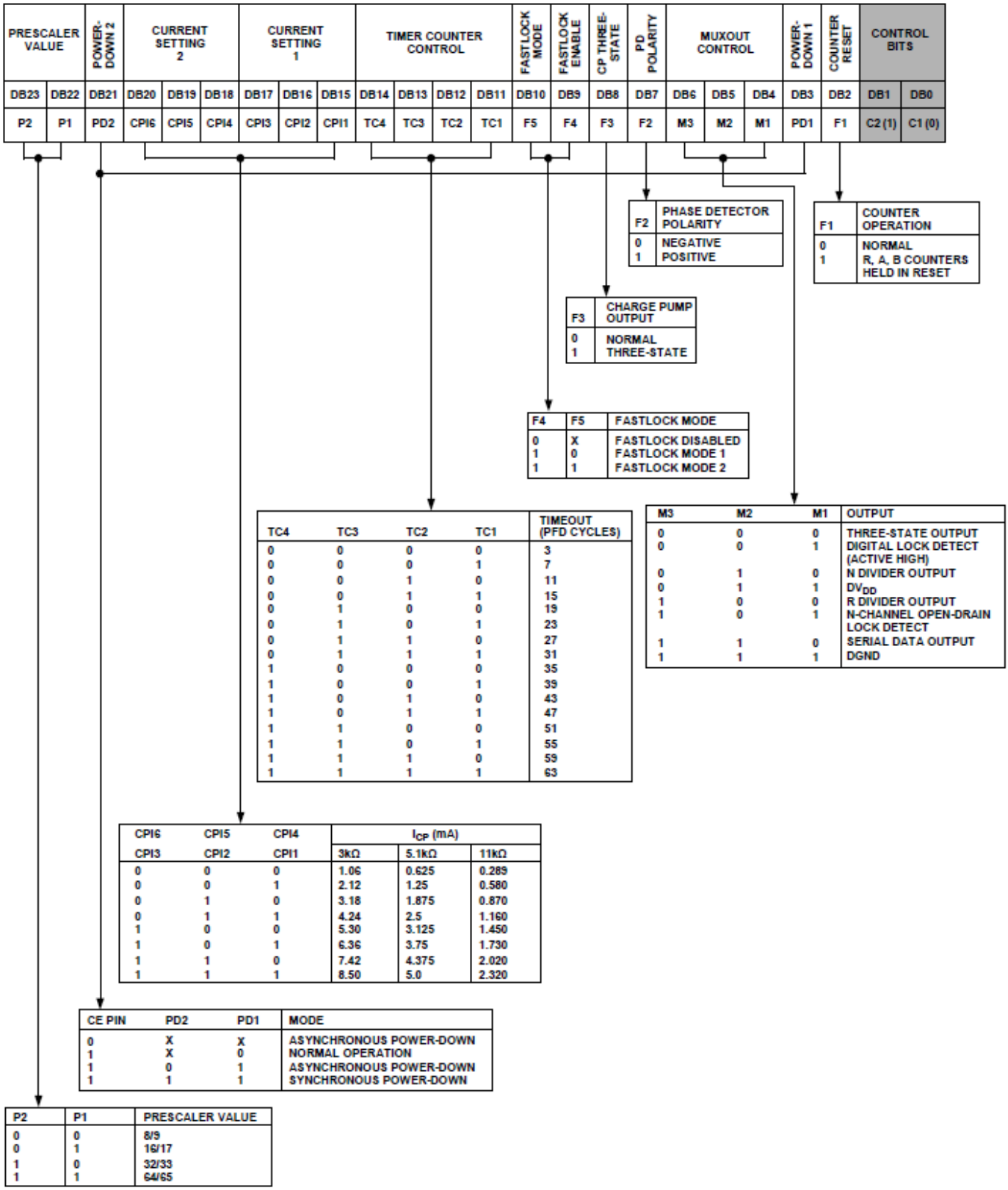

Figure 12. Function Latch Map

INITIALIZATION LATCH MAP

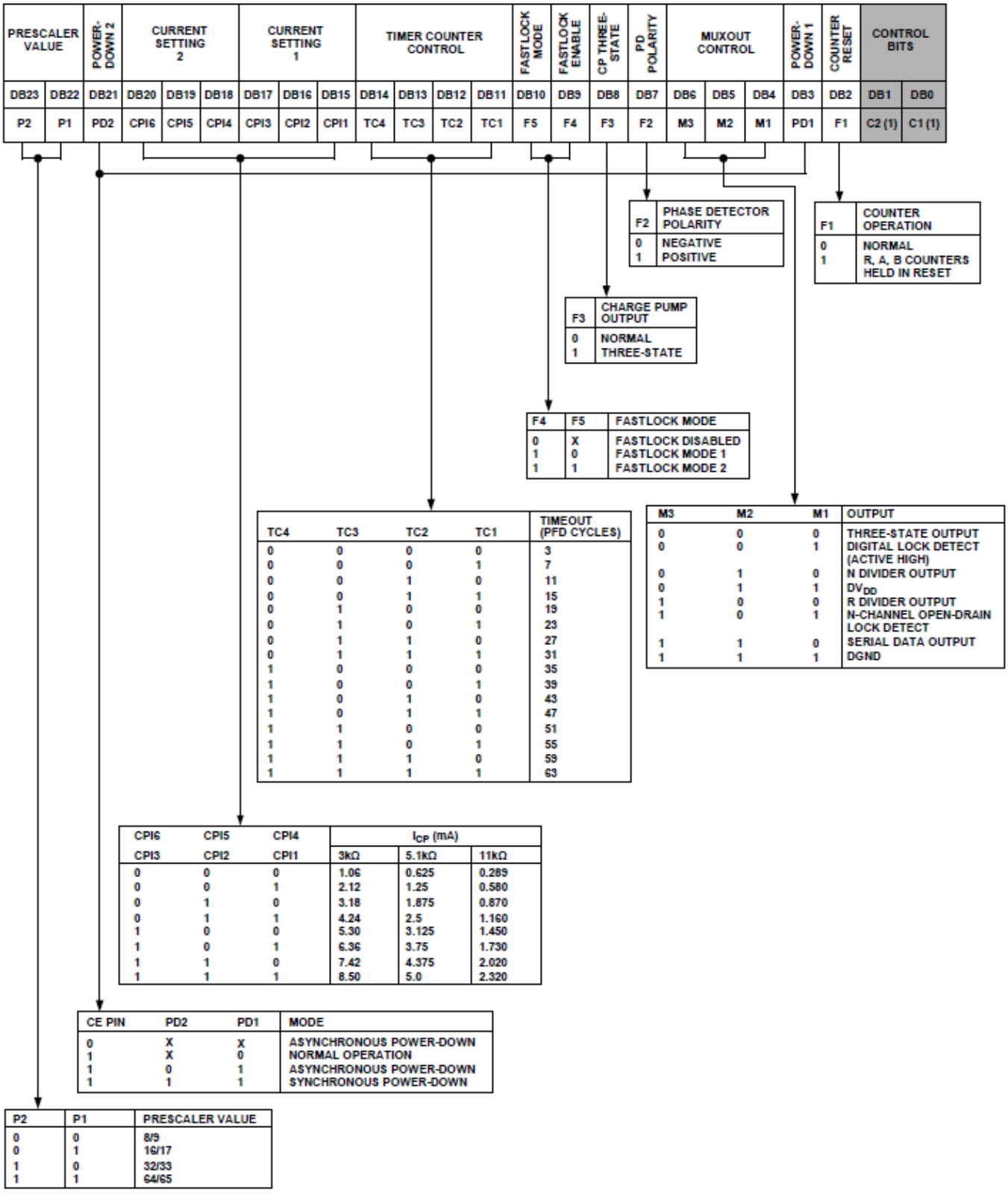

Figure 13. Initialization Latch Map

FUNCTION LATCH

The on-chip function latch is programmed with C2 and C1 set to 1 and 0, respectively. Figure 12 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this bit is 1, the R counter and the AB counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit needs to be disabled (set to 0). Then, the N counter resumes counting in close alignment with the R counter. (The maximum error is one prescaler cycle.)

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. They are enabled by the CE pin.
When the CE pin is low, the device is immediately disabled regardless of the states of PD2 and PD1.
In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into the PD1 bit, with the condition that PD2 has been loaded with a 0.
In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into PD1 (on condition that a 1 has also been loaded to PD2), the device goes into power-down on the occurrence of the next charge pump event.
When a power-down is activated (either synchronous or asynchronous mode, including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RFIN input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4108. Figure 12 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. Fastlock is enabled only when this bit is 1.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected; and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2.
The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2.
The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4:TC1, the CP gain bit in the AB counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Figure 12 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed).
The normal sequence of events is as follows:
The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, it must be decided how long the secondary current is to stay active before reverting to the primary current. This is controlled by the timer counter control bits, DB14:DB11 (TC4:TC1) in the function latch. The truth table is given in Figure 12.
Now, to program a new output frequency, the user simply programs the AB counter latch with new values for A and B. At the same time, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6:CPI4 for a period of time determined by TC4:TC1. When this time is up, the charge pump current reverts to the value set by CPI3:CPI1. At the same time, the CP gain bit in the AB counter latch is reset to 0 and is now ready for the next time the user wishes to change the frequency.
Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents
CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Figure 12.

Prescaler Value
P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 300 MHz. Thus, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

PD Polarity
This bit sets the phase detector polarity bit. See Figure 12.

CP Three-State
This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

INITIALIZATION LATCH
The initialization latch is programmed when C2 and C1 are set to 1 and 1. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0). See Figure 13.
However, when the initialization latch is programmed, an additional internal reset pulse is applied to the R and AB counters. This pulse ensures that the AB counter is at load point when the AB counter data is latched and the device will begin counting in close phase alignment.
If the latch is programmed for synchronous power-down (CE pin is high; PD1 bit is high; PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse and so close phase alignment is maintained when counting resumes.
When the first AB counter data is latched after initialization, the internal reset pulse is again activated. However, successive AB counter loads after this do not trigger the internal reset pulse.

Device Programming After Initial Power-Up
After initially powering up the device, there are three ways to program the device.

Initialization Latch Method
1. Apply VDD.
2. Program the initialization latch (11 in 2 LSBs of input word). Make sure that the F1 bit is programmed to 0.
3. Next, do a function latch load (10 in 2 LSBs of the control word), making sure that the F1 bit is programmed to a 0.
4. Then do an R load (00 in 2 LSBs).
5. Then do an AB load (01 in 2 LSBs).

When the initialization latch is loaded, the following occurs:
1. The function latch contents are loaded.
2. An internal pulse resets the R, AB, and timeout counters to load state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first AB counter data after the initialization word activates the same internal reset pulse. Successive AB loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method
1. Apply VDD.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the AB counter latch (01).
6. Bring CE high to take the device out of power-down. The R and AB counters will now resume counting in close alignment.

Note that after CE goes high, a duration of 1 µs may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.
CE can be used to power the device up and down to check for channel activity. The input register does not need to be repro-grammed each time the device is disabled and enabled as long as it has been programmed at least once after VDD was initially applied.

Counter Reset Method
1. Apply VDD.
2. Do a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in 2 LSBs).
4. Do an AB counter load (01 in 2 LSBs).
5. Do a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

INTERFACING

The ADF4108 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table III for the latch truth table.
The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

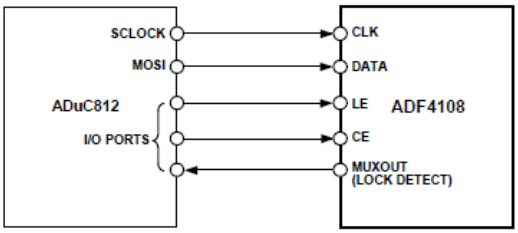

Figure 14 ADuC812 to ADF4108 Interface

ADuC812 Interface example
Figure 14 shows the interface between the ADF4108 and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4108 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.
On first applying power to the ADF4108, it needs four writes (one each to the initialization latch, function latch, R counter latch, and N counter latch) for the output to become active.
I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).
When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4108L703F	–55°C to +125°C	16 Lead Bottom Brazed Flat Pack	X

8.0. Revision History

Rev	Description of Change	Date
A	Initial Release	05/06/2013