22, 15, 7 Stage Data Scrambler with Differential I/O

Description

The CXB1133Q is an ultra high speed monolithic ECL Data Scrambler with variable bit length.

Select switch M selects a mode: "scrambler" or "Maximal code sequence generator". In scrambler mode, input data is converted into a quasi-random data sequence. The quasi-random data can be re-converted into the original input data by a Descrambler such as the CXB1134Q. In M-code sequence generator mode, the IC generates a quasi-random number sequence.

Select inputs S1 and S2 select a bit length.

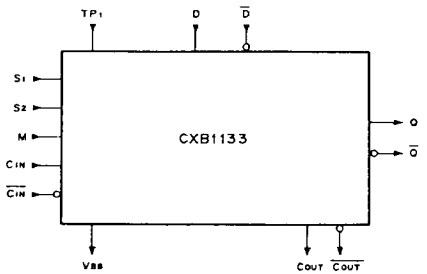
Features

- Typical clock rate up to 1.4GHz
- Variable bit length: 22-bit, 15-bit, 7-bit
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential input and output

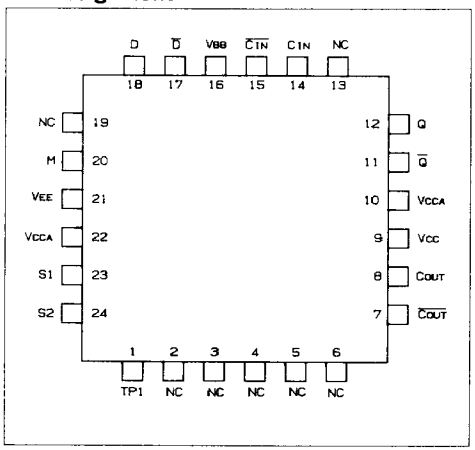
Pin Names

D, $\overline{D}$	Data inputs in scrambler mode
M	Mode Select input
Sn	Select inputs
C_{IN}, $\overline{C_{IN}}$	Clock inputs (positive edge trigger)
Q, $\overline{Q}$	Data outputs
C_{OUT}, $\overline{C_{OUT}}$	Buffered clock outputs
TP1	Test point (It must be left open)
V_{BB}	Reference voltage
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Nagative voltage supply

Logic Symbol



Pin Assignment



Stage Select

S1	S2	Operation
L	L	22 Stage
L	H	15 Stage
H	L	7 Stage
H	H	

Function Select

M	Operation
H	Maximal code sequence generator
L	Data scrambler

H: HIGH voltage level, L: LOW voltage level

DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−147	−108	−76	mA

Note: Other DC characteristics; See page 3-3, 3-4

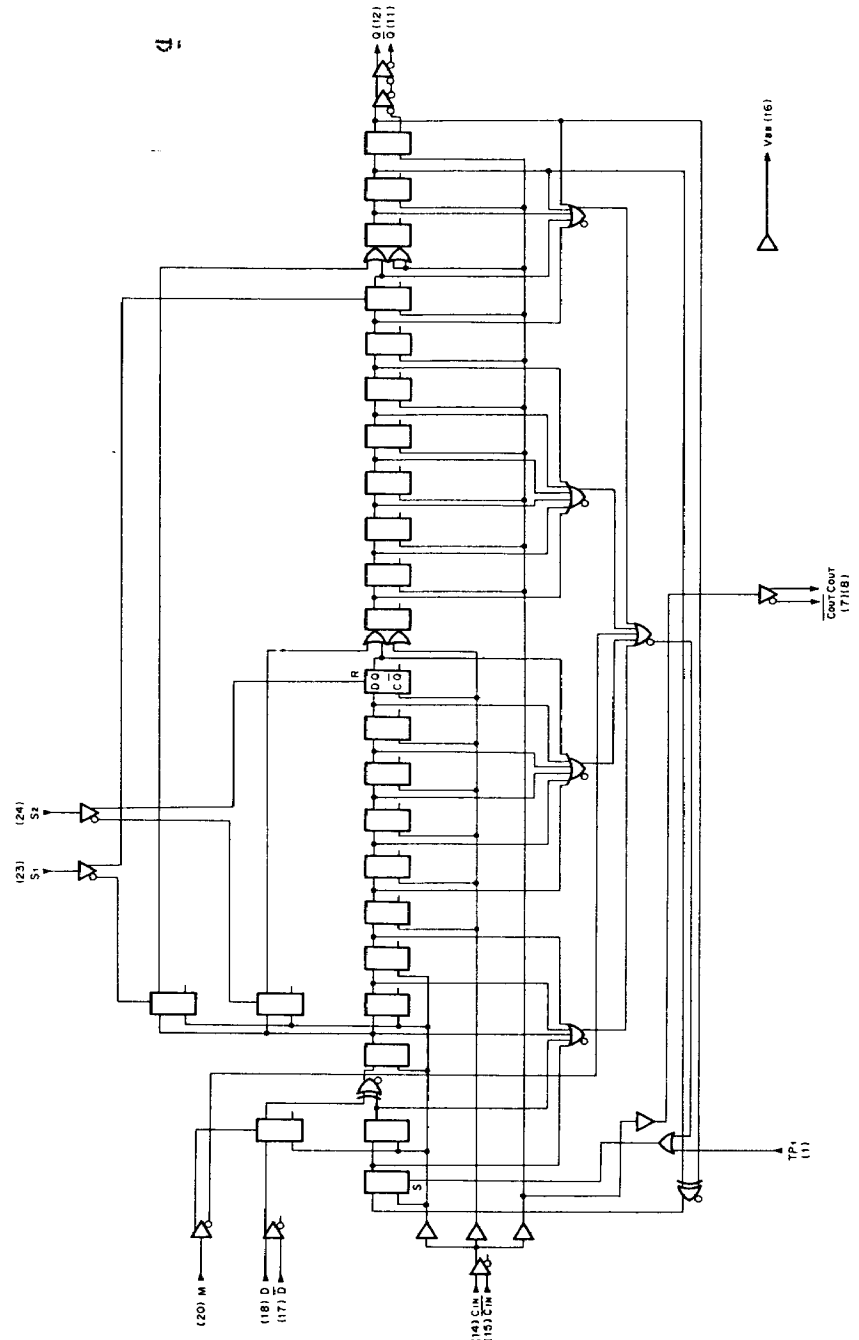
AC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	C_{IN}	Q		1040	1390	1765	ps
	T_{PHL}				1030	1370	1740	
	T_{PLH}		C_{OUT}		650	870	1100	
	T_{PHL}				650	870	1100	
Set up time	T_S	D, C_{IN}	Q	S1=S2=L M=L	80			
Hold time	T_h	C_{IN}, D			290			
Max. Toggle frequency	f_{MAX}	C_{IN}			1.1	1.4		GHz
Rise time	T_{TLH}		Q, C_{OUT}	20% to 80%		300	380	ps
Fall time	T_{THL}					280	355	

Note: AC test circuit; See page 4-4, 4-5

Block Diagram



Scrambler/Descrambler principle

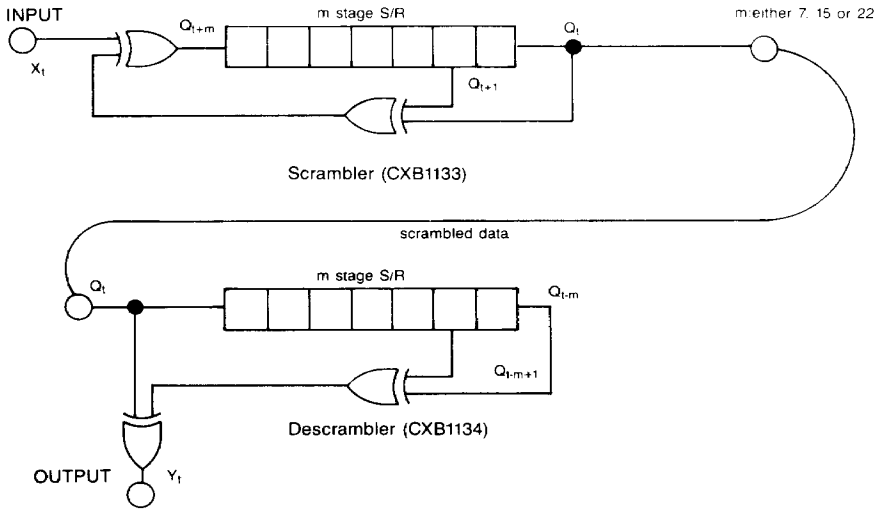


Figure 1. Scrambler/Descrambler (Timming at t)

Scrambler:

$$(Q_t + Q_{t+1}) + X_t = Q_{t+m} \quad \text{--------(1)}$$

Descrambler:

$$(Q_{t-m} + Q_{t-m+1}) + Q_t = Y_t \quad \text{--------(2)}$$

When t = t + m at (2) ;

$$(Q_t + Q_{t+1}) + Q_{t+m} = Y_{t+m} \quad \text{--------(3)}$$

Put (1) into (3);

$$(Q_t + Q_{t+1}) + (Q_t + Q_{t+1}) + X_t = Y_{t+m}$$

$$0 + X_t = Y_{t+m}$$

Thus,

$$X_t = Y_{t+m}$$

Then, data will be restored after m clock.