

54ACT11620, 74ACT11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

T10090—D2857, JULY 1987—REVISED MARCH 1990

- Inputs are TTL-Voltage Compatible
- Local Bus-Latch Capability
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

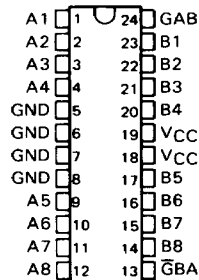
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\bar{G}BA$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

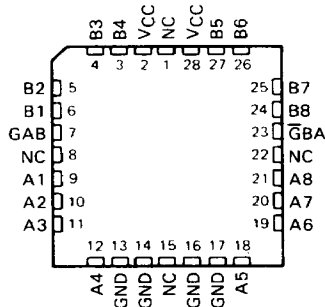
The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\bar{G}BA$ and GAB . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary for the ACT11620.

The 54ACT11620 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT11620 is characterized for operation from -40°C to 85°C .

54ACT11620 ... JT PACKAGE
74ACT11620 ... DW OR NT PACKAGE
(TOP VIEW)



54ACT11620 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\bar{G}BA$	GAB	
L	L	\bar{B} data to A bus
H	H	\bar{A} data to B bus
H	L	Isolation
L	H	\bar{B} data to A bus, \bar{A} data to B bus

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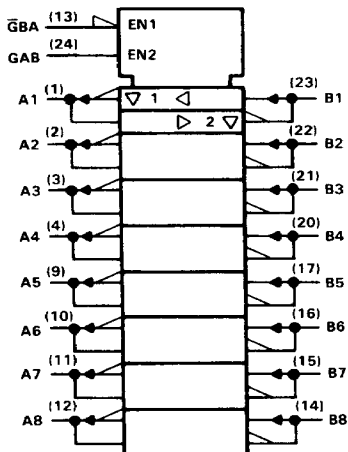
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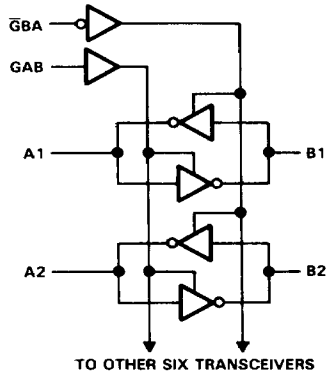
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

		54ACT11620		74ACT11620		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	6.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-24	mA
I _{OL}	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11620		74ACT11620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4	4.4	V		
		5.5 V	5.4			5.4	5.4			
	I _{OH} = -24 mA	4.5 V	3.94			3.7	3.8			
		5.5 V	4.94			4.7	4.8			
	I _{OH} = -50 mA [†]	5.5 V				3.85				
I _{OH} = -75 mA [†]	5.5 V					3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1	0.1	V		
		5.5 V			0.1	0.1	0.1			
	I _{OL} = 24 mA	4.5 V			0.36	0.5	0.44			
		5.5 V			0.36	0.5	0.44			
	I _{OL} = 50 mA [†]	5.5 V				1.65				
I _{OL} = 75 mA [†]	5.5 V					1.65				
I _{OZ}	A or B ports [‡]	V _O = V _{CC} or GND	5.5 V		±0.5	±10	±5	μA		
I _I	\bar{G} B A or GAB	V _I = V _{CC} or GND	5.5 V		±0.1	±1	±1	μA		
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V		8	16	8	μA		
ΔI _{CC} [§]		One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.9	1	1	mA		
C _i	\bar{G} B A or GAB	V _I = V _{CC} or GND	5 V		4			pF		
C _o	A or B ports	V _O = V _{CC} or GND	5 V		12			pF		

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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switching characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11620		74ACT11620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	5.7	8.5	1.5	10	1.5	9.4	ns
t_{PHL}			1.5	5.9	7.7	1.5	9.2	1.5	8.6	
t_{PZH}	$\overline{\text{C}}\text{BA}$	A	1.5	7.2	9.1	1.5	11.1	1.5	10.3	ns
t_{PZL}			1.5	7.1	9.2	1.5	10.8	1.5	10.1	
t_{PHZ}	$\overline{\text{C}}\text{BA}$	A	1.5	7.9	9.6	1.5	11	1.5	10.4	ns
t_{PLZ}			1.5	8.3	10	1.5	11.6	1.5	10.9	
t_{PZH}	GAB	B	1.5	7.5	10.2	1.5	12.2	1.5	11.3	ns
t_{PZL}			1.5	7.7	9.8	1.5	11.9	1.5	11	
t_{PHZ}	GAB	B	1.5	7.2	8.9	1.5	9.8	1.5	9.4	ns
t_{PLZ}			1.5	7.2	8.9	1.5	10	1.5	9.6	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	54	pF
		Outputs disabled		11	

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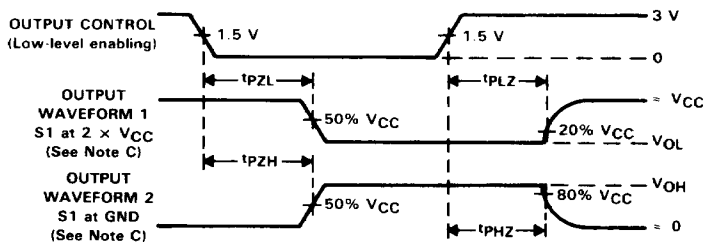
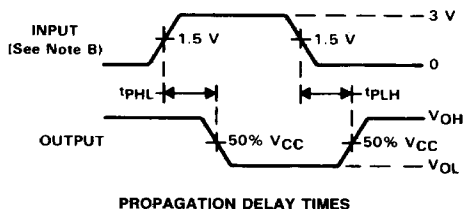
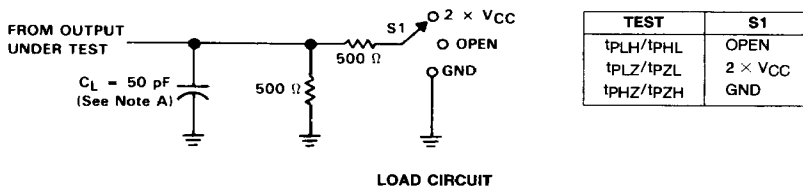

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by the generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS



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