Integrated Device Technology, Inc.

32K x 8-BIT BiCMOS SRAM WITH ADDRESS LATCH

ADVANCE INFORMATION
IDT71B556

FEATURES:

- 32K x 8 BiCEMOS™ Static RAM with Address Latch
- High-speed address/chip select time
  - — Military: 20ns
  - — Commercial: 12/15/20ns
- Two Chip Selects plus one Output Enable pin
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 32-pin sidebraze and plastic, 300 mil DIP and 32-pin, 300 mil SOJ packages
- Military product is fully compliant to MIL-STD-883, Class B

DESCRIPTION:

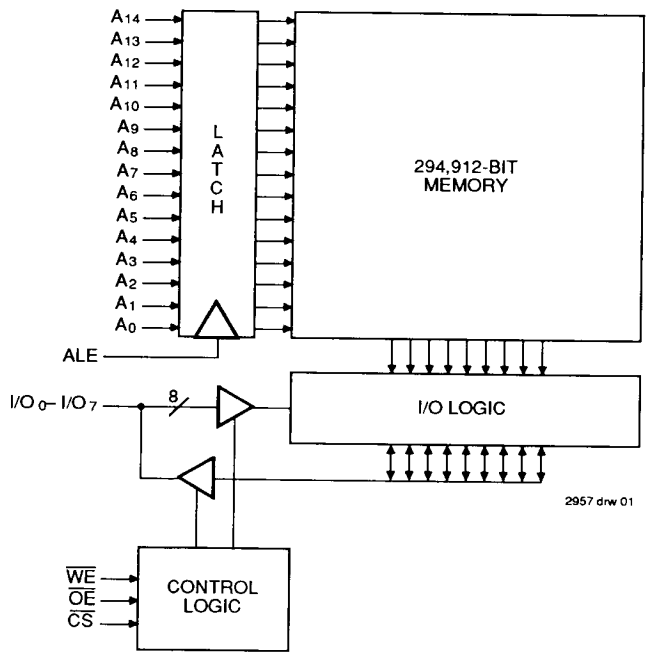
The IDT71B556 is a 256,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high performance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

This memory is based on the standard 32K x 8 pinout and functionality, but also contains an address latch. When ALE is high the latch is transparent. When ALE is low, the address is latched.

Address access times as fast as 12 ns are available with power consumption of only 550mW (typ.). All inputs and outputs of the IDT71B556 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used.

The IDT71B556 is packaged in a 32-pin, 300-mil sidebraze; 32-pin, 300 mil plastic DIP and a 32-pin SOJ package. The IDT71B556 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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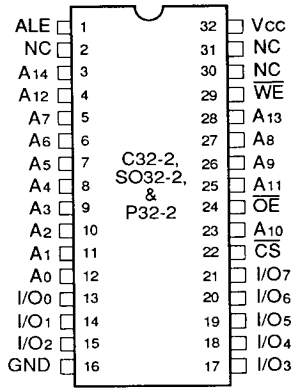
PIN CONFIGURATIONS



2957 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2957 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE(1)

CS_2	$\overline{CS_1}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	Hi-Z	Deselect chip
L	L	X	X	Hi-Z	Deselect Chip
H	L	L	H	D_{OUT}	Read
H	L	X	L	D_{IN}	Write
H	L	H	X	Hi-Z	Output Disabled

NOTE: 2957 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don,t care.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	12	pF

NOTE: 2957 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2957 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71556 Min.	IDT71556 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., CS = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2957 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B556S12		71B556S15		71B556S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	200	—	190	—	170	180	mA

NOTES:
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$.

2957 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2957 tbl 07

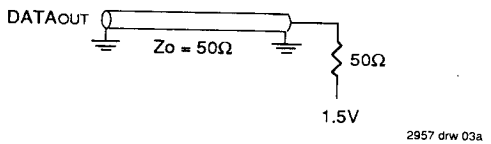


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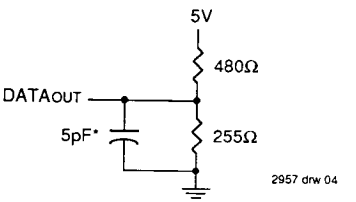
Figure 1A. AC Test Load



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*Including jig and scope capacitance.

Figure 1B.

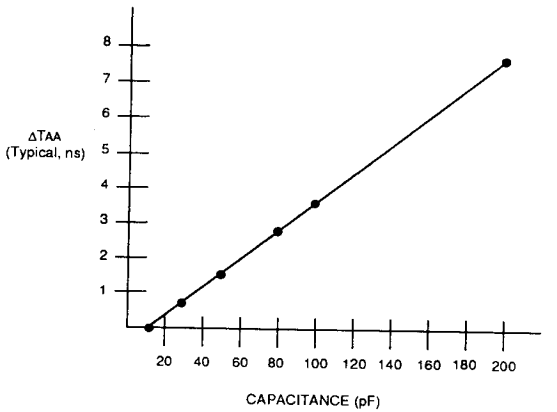

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Figure 1C. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B556-12(1) Min.	71B556-12(1) Max.	71B556-15(1) Min.	71B556-15(1) Max.	71B556-20 Min.	71B556-20 Max.	Unit
Read Cycle								
tRC	Read Cycle Time	12	—	15	—	20	—	ns
tCH	ALE High	6	—	7	—	10	—	ns
tCL	ALE Low	6	—	7	—	10	—	ns
tAS	ALE Setup Time	4	—	4	—	5	—	ns
tAA	Address Access Time	—	12	—	15	—	20	ns
tAH	Address Latch Hold	3	—	4	—	5	—	ns
tACS	CS Access Time	—	7	—	8	—	10	ns
tOE	Output Enable Time	—	7	—	8	—	10	ns
tCLZ(2)	$\overline{CS}$ to Output in Low Z	3	—	4	—	5	—	ns
tCHZ(2)	$\overline{CS}$ to Output in High Z	—	4	—	5	—	6	ns
tOLZ(2)	$\overline{OE}$ to Output Low Z	3	—	4	—	5	—	ns
tOHZ(2)	$\overline{OE}$ to Output High Z	—	4	—	5	—	6	ns
tOH	Out Hold from Add Change	3	—	3	—	3	—	ns
Write Cycle								
tWC	Write Cycle Time	12	—	15	—	20	—	ns
tCH	ALE High	6	—	7	—	10	—	ns
tCL	ALE Low	6	—	7	—	10	—	ns
tAS	ALE Setup Time	0	—	0	—	0	—	ns
tAH	ALE Hold TIme	3	—	4	—	5	—	ns
tAW	Address to End of Write	9	—	10	—	12	—	ns
tASW	Address Setup Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	9	—	10	—	12	—	ns
tCW1	$\overline{CS}$ to End of Write	8	—	9	—	10	—	ns
tWR1	Write Recovery	0	—	0	—	0	—	ns
tWR2	Write Recovery	-1	—	-1	—	-1	—	ns
tWHZ(2)	$\overline{WE}$ to Output in High Z	—	5	—	6	—	7	ns
tDW	Data Set-Up	6	—	8	—	10	—	ns
tDH	Data Hold	2	—	2	—	2	—	ns
tOW	Output from End of Write	3	—	4	—	4	—	ns

2957 tbl 08

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.

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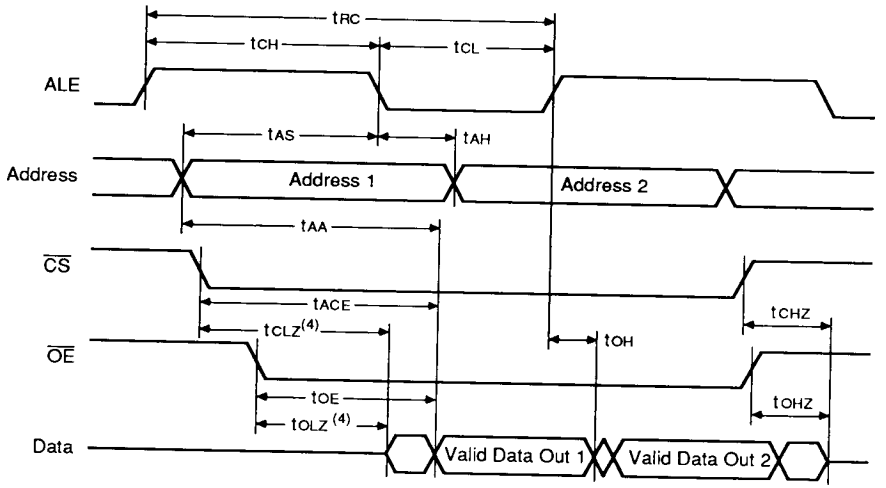
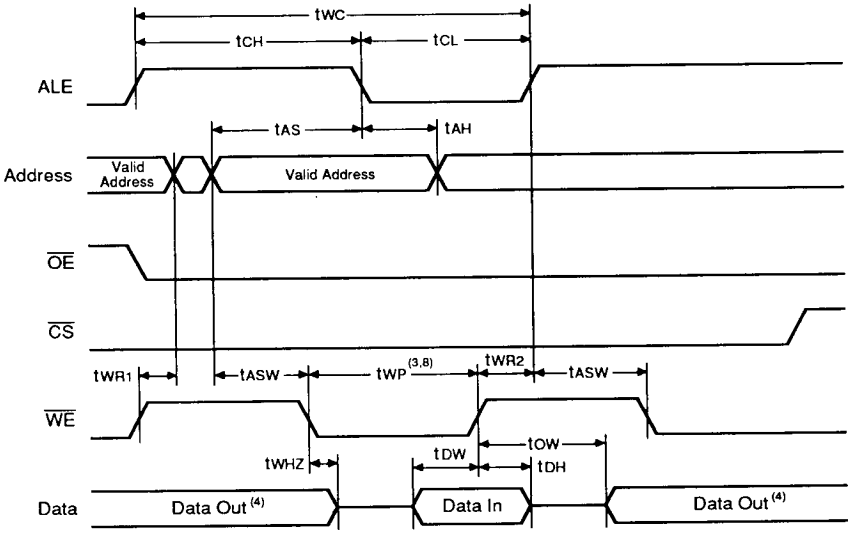
TIMING WAVEFORM OF READ CYCLE(1,2,3)



NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)(1,2,5,6,7)



NOTES:
1. $\overline{OE}$ is low in order to show tWHZ and tOW.
2. A write occurs during the overlap (tWC and tWP) of $\overline{CS}$ low and $\overline{WE}$ low.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ being deasserted.
4. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
5. If $\overline{CS}$ is asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
6. If $\overline{CS}$ is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
7. The transition is measured ±200mV from steady state with a 5pF load.
8. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse width can be as rt as the specified tWP.

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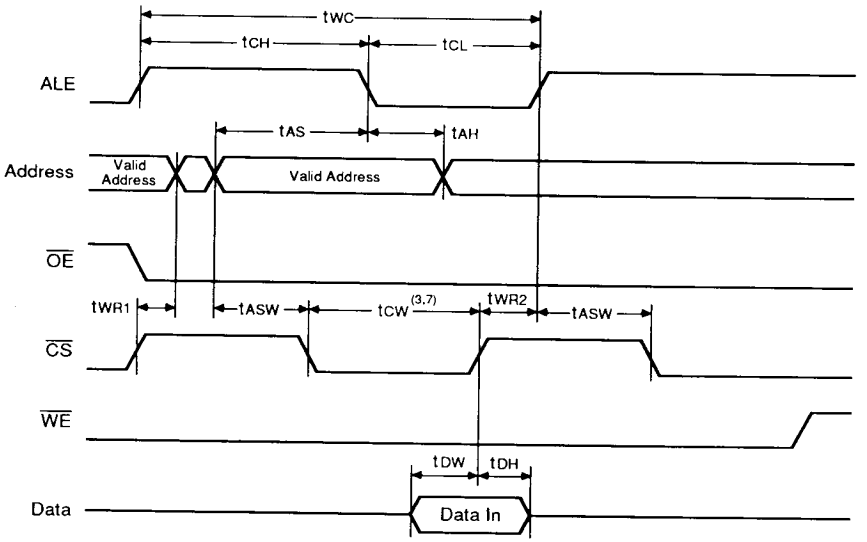
TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ Controlled)(1,2,4,5,6)



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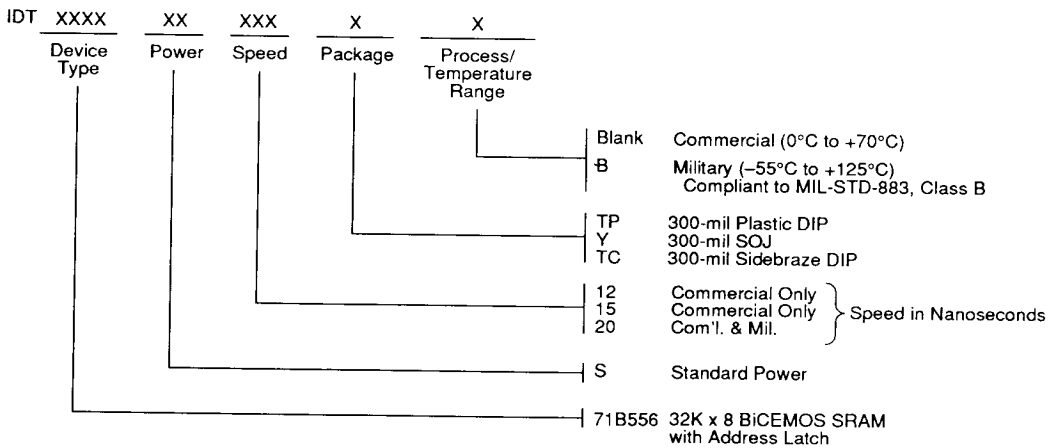
NOTES:
1. $\overline{OE}$ is low in order to show tWHZ and tOW.
2. A write occurs during the overlap (tWC and tWP) of $\overline{CS}$ low and $\overline{WE}$ low.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ being deasserted.
4. If $\overline{CS}$ is asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
5. If $\overline{CS}$ is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse width can be as short as the specified tWP.

ORDERING INFORMATION



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