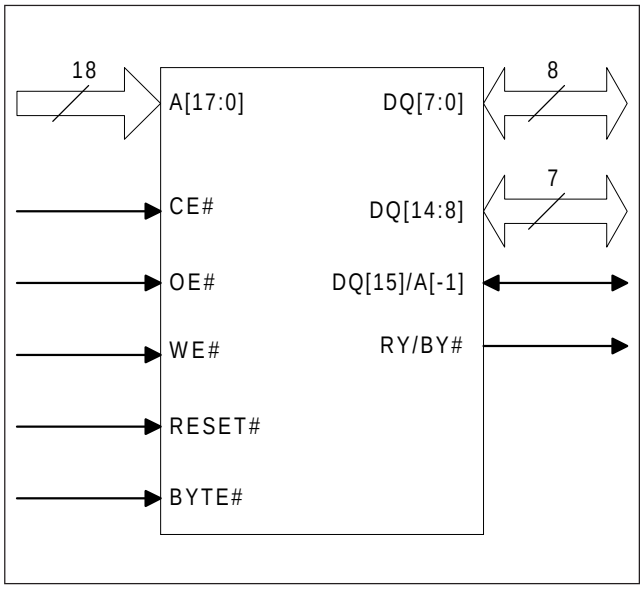
KEY FEATURES

- **Single Power Supply Operation**
  - Read, program and erase operations from 2.7 to 3.6 volts
  - Ideal for battery-powered applications
- **High Performance**
  - 70 and 90 ns access time versions for full voltage range operation
  - 55 ns access time version for operation from 3.0 to 3.6 volts
- **Ultra-low Power Consumption (Typical Values)**
  - Automatic sleep mode current: 0.2 µA
  - Standby mode current: 0.2 µA
  - Read current: 7 mA (at 5 Mhz)
  - Program/erase current: 15 mA
- **Flexible Sector Architecture:**
  - One 16 KB, two 8 KB, one 32 KB and seven 64 KB sectors in byte mode
  - One 8 KW, two 4 KW, one 16 KW and seven 32 KW sectors in word mode
  - Top or bottom boot block configurations available
- **Sector Protection**
  - Allows locking of a sector or sectors to prevent program or erase operations within that sector
  - Sectors lockable in-system or via programming equipment
  - Temporary Sector Unprotect allows changes in locked sectors (requires high voltage on RESET# pin)
- **Fast Program and Erase Times**
  - Sector erase time: 0.5 sec typical for each sector
  - Chip erase time: 5 sec typical
  - Byte program time: 9 µs typical
  - Word program time: 11 µs typical
- **Unlock Bypass Program Command**
  - Reduces programming time when issuing multiple program command sequences
- **Automatic Erase Algorithm Preprograms and Erases Any Combination of Sectors or the Entire Chip**
- **Automatic Program Algorithm Writes and Verifies Data at Specified Addresses**
- **Minimum 100,000 Write Cycles per Sector**
- **Compatible With JEDEC standards**
  - Pinout and software compatible with single-power supply Flash devices
  - Superior inadvertent write protection
- **Data# Polling and Toggle Bits**
  - Provide software confirmation of completion of program and erase operations
- **Ready/Busy# Pin**
  - Provides hardware confirmation of completion of program and erase operations
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to allow reading data from, or programming data to, a sector that is not being erased
  - Erase Resume can then be invoked to complete suspended erasure
- **Hardware Reset Pin (RESET#) Resets the Device to Reading Array Data**
- **Space Efficient Packaging**
  - 48-pin TSOP and 48-ball FBGA packages

LOGIC DIAGRAM



GENERAL DESCRIPTION

The HY29LV400 is a 4 Mbit, 3 volt-only, CMOS Flash memory organized as 524,288 (512K) bytes or 262,144 (256K) words that is available in 48-pin TSOP and 48-ball FBGA packages. Word-wide data (x16) appears on DQ[15:0] and byte-wide (x8) data appears on DQ[7:0].

The HY29LV400 can be programmed and erased in-system with a single 3 volt V_{CC} supply. Internally generated and regulated voltages are provided for program and erase operations, so that the device does not require a higher voltage V_{PP} power supply to perform those functions. The device can also be programmed in standard EPROM programmers. Access times as low as 70 ns over the full operating voltage range of 2.7 - 3.6 volts are offered for timing compatibility with the zero wait state requirements of high speed microprocessors. A 55 ns version operating from 3.0 to 3.6 volts is also available. To eliminate bus contention, the HY29LV400 has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device is compatible with the JEDEC single-power-supply Flash command set standard. Commands are written to the command register using standard microprocessor write timings. They are then routed to an internal state-machine that controls the erase and programming circuits. Device programming is performed a byte/word at a time by executing the four-cycle Program Command write sequence. This initiates an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Faster programming times can be achieved by placing the HY29LV400 in the Unlock Bypass mode, which requires only two write cycles to program data instead of four.

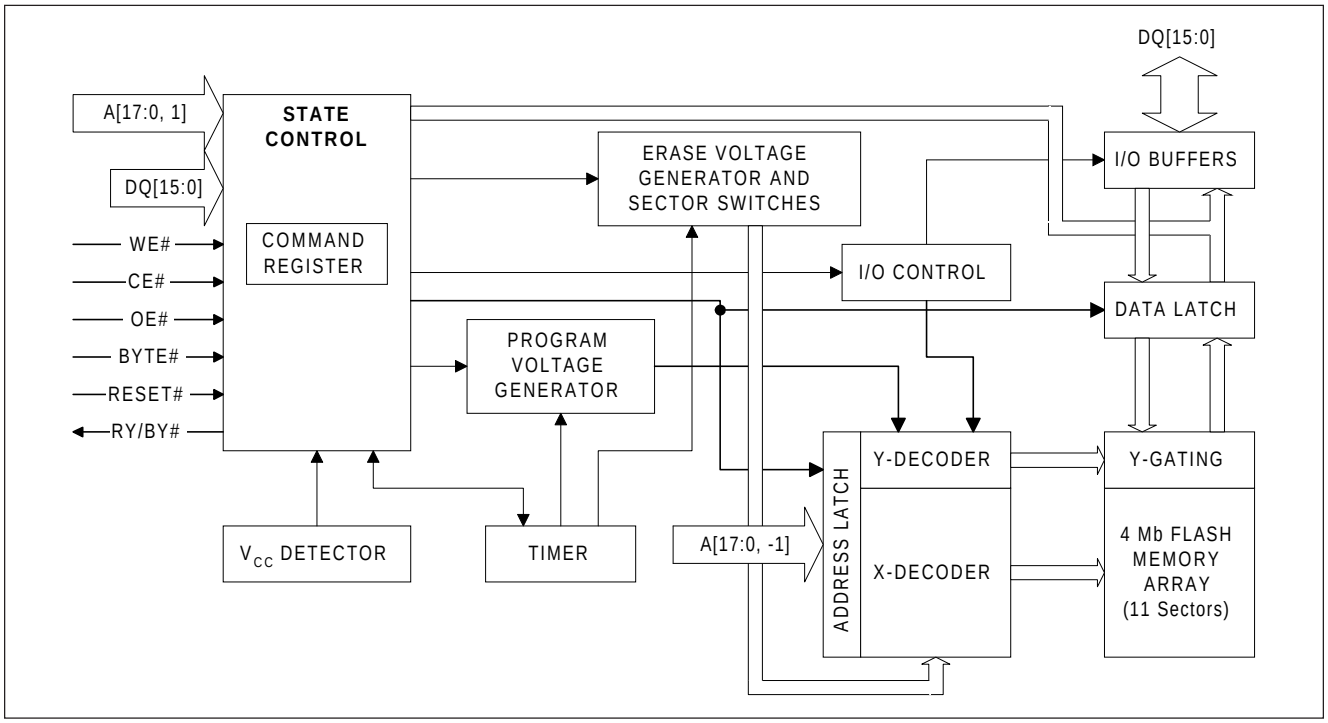
The HY29LV400's sector erase architecture allows any number of array sectors to be erased and reprogrammed without affecting the data contents of other sectors. Device erasure is initiated by executing the Erase Command sequence. This initiates an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. As during programming cycles, the device automatically times the erase pulse widths and verifies proper cell margin. Hardware Sector Protection optionally disables both program and erase operations in any combination of the sectors of the memory array, while Temporary Sector Unprotect allows in-system erasure and code changes in previously protected sectors. Erase Suspend enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. The device is fully erased when shipped from the factory.

Addresses and data needed for the programming and erase operations are internally latched during write cycles, and the host system can detect completion of a program or erase operation by observing the RY/BY# pin, or by reading the DQ[7] (Data# Polling) and DQ[6] (toggle) status bits. Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions.

After a program or erase cycle has been completed, or after assertion of the RESET# pin (which terminates any operation in progress), the device is ready to read data or to accept another command. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Two power-saving features are embodied in the HY29LV400. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The host can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Name	Type	Description
A[17:0]	Inputs	**Address, active High.** These 18 inputs, combined with the DQ[15]/A[-1] input in Byte mode, select one location within the array for read or write operations.
DQ[15]/A[-1], DQ[14:0]	Inputs/Outputs Tri-state	**Data Bus, active High**. These pins provide an 8- or 16-bit data path for read and write operations. In Byte mode, DQ[15]/A[-1] is used as the LSB of the 19-bit byte address input. DQ[14:8] are unused and remain tri-stated in Byte mode.
BYTE#	Input	**Byte Mode, active Low.** Low selects Byte mode, High selects Word mode.
CE#	Input	**Chip Enable, active Low.** This input must be asserted to read data from or write data to the HY29LV400. When High, the data bus is tri-stated and the device is placed in the Standby mode.
OE#	Input	**Output Enable, active Low**. Asserted for read operations and negated for write operations. BYTE# determines whether a byte or a word is read during the read operation.
WE#	Input	**Write Enable, active Low.** Controls writing of commands or command sequences in order to program data or erase sectors of the memory array. A write operation takes place when WE# is asserted while CE# is Low and OE# is High.
RESET#	Input	**Hardware Reset, active Low.** Provides a hardware method of resetting the HY29LV400 to the read array state. When the device is reset, it immediately terminates any operation in progress. While RESET# is asserted, the device will be in the Standby mode.
RY/BY#	Output Open Drain	**Ready/Busy Status.** Indicates whether a write or erase command is in progress or has been completed. Remains Low while the device is actively programming data or erasing, and goes High when it is ready to read array data.
V_{CC}	--	**3-volt (nominal) power supply.**
V_{SS}	--	**Power and signal ground.**

PIN CONFIGURATIONS

48-Ball FBGA (6 x 8 mm, Top View, Balls Facing Down)

A6	B6	C6	D6	E6	F6	G6	H6
A[13]	A[12]	A[14]	A[15]	A[16]	BYTE#	DQ[15]/A[-1]	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A[9]	A[8]	A[10]	A[11]	DQ[7]	DQ[14]	DQ[13]	DQ[6]
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	NC	DQ[5]	DQ[12]	V_{CC}	DQ[4]
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	NC	NC	DQ[2]	DQ[10]	DQ[11]	DQ[3]
A2	B2	C2	D2	E2	F2	G2	H2
A[7]	A[17]	A[6]	A[5]	DQ[0]	DQ[8]	DQ[9]	DQ[1]
A1	B1	C1	D1	E1	F1	G1	H1
A[3]	A[4]	A[2]	A[1]	A[0]	CE#	OE#	V_{SS}

TSOP48

A15	1	48	A16
A14	2	47	BYTE#
A13	3	46	V_{SS}
A12	4	45	DQ15/A-1
A11	5	44	DQ7
A10	6	43	DQ14
A9	7	42	DQ6
A8	8	41	DQ13
NC	9	40	DQ5
NC	10	39	DQ12
WE#	11	38	DQ4
RESET#	12	37	V_{CC}
NC	13	36	DQ11
NC	14	35	DQ3
RY/BY#	15	34	DQ10
NC	16	33	DQ2
A17	17	32	DQ9
A7	18	31	DQ1
A6	19	30	DQ8
A5	20	29	DQ0
A4	21	28	OE#
A3	22	27	V_{SS}
A2	23	26	CE#
A1	24	25	A0

CONVENTIONS

Unless otherwise noted, a positive logic (active High) convention is assumed throughout this document, whereby the presence at a pin of a higher, more positive voltage (V_{IH}) causes assertion of the signal. A '#' symbol following the signal name, e.g., RESET#, indicates that the signal is asserted in the Low state (V_{IL}). See DC specifications for V_{IH} and V_{IL} values.

Whenever a signal is separated into numbered bits, e.g., DQ[7], DQ[6], ..., DQ[0], the family of bits may also be shown collectively, e.g., as DQ[7:0].

The designation 0xNNNN (N = 0, 1, 2, . . . , 9, A, . . . , E, F) indicates a number expressed in hexadecimal notation. The designation 0bXXXX indicates a number expressed in binary notation (X = 0, 1).

MEMORY ARRAY ORGANIZATION

The 4 Mbit Flash memory array is organized into eleven blocks called *sectors* (S0, S1, . . . , S10). A sector is the smallest unit that can be erased and that can be protected to prevent accidental or unauthorized erasure. See the 'Bus Operations' and 'Command Definitions' sections of this document for additional information on these functions.

In the HY29LV400, four of the sectors, which comprise the *boot block*, vary in size from 8 to 32 Kbytes (4 to 16 Kwords), while the remaining seven sectors are uniformly sized at 64 Kbytes (32 Kwords). The boot block can be located at the bottom of the address range (HY29LV400B) or at the top of the address range (HY29LV400T).

Tables 1 and 2 define the sector addresses and corresponding address ranges for the top and bottom boot block versions of the HY29LV400.

BUS OPERATIONS

Device bus operations are initiated through the internal command register, which consists of sets of latches that store the commands, along with the address and data information, if any, needed to execute the specific command. The command register itself does not occupy any addressable memory location. The contents of the command register serve as inputs to an internal state machine whose outputs control the operation of the device. Table 3 lists the normal bus operations, the inputs and control levels they require, and the resulting outputs. Certain bus operations require a high voltage on one or more device pins. Those are described in Table 4.

Read Operation

Data is read from the HY29LV400 by using standard microprocessor read cycles while placing the byte or word address on the device's address inputs. The host system must drive the CE# and OE# pins LOW and drive WE# high for a valid read operation to take place. The BYTE# pin determines whether the device outputs array data in words (DQ[15:0]) or in bytes (DQ[7:0]).

The HY29LV400 is automatically set for reading array data after device power-up and after a hardware reset to ensure that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data, and the device remains enabled for read accesses until the command register contents are altered.

This device features an Erase Suspend mode. While in this mode, the host may read the array data from any sector of memory that is not marked for erasure. If the host reads from an address within an erase-suspended (or erasing) sector, or while the device is performing a byte or word program operation, the device outputs status data instead of array data. After completing an Automatic Program or Automatic Erase algorithm within a sector, that sector automatically returns to the read array data mode. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception noted above.

The host must issue a hardware reset or the software reset command to return a sector to the read array data mode if DQ[5] goes high during a program or erase cycle, or to return the device to the read array data mode while it is in the Electronic ID mode.

Table 1. HY29LV400T (Top Boot Block) Memory Array Organization

Sector	Size (KB/KW)	Sector Address [1]						Byte Mode Address Range [2, 3]	Word Mode Address Range [2, 3]
		A[17]	A[16]	A[15]	A[14]	A[13]	A[12]		
S0	64/32	0	0	0	X	X	X	0x00000 - 0x0FFFF	0x00000 - 0x07FFF
S1	64/32	0	0	1	X	X	X	0x10000 - 0x1FFFF	0x08000 - 0x0FFFF
S2	64/32	0	1	0	X	X	X	0x20000 - 0x2FFFF	0x10000 - 0x17FFF
S3	64/32	0	1	1	X	X	X	0x30000 - 0x3FFFF	0x18000 - 0x1FFFF
S4	64/32	1	0	0	X	X	X	0x40000 - 0x4FFFF	0x20000 - 0x27FFF
S5	64/32	1	0	1	X	X	X	0x50000 - 0x5FFFF	0x28000 - 0x2FFFF
S6	64/32	1	1	0	X	X	X	0x60000 - 0x6FFFF	0x30000 - 0x37FFF
S7	32/16	1	1	1	0	X	X	0x70000 - 0x77FFF	0x38000 - 0x3BFFF
S8	8/4	1	1	1	1	0	0	0x78000 - 0x79FFF	0x3C000 - 0x3CFFF
S9	8/4	1	1	1	1	0	1	0x7A000 - 0x7BFFF	0X3D000 - 0x3DFFF
S10	16/8	1	1	1	1	1	X	0x7C000 - 0x7FFFF	0x3E000 - 0x3FFFF

Notes:
1. 'X' indicates don't care.
2. '0xN. . . N' indicates an address in hexadecimal notation.
3. The address range in byte mode is A[17:0, -1]. The address range in word mode is A[17:0].

Table 2. HY29LV400B (Bottom Boot Block) Memory Array Organization

Sector	Size (KB/KW)	Sector Address [1]						Byte Mode Address Range [2, 3]	Word Mode Address Range [2, 3]
		A[17]	A[16]	A[15]	A[14]	A[13]	A[12]		
S0	16/8	0	0	0	0	0	X	0x00000 - 0x03FFF	0x00000 - 0x01FFF
S1	8/4	0	0	0	0	1	0	0x04000 - 0x05FFF	0x02000 - 0x02FFF
S2	8/4	0	0	0	0	1	1	0x06000 - 0x07FFF	0X03000 - 0x03FFF
S3	32/16	0	0	0	1	X	X	0x08000 - 0x0FFFF	0x04000 - 0x07FFF
S4	64/32	0	0	1	X	X	X	0x10000 - 0x1FFFF	0x08000 - 0x0FFFF
S5	64/32	0	1	0	X	X	X	0x20000 - 0x2FFFF	0x10000 - 0x17FFF
S6	64/32	0	1	1	X	X	X	0x30000 - 0x3FFFF	0x18000 - 0x1FFFF
S7	64/32	1	0	0	X	X	X	0x40000 - 0x4FFFF	0x20000 - 0x27FFF
S8	64/32	1	0	1	X	X	X	0x50000 - 0x5FFFF	0x28000 - 0x2FFFF
S9	64/32	1	1	0	X	X	X	0x60000 - 0x6FFFF	0x30000 - 0x37FFF
S10	64/32	1	1	1	X	X	X	0x70000 - 0x7FFFF	0x38000 - 0x3FFFF

Notes:
1. 'X' indicates don't care.
2. '0xN. . . N' indicates an address in hexadecimal notation.
3. The address range in byte mode is A[17:0, -1]. The address range in word mode is A[17:0].

Table 3. HY29LV400 Normal Bus Operations [1]

Operation	CE#	OE#	WE#	RESET#	Address [2]	DQ[7:0]	DQ[15:8] [3]	
							BYTE# = H	BYTE# = L
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	High-Z
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
CE# Normal Standby	H	X	X	H	X	High-Z	High-Z	High-Z
CE# Deep Standby	V_{CC} ± 0.3V	X	X	V_{CC} ± 0.3V	X	High-Z	High-Z	High-Z
Hardware Reset (Normal Standby)	X	X	X	L	X	High-Z	High-Z	High-Z
Hardware Reset (Deep Standby)	X	X	X	V_{SS} ± 0.3V	X	High-Z	High-Z	High-Z

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care (L or H), D_{OUT} = Data Out, D_{IN} = Data In. See DC Characteristics for voltage levels.
2. Address is A[17:0, -1] in Byte Mode and A[17:0] in Word Mode.
3. DQ[15] is the A[-1] input in Byte Mode (BYTE# = L).

Table 4. HY29LV400 Bus Operations Requiring High Voltage [1, 2]

Operation [3]		CE#	OE#	WE#	RESET#	A[19:12]	A[9]	A[6]	A[1]	A[0]	DQ[7:0]	DQ[15:8]	
												BYTE# = H	BYTE# = L [5]
Sector Protect		L	H	L	V_{ID}	SA [4]	X	L	H	L	D_{IN}/D_{OUT}	X	X
Sector Unprotect		L	H	L	V_{ID}	X	X	H	H	L	D_{IN}/D_{OUT}	X	X
Temporary Sector Unprotect [6]		--	--	--	V_{ID}	--	--	--	--	--	--	--	--
Manufacturer Code		L	L	H	H	X	V_{ID}	L	L	L	0xAD	X	High-Z
Device Code	HY29LV400B	L	L	H	H	X	V_{ID}	L	L	H	0xBA	0x22	High-Z
	HY29LV400T										0xB9		
Sector Protection Verification		L	L	H	H	SA [4]	V_{ID}	L	H	L	0x00 = Unprotected 0x01 = Protected	X	High-Z

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care (L OR H). See DC Characteristics for voltage levels.
2. Address bits not specified are Don't Care.
3. See text and for additional information.
4. SA = Sector Address. See Tables 1 and 2.
5. DQ[15] is the A[-1] input in Byte Mode (BYTE# = L).
6. Normal read, write and output disable operations are used in this mode. See Table 3.

Write Operation

Certain operations, including programming data and erasing sectors of memory, require the host to write a command or command sequence to the HY29LV400. Writes to the device are performed by placing the byte or word address on the device's address inputs while the data to be written is input on DQ[15:0] (BYTE# = High) or DQ[7:0] (BYTE# = Low). The host system must drive the CE# and WE# pins Low and drive OE# High for a valid write operation to take place. All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first.

The "Device Commands" section of this data sheet provides details on the specific device commands implemented in the HY29LV400.

Standby Operation

When the system is not reading or writing to the device, it can place the HY29LV400 in the Standby mode. In this mode, current consumption is greatly reduced, and the data bus outputs are placed in the high impedance state, independent of the OE# input. The Standby mode can be invoked using two methods.

The device enters the CE# Deep Standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3V$. Note that this is a more restricted voltage range than V_{IH} . If both CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3V$, the device will be in the CE# Normal Standby mode, but the standby current will be greater.

The device enters the RESET# Deep Standby mode when the RESET# pin is held at $V_{SS} \pm 0.3V$. If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3V$, the device will be in the RESET# Normal Standby mode, but the standby current will be greater. See Reset Operation for additional information.

The device requires standard access time (t_{CE}) for read access when the device is in either of the standby modes, before it is ready to read data.

> **Note**: If the device is deselected during an erase or programming operation, it continues to draw active current until the operation is completed.

Sleep Mode

The sleep mode automatically minimizes device power consumption. This mode is automatically entered when addresses remain stable for t_{ACC} + 30 ns (typical) and is independent of the state of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

> **NOTE:** Sleep mode is entered only when the device is in Read mode. It is not entered if the device is executing an automatic algorithm, if it is in Erase Suspend mode, or during receipt of a command sequence.

Output Disable Operation

When the OE# input is at V_{IH}, output data from the device is disabled and the data bus pins are placed in the high impedance state.

Reset Operation

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for the minimum specified period, the device immediately terminates any operation in progress, tri-states the data bus pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. If an operation was interrupted by the assertion of RESET#, it should be reinitiated once the device is ready to accept another command sequence to ensure data integrity.

Current is reduced for the duration of the RESET# pulse as described in the Standby Operation section above.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains Low (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Automatic Algorithms). The system can thus monitor RY/BY# to determine when the reset operation completes, and can perform a read or write operation t_{RB} after RY/BY# goes High. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is High), the reset operation is completed within a time of t_{RP}. In this case, the host can perform a read or write operation t_{RH} after the RESET# pin returns High .

The RESET# pin may be tied to the system reset signal. Thus, a system reset would also reset the device, enabling the system to read the boot-up firmware from the Flash memory.

Sector Protect Operation

The hardware sector protection feature disables both program and erase operations in any sector or combination of sectors. This function can be implemented either in-system or by using programming equipment.

The Sector Protect procedure requires V_{ID} on the RESET# pin and uses standard microprocessor bus cycle timing to implement sector protection. The flow chart in Figure 1 illustrates the algorithm.

The HY29LV400 is shipped with all sectors unprotected. It is possible to determine whether a sector is protected or unprotected. See the Electronic ID Mode section for details.

Sector Unprotect Operation

The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. This function can be implemented either in-system or by using programming equipment. Note that to unprotect any sector, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. Also, the unprotect procedure will cause all sectors to become unprotected, thus, sectors that require protection must be protected again after the unprotect procedure is run.

The Sector Unprotect procedure requires V_{ID} on the RESET# pin and uses standard microprocessor bus cycle timing to implement sector unprotection. The flow chart in Figure 2 illustrates the algorithm.

Temporary Sector Unprotect Operation

This feature allows temporary unprotection of previously protected sectors to allow changing the data in-system. Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. While in this mode, formerly protected sectors can be programmed or erased by invoking the appropriate commands (see Device Commands section). Once V_{ID} is removed from RESET#, all the previously protected sectors are protected again. Figure 3 illustrates the algorithm.

Electronic ID Operation (High Voltage Method)

The Electronic ID mode provides manufacturer and device identification and sector protection verification through codes output on DQ[15:0]. This mode is intended primarily for programming equipment to automatically match a device to be pro-

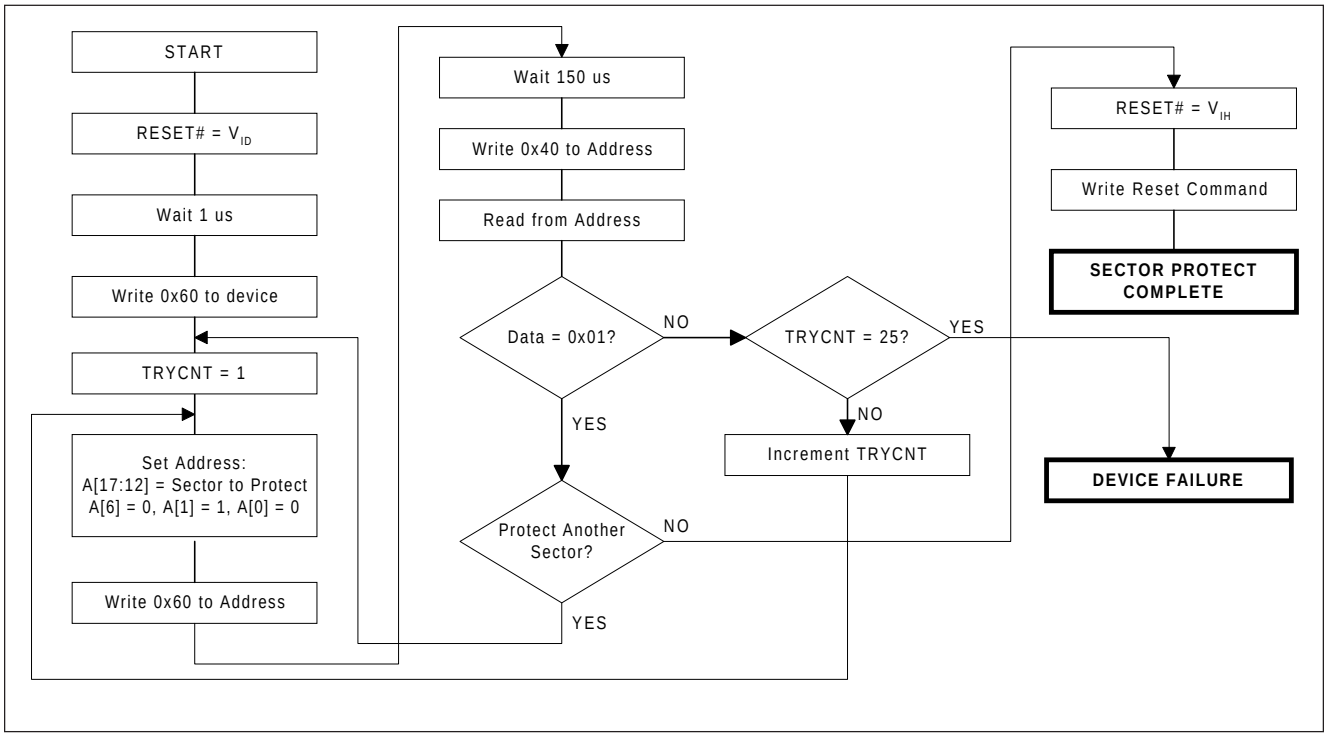


Figure 1. Sector Protect Algorithm

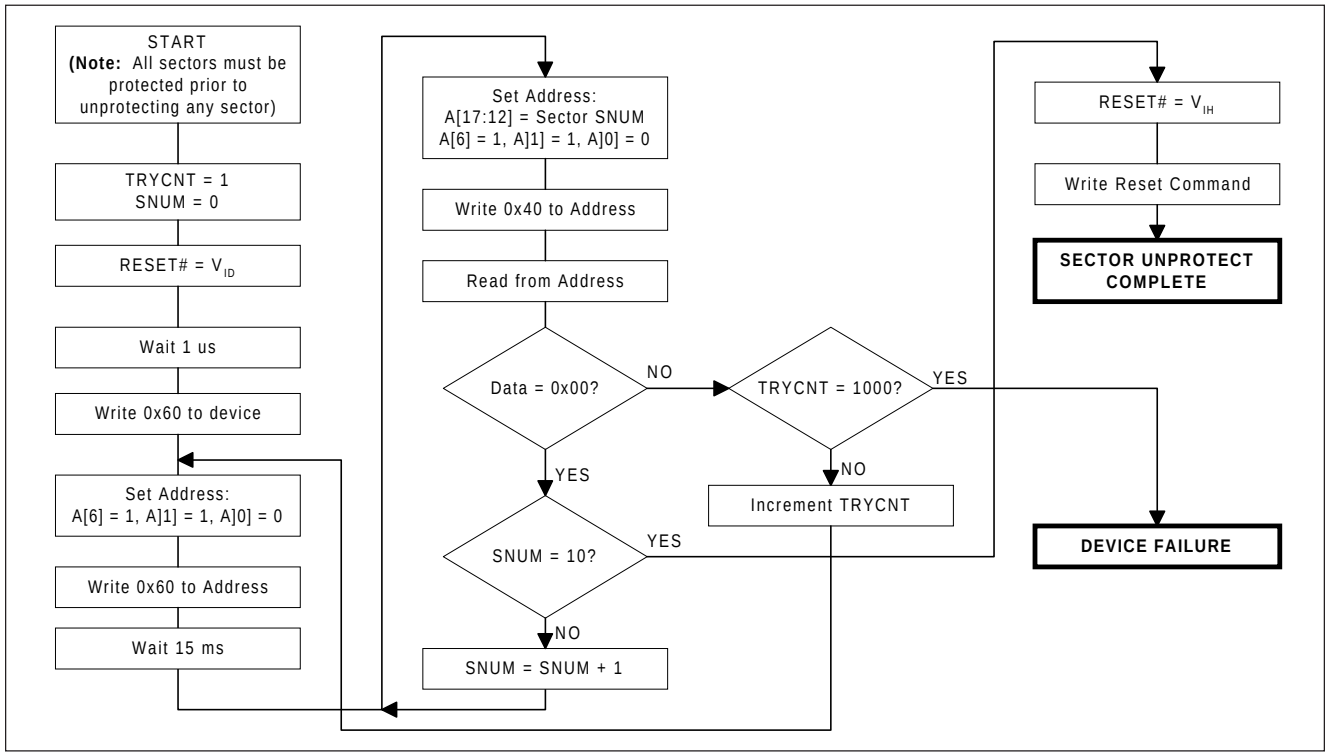


Figure 2. Sector Unprotect Algorithm

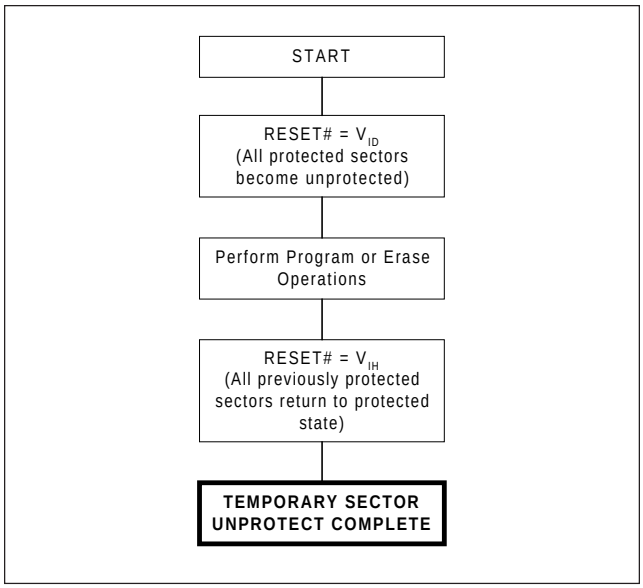


Figure 3. Temporary Sector Unprotect Algorithm

grammed with its corresponding programming algorithm.

Two methods are provided for accessing the Electronic ID data. The first requires V_{ID} on address pin A[9], with additional requirements for obtaining specific data items listed in Table 4. The Electronic ID data can also be obtained by the host through specific commands issued via the command register, as described in the 'Device Commands' section of this data sheet.

While in the high-voltage Electronic ID mode, the system may read at specific addresses to obtain certain device identification and status information:

- A read cycle at address 0xXXX00 retrieves the manufacturer code.
- A read cycle at address 0xXXX01 in Word mode or 0xXXX02 in Byte mode returns the device code.
- A read cycle containing a sector address (SA) in A[17:12] and the address 0x02 in Word mode or 0x04 in Byte mode, returns 0x01 if that sector is protected, or 0x00 if it is unprotected.

DEVICE COMMANDS

Device operations are initiated by writing designated address and data *command sequences* into the device. Addresses are latched on the falling edge of WE# or CE#, whichever happens later. Data is latched on the rising edge of WE# or CE#, whichever happens first.

A command sequence is composed of one, two or three of the following sub-segments: an *unlock cycle*, a *command cycle* and a *data cycle*. Table 5 summarizes the composition of the valid command sequences implemented in the HY29LV400, and these sequences are fully described in Table 6 and in the sections that follow.

Writing incorrect address and data values or writing them in the improper sequence resets the HY29LV400 to the Read mode.

Reading Data

The device automatically enters the Read mode after device power-up, after the RESET# input is asserted and upon the completion of certain commands. Commands are not required to retrieve data in this mode. See Read Operation section for additional information.

Reset Command

Writing the Reset command resets the sectors to the Read or Erase-Suspend mode. Address bits are don't cares for this command.

As described above, a Reset command is not normally required to begin reading array data. However, a Reset command must be issued in order to read array data in the following cases:

- If the device is in the Electronic ID mode, a Reset command must be written to return to the Read mode. If the device was in the Erase Suspend mode when the device entered the Electronic ID mode, writing the Reset command returns the device to the Erase Suspend mode.

  Note: When in the Electronic ID bus operation mode, the device returns to the Read mode when V_{ID} is removed from the A[9] pin. The Reset command is not required in this case.

- If DQ[5] (Exceeded Time Limit) goes High during a program or erase operation, a Reset command must be invoked to return the sectors to the Read mode (or to the Erase Suspend mode if the device was in Erase Suspend when the Program command was issued).

The Reset command may also be used to abort certain command sequences:

- In a Sector Erase or Chip Erase command sequence, the Reset command may be written at any time before erasing actually begins, including, for the Sector Erase command, between the cycles that specify the sectors to be erased (see Sector Erase command description). This aborts the command and resets the device to the Read mode. Once erasure begins, however, the device ignores the Reset command until the operation is complete.

- In a Program command sequence, the Reset command may be written between the sequence cycles before programming actually begins. This aborts the command and resets the device to the Read mode, or to the Erase Suspend mode if the Program command sequence is written while the device is in the Erase Suspend mode. Once programming begins, however, the device ignores the Reset command until the operation is complete.

Table 5. Composition of Command Sequences

Command Sequence	Number of Bus Cycles		
	Unlock	Command	Data
Reset	0	1	0
Read	0	0	Note 1
Byte/Word Program	2	1	1
Unlock Bypass	2	1	0
Unlock Bypass Reset	0	1	1
Unlock Bypass Byte/Word Program	0	1	1
Chip Erase	4	1	1
Sector Erase	4	1	1 (Note 2)
Erase Suspend	0	1	0
Erase Resume	0	1	0
Electronic ID	2	1	Note 3

Notes:
1. Any number of Flash array read cycles are permitted.
2. Additional data cycles may follow. See text.
3. Any number of Electronic ID read cycles are permitted.

Table 6. HY29LV400 Command Sequences

Command Sequence		Write Cycles	Bus Cycles [1, 2, 3] First Add	First Data	Second Add	Second Data	Third Add	Third Data	Fourth Add	Fourth Data	Fifth Add	Fifth Data	Sixth Add	Sixth Data
Read		0	RA	RD										
Reset [7]		1	XXX	F0										
Normal Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte		AAA		555		AAA							
Unlock Bypass	Word	3	555	AA	2AA	55	555	20						
	Byte		AAA		555		AAA							
Unlock Bypass Reset		2	XXX	90	XXX	00								
Unlock Bypass Program [8]	Word	2	XXX	A0	PA	PD								
	Byte													
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte		AAA		555		AAA		AAA		555			
Erase Suspend [4]		1	XXX	B0										
Erase Resume [5]		1	XXX	30										
Electronic ID [6] Manufacturer Code	Word	3	555	AA	2AA	55	555	90	X00	AD				
	Byte		AAA		555		AAA							
Device Code	Word	3	555	AA	2AA	55	555	90	X01	22B9 (Top Boot), 22BA (Bottom Boot)				
	Byte		AAA		555		AAA		X02	B9 (Top Boot), BA (Bottom Boot)				
Sector Protect Verify	Word	3	555	AA	2AA	55	555	90	(SA)X02	00 = Unprotected Sector 01 = Protected Sector				
	Byte		AAA		555		AAA		(SA)X04					

Legend:
X = Don't Care
RA = Memory address of data to be read
RD = Data read from location RA during the read operation
PA = Address of the data to be programmed
PD = Data to be programmed at address PA
SA = Sector address of sector to be erased or verified (see Note 3 and Tables 1 and 2).

Notes:
See next page for notes.

Notes for Table 6:

1. All values are in hexadecimal. DQ[15:8] are don't care for unlock and command cycles.
2. All bus cycles are write operations unless otherwise noted.
3. Address is A[10:0] in Word mode and A[10:0, -1] in Byte mode. A[17:11] are don't care except as follows:
   - For RA and PA, A[17:11] are the upper address bits of the byte to be read or programmed.
   - For the sixth cycle of Sector Erase, SA = A[17:12] are the sector address of the sector to be erased.
   - For the fourth cycle of Sector Protect Verify, SA = A[17:12] are the sector address of the sector to be verified.
4. The Erase Suspend command is valid only during a sector erase operation. The system may read and program in non-erasing sectors, or enter the Electronic ID mode, while in the Erase Suspend mode.
5. The Erase Resume command is valid only during the Erase Suspend mode.
6. The fourth bus cycle is a read cycle.
7. The command is required only to return to the Read mode when the device is in the Electronic ID command mode. It must also be issued to return to read mode if DQ[5] goes High during a program or erase operation. It is not required for normal read operations.
8. The Unlock Bypass command is required prior to the Unlock Bypass Program command.

■ The Reset command may be written between the cycles in an Electronic ID command sequence to abort that command. As described above, once in the Electronic ID mode, the Reset command *must* be written to return to the array Read mode.

Program Command

The system programs the device a word or byte at a time by issuing the appropriate four-cycle program command sequence as shown in Table 6. The sequence begins by writing two unlock cycles, followed by the program setup command and, lastly, the program address and data. This initiates the Automatic Program algorithm which automatically provides internally generated program pulses and verifies the programmed cell margin. The host is not required to provide further controls or timings during this operation. When the Automatic Program algorithm is complete, the device returns to the array Read mode (or to the Erase Suspend mode if the device was in Erase Suspend when the Program command was issued). Several methods are provided to allow the host to determine the status of the programming operation, as described in the Write Operation Status section.

Commands written to the device during execution of the Automatic Program algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. To ensure data integrity, the aborted Program command sequence should be reinitiated once the reset operation is complete.

Programming is allowed in any sequence. Only erase operations can convert a stored "0" to a "1". Thus, a bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set DQ[5] to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0".

Figure 4 illustrates the programming procedure.

Unlock Bypass/Bypass Program/Bypass Reset Commands

Unlock bypass provides a faster method for the host system to program the device. As shown in Table 6, the Unlock Bypass command sequence consists of two unlock write cycles followed by a third write cycle containing the Unlock Bypass command, 0x20. In the Unlock Bypass mode, a two-cycle Unlock Bypass Program command sequence is used instead of the standard four-cycle Program sequence to invoke a programming operation. The first cycle in this sequence contains the Unlock Bypass Program command, 0xA0, and the second cycle specifies the program address and data, thus eliminating the initial two unlock cycles required in the standard Program command sequence Additional data is programmed in the same manner.

During the Unlock Bypass mode, only the Unlock Bypass program and Unlock Bypass Reset commands are valid. To exit the Unlock Bypass mode, the host must issue the two-cycle Unlock Bypass Reset command sequence shown in Table 6. The device then returns to the array Read mode.

Chip Erase Command

The Chip Erase command sequence consists of two unlock cycles, followed by a set-up command, two additional unlock cycles and then the Chip Erase command. This sequence invokes the Au-

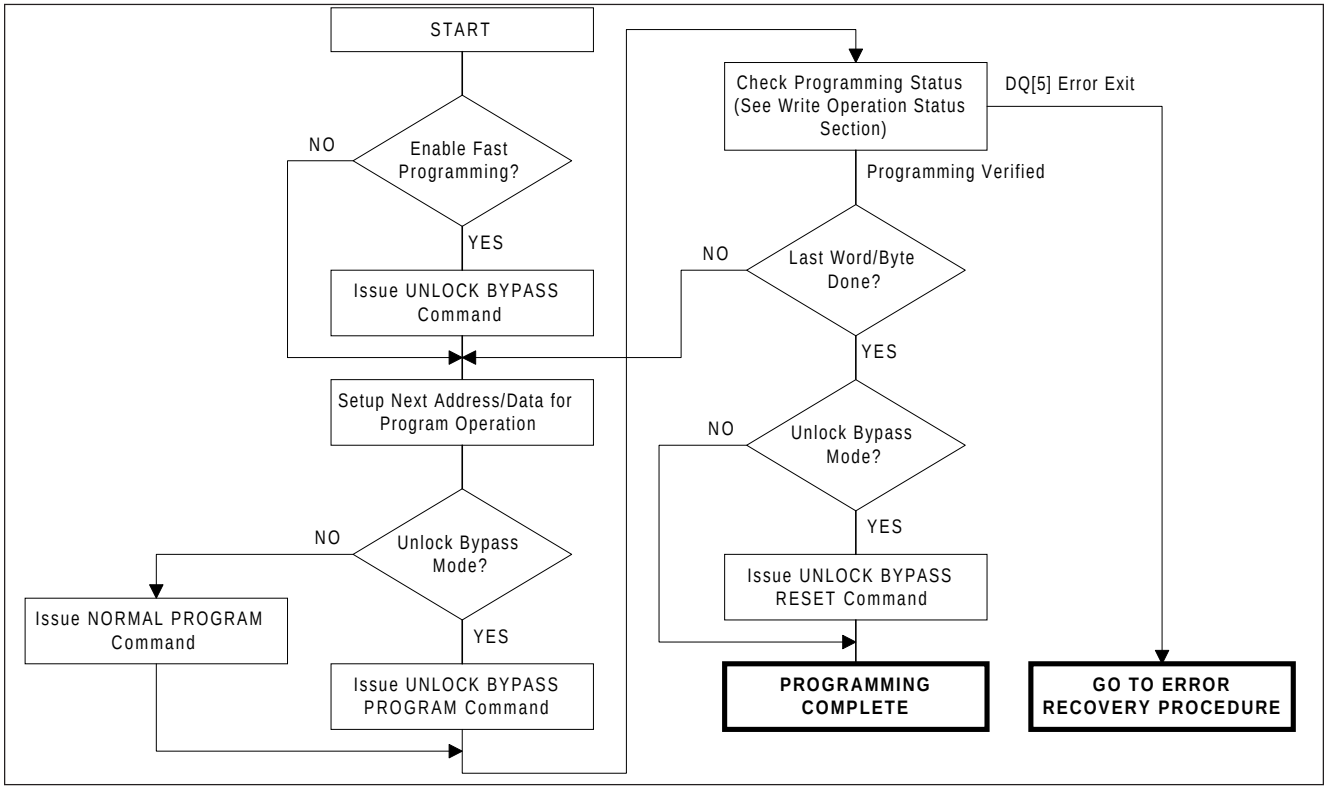


Figure 4. Normal and Unlock Bypass Programming Procedures

tomatic Erase algorithm that automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The host system is not required to provide any controls or timings during these operations.

Commands written to the device during execution of the Automatic Erase algorithm are ignored. Note that a hardware reset immediately terminates the chip erase operation. To ensure data integrity, the aborted Chip Erase command sequence should be reissued once the reset operation is complete.

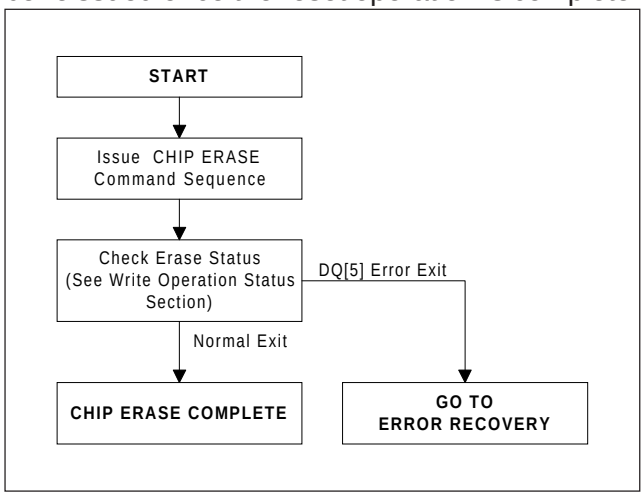


Figure 5. Chip Erase Procedure

When the Automatic Erase algorithm is complete, the device returns to the array Read mode. Several methods are provided to allow the host to determine the status of the erase operation, as described in the Write Operation Status section.

Figure 5 illustrates the chip erase procedure.

Sector Erase Command

The Sector Erase command sequence consists of two unlock cycles, followed by the Erase command, two additional unlock cycles and then the sector erase data cycle, which specifies the sector to be erased. As described later in this section, multiple sectors can be specified for erasure with a single command sequence. During sector erase, all specified sectors are erased sequentially. The data in sectors not specified for erasure, as well as the data in any protected sectors, even if specified for erasure, is not affected by the sector erase operation.

The Sector Erase command sequence starts the Automatic Erase algorithm, which preprograms and verifies the specified unprotected sectors for an all zero data pattern prior to electrical erase. The device then provides the required number of

internally generated erase pulses and verifies cell erasure within the proper cell margins. The host system is not required to provide any controls or timings during these operations.

After the sector erase data cycle (the sixth bus cycle) of the command sequence is issued, a sector erase time-out of 50 µs (min), measured from the rising edge of the final WE# pulse in that bus cycle, begins. During this time-out window, an additional sector erase data cycle, specifying the sector address of another sector to be erased, may be written into an internal sector erase buffer. This buffer may be loaded in any sequence, and the number of sectors specified may be from one sector to all sectors. The only restriction is that the time between these additional data cycles must be less than 50 µs, otherwise erasure may begin before the last data cycle is accepted. To ensure that all data cycles are accepted, it is recommended that host processor interrupts be disabled during the time that the additional cycles are being issued and then be re-enabled afterwards.

If all sectors specified for erasing are protected, the device returns to reading array data after approximately 100 µs. If at least one specified sector is not protected, the erase operation erases the unprotected sectors, and ignores the command for the sectors that are protected.

The system can monitor DQ[3] to determine if the 50 µs sector erase time-out has expired, as described in the Write Operation Status section. If the time between additional sector erase data cycles can be insured to be less than the time-out, the system need not monitor DQ[3].

Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must then rewrite the command sequence, including any additional sector erase data cycles. Once the sector erase operation itself has begun, only the Erase Suspend command is valid. All other commands are ignored.

As for the Chip Erase command, note that a hardware reset immediately terminates the sector erase operation. To ensure data integrity, the aborted Sector Erase command sequence should be reissued once the reset operation is complete.

When the Automatic Erase algorithm terminates, the device returns to the array Read mode. Several methods are provided to allow the host to determine the status of the erase operation, as described in the Write Operation Status section.

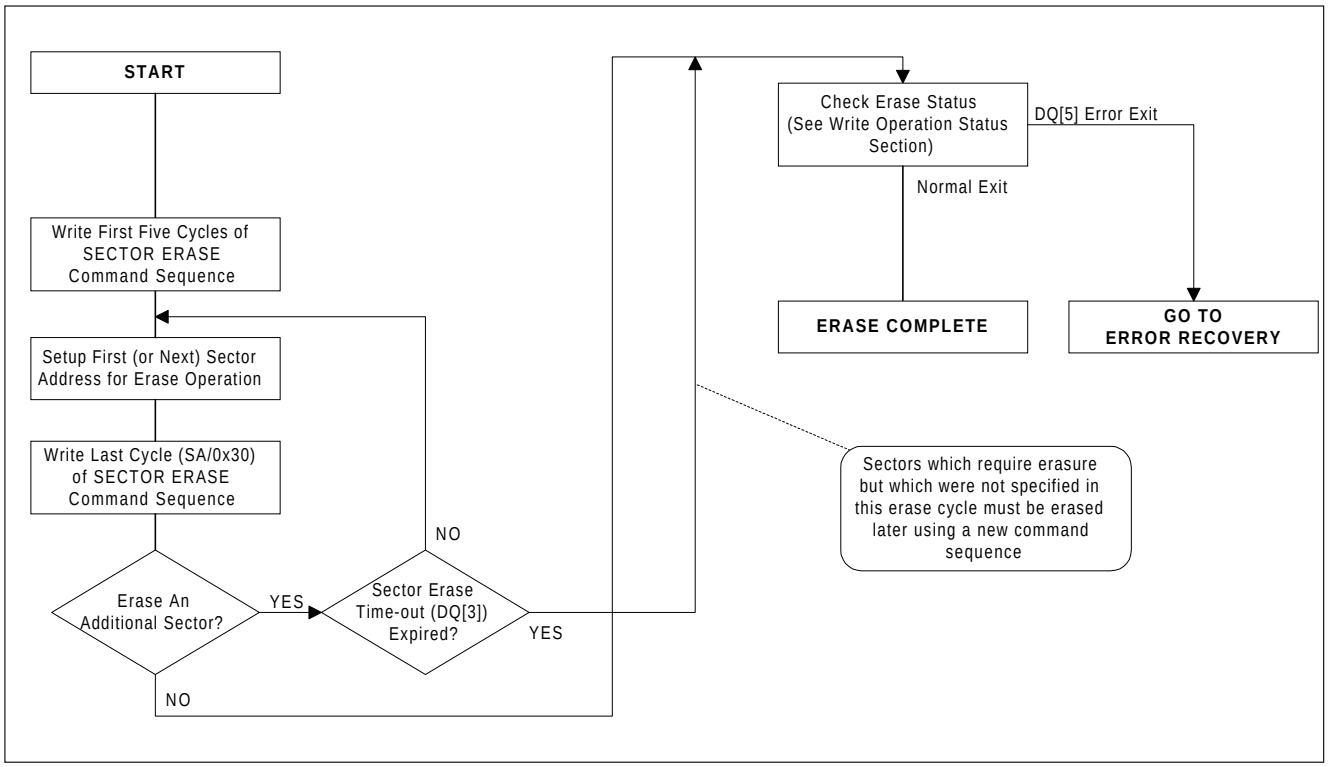


Figure 6. Sector Erase Procedure

Figure 6 illustrates the Sector Erase procedure.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation to read data from, or program data in, any sector not being erased. The command causes the erase operation to be suspended in all sectors specified for erasure. This command is valid only during the sector erase operation, including during the 50 µs time-out period at the end of the command sequence, and is ignored if it is issued during chip erase or programming operations.

The HY29LV400 requires a maximum of 20 µs to suspend the erase operation if the Erase Suspend command is issued during sector erasure. However, if the command is written during the time-out, the time-out is terminated and the erase operation is suspended immediately. Once the erase operation has been suspended, the system can read array data from or program data to any sector not specified for erasure. Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ[7:0]. The host can use DQ[7], or DQ[6] and DQ[2] together, to determine if a sector is actively erasing or is erase-suspended. See the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the host can initiate another programming operation (or read operation) within non-suspended sectors. The host can determine the status of a program operation during the Erase-Suspended state just as in the standard programming operation.

The host may also write the Electronic ID command sequence when the device is in the Erase Suspend mode. The device allows reading Electronic ID codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the Electronic ID mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See Electronic ID Mode section for more information.

The system must write the Erase Resume command to exit the Erase Suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Electronic ID Command

The Electronic ID mode provides manufacturer and device identification and sector protection verification through identifier codes output on DQ[7:0]. This mode is intended primarily for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm.

Two methods are provided for accessing the Electronic ID data. The first requires V_{ID} on address pin A[9], as described previously in the Device Operations section.

The Electronic ID data can also be obtained by the host by invoking the Electronic ID command, as shown in Table 6. This method does not require V_{ID}. The Electronic ID command sequence may be issued while the device is in the Read mode or in the Erase Suspend Read mode, that is, except while programming or erasing.

The Electronic ID command sequence is initiated by writing two unlock cycles, followed by the Electronic ID command. The device then enters the Electronic ID mode, and the system may read at any address any number of times, without initiating another command sequence.

- A read cycle at address 0xXXX00 retrieves the manufacturer code.
- A read cycle at address 0xXXX01 in Word mode or 0xXXX02 in Byte mode returns the device code.
- A read cycle containing a sector address (SA) in A[17:12] and the address 0x02 in A[7:0] in Word mode (or 0x04 in A[6:0, -1] in Byte mode) returns 0x01 if that sector is protected, or 0x00 if it is unprotected.

The system must write the Reset command to exit the Electronic ID mode and return to reading array data.

Table 7. Write and Erase Operation Status Summary

Mode	Operation	DQ[7] [1]	DQ[6]	DQ[5]	DQ[3]	DQ[2] [1]	RY/BY#
Normal	Programming in progress	DQ[7]#	Toggle	0/1 [2]	N/A	N/A	0
	Programming completed	Data	Data [4]	Data	Data	Data	1
	Erase in progress	0	Toggle	0/1 [2]	1 [3]	Toggle	0
	Erase completed [5]	Data	Data [4]	Data	Data	Data [4]	1
Erase Suspend	Read within erase suspended sector	1	No toggle	0	N/A	Toggle	1
	Read within non-erase suspended sector	Data	Data	Data	Data	Data	1
	Programming in progress [6]	DQ[7]#	Toggle	0/1 [2]	N/A	N/A	0
	Programming completed [6]	Data	Data [4]	Data	Data	Data	1

Notes:
1. A valid address is required when reading status information. See text for additional information.
2. DQ[5] status switches to a '1' when a program or erase operation exceeds the maximum timing limit.
3. A '1' during sector erase indicates that the 50 µs time-out has expired and active erasure is in progress. DQ[3] is not applicable to the chip erase operation.
4. Equivalent to 'No Toggle' because data is obtained in this state.
5. Data (DQ[7:0]) = 0xFF immediately after erasure.
6. Programming can be done only in a non-suspended sector (a sector not specified for erasure).

WRITE OPERATION STATUS

The HY29LV400 provides a number of facilities to determine the status of a program or erase operation. These are the RY/BY# (Ready/Busy#) pin and certain bits of a status word which can be read from the device during the programming and erase operations. Table 7 summarizes the status indications and further detail is provided in the subsections which follow.

RY/BY# - Ready/Busy#

RY/BY# is an open-drain output pin that indicates whether a programming or erase Automatic Algorithm is in progress or has completed. A pull-up resistor to V_{CC} is required for proper operation. RY/BY# is valid after the rising edge of the final WE# pulse in the corresponding command sequence.

If the output is Low (busy), the device is actively erasing or programming, including programming while in the Erase Suspend mode. If the output is High (ready), the device has completed the operation and is ready to read array data in the normal or Erase Suspend modes, or it is in the Standby mode.

DQ[7] - Data# Polling

The Data# ("Data Bar") Polling bit, DQ[7], indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend mode. Data# Polling is valid after the rising edge of the final WE# pulse in the Program or Erase command sequence.

The system must do a read at the program address to obtain valid programming status information on this bit. While a programming operation is in progress, the device outputs the complement of the value programmed to DQ[7]. When the programming operation is complete, the device outputs the value programmed to DQ[7]. If a program operation is attempted within a protected sector, Data# Polling on DQ[7] is active for approximately 1 µs, then the device returns to reading array data.

The host must read at an address within any non-protected sector specified for erasure to obtain valid erase status information on DQ[7]. During an erase operation, Data# Polling produces a "0" on DQ[7]. When the erase operation is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ[7]. If all sectors selected for erasing are protected, Data# Polling on DQ[7] is active for approximately 100 µs, then the device returns to reading array data. If at least one selected sector is not protected, the erase operation erases the unprotected sectors,

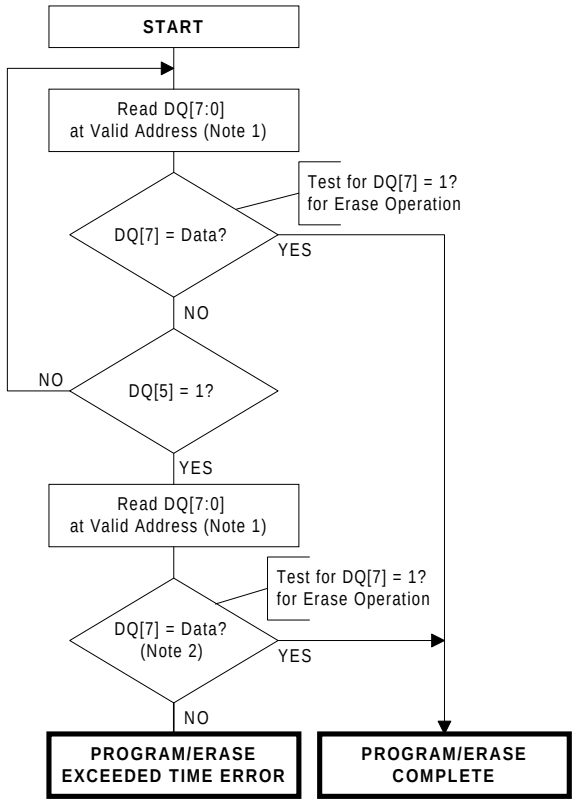
and ignores the command for the specified sectors that are protected.

When the system detects that DQ[7] has changed from the complement to true data (or “0” to “1” for erase), it should do an additional read cycle to read valid data from DQ[7:0]. This is because DQ[7] may change asynchronously with respect to the other data bits while Output Enable (OE#) is asserted low.

Figure 7 illustrates the Data# Polling test algorithm.

DQ[6] - Toggle Bit I

Toggle Bit I on DQ[6] indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the Program or Erase command sequence, including during the sector erase time-out. The system may use either OE# or CE# to control the read cycles.



Notes:
1. During *programming* , the program address. During *sector erase* , an address within any non-protected sector specified for erasure. During *chip erase* , an address within any non-protected sector.
2. Recheck DQ[7] since it may change asynchronously to DQ[5].

Figure 7. Data# Polling Test Algorithm

Successive read cycles at any address during an Automatic Program algorithm operation (including programming while in Erase Suspend mode) cause DQ[6] to toggle. DQ[6] stops toggling when the operation is complete. If a program address falls within a protected sector, DQ[6] toggles for approximately one µs after the program command sequence is written, then returns to reading array data.

While the Automatic Erase algorithm is operating, successive read cycles at any address cause DQ[6] to toggle. DQ[6] stops toggling when the erase operation is complete or when the device is placed in the Erase Suspend mode. The host may use DQ[2] to determine which sectors are erasing or erase-suspended (see below). After an Erase command sequence is written, if all sectors selected for erasing are protected, DQ[6] toggles for approximately 100 µs, then returns to reading array data. If at least one selected sector is not protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

DQ[2] - Toggle Bit II

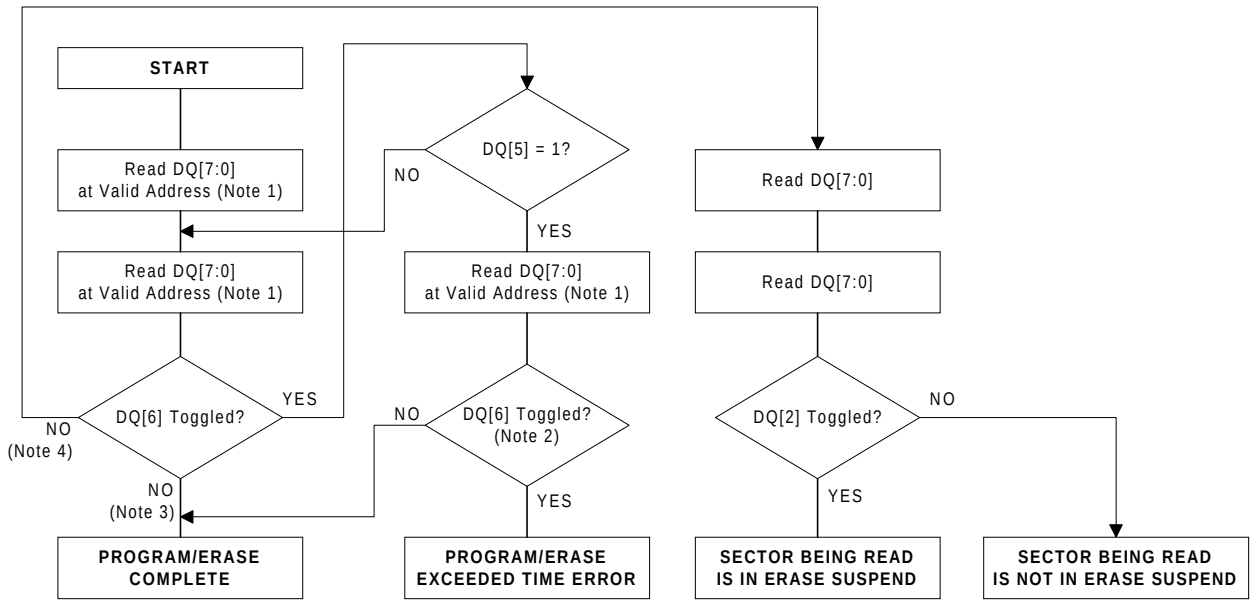
Toggle Bit II, DQ[2], when used with DQ[6], indicates whether a particular sector is actively erasing or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. The device toggles DQ[2] with each OE# or CE# read cycle.

DQ[2] toggles when the host reads at addresses within sectors that have been specified for erasure, but cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ[6], by comparison, indicates whether the device is actively erasing or is in Erase Suspend, but cannot distinguish which sectors are specified for erasure. Thus, both status bits are required for sector and mode information.

Figure 8 illustrates the operation of Toggle Bits I and II.

DQ[5] - Exceeded Timing Limits

DQ[5] is set to a ‘1’ when the program or erase time has exceeded a specified internal pulse count



Notes:
1. During programming, the program address.
   During sector erase, an address within any sector scheduled for erasure.
2. Recheck DQ[6] since toggling may stop at the same time as DQ[5] changes from 0 to 1.
3. Use this path if testing for Program/Erase status.
4. Use this path to test whether sector is in Erase Suspend mode.

Figure 8. Toggle Bit I and II Test Algorithm

limit. This is a failure condition that indicates that the program or erase cycle was not successfully completed. DQ[5] status is valid only while DQ[7] or DQ[6] indicate that the Automatic Algorithm is in progress.

The DQ[5] failure condition will also be signaled if the host tries to program a '1' to a location that is previously programmed to '0', since only an erase operation can change a '0' to a '1'.

For both of these conditions, the host must issue a Reset command to return the device to the Read mode.

DQ[3] - Sector Erase Timer

After writing a Sector Erase command sequence, the host may read DQ[3] to determine whether or not an erase operation has begun. When the sector erase time-out expires and the sector erase operation commences, DQ[3] switches from a '0' to a '1'. Refer to the "Sector Erase Command" section for additional information. Note that the sector erase timer does not apply to the Chip Erase command.

After the initial Sector Erase command sequence is issued, the system should read the status on DQ[7] (Data# Polling) or DQ[6] (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ[3]. If DQ[3] is a '1', the internally controlled erase cycle has begun and all further sector erase data cycles or commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ[3] is a '0', the device will accept a sector erase data cycle to mark an additional sector for erasure. To ensure that the data cycles have been accepted, the system software should check the status of DQ[3] prior to and following each subsequent sector erase data cycle. If DQ[3] is high on the second status check, the last data cycle might not have been accepted.

HARDWARE DATA PROTECTION

The HY29LV400 provides several methods of protection to prevent accidental erasure or programming which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise. These methods are described in the sections that follow.

Command Sequences

Commands that may alter array data require a sequence of cycles as described in Table 6. This provides data protection against inadvertent writes.

Low V_{cc} Write Inhibit

To protect data during V_{CC} power-up and power-down, the device does not accept write cycles when V_{CC} is less than V_{LKO} (typically 2.4 volts). The command register and all internal program/erase circuits are disabled, and the device resets to the Read mode. Writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by asserting any one of the following conditions: OE# = V_{IL} , CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the Read mode on power-up.

Sector Protection

Additional data protection is provided by the HY29LV400’s sector protect feature, described previously, which can be used to protect sensitive areas of the Flash array from accidental or unauthorized attempts to alter the data.

ABSOLUTE MAXIMUM RATINGS [4]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	ºC
T_{BIAS}	Ambient Temperature with Power Applied	-65 to +125	ºC
V_{IN2}	Voltage on Pin with Respect to V_{SS} : VCC [1] A[9], OE#, RESET# [2] All Other Pins [1]	 -0.5 to +4.0 -0.5 to +12.5 -0.5 to V_{CC} +0.5	 V V V
I_{OS}	Output Short Circuit Current [3]	200	mA

Notes:
1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0V for periods of up to 20 ns. See Figure 9. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 10.
2. Minimum DC input voltage on pins A[9], OE#, and RESET# is -0.5 V. During voltage transitions, A[9], OE#, and RESET# may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin A[9] is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output at a time may be shorted to V_{SS}. Duration of the short circuit should be less than one second.
4. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: Commercial Temperature Devices Industrial Temperature Devices	 0 to +70 -40 to +85	 ºC ºC
V_{CC}	Operating Supply Voltage: -55 Version Other Versions	 +3.0 to +3.6 +2.7 to +3.6	 V V

Notes:
1. Recommended Operating Conditions define those limits between which the functionality of the device is guaranteed.

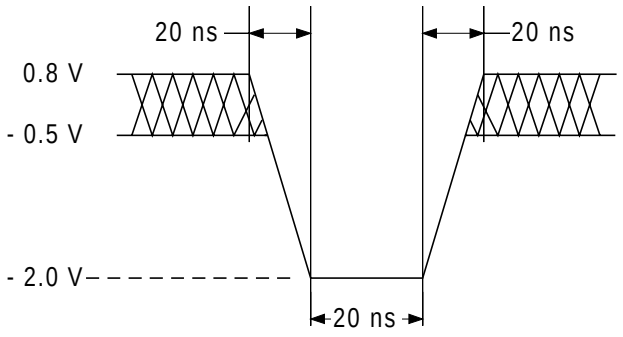


Figure 9. Maximum Undershoot Waveform

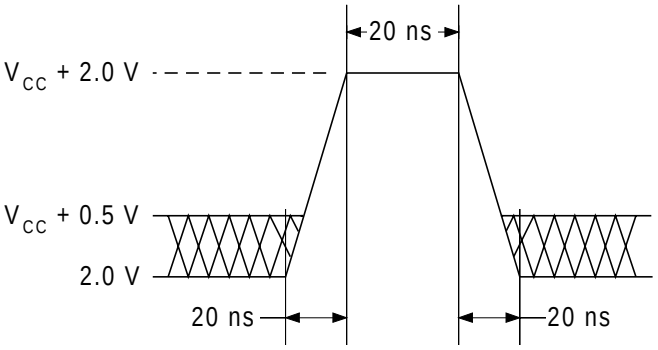


Figure 10. Maximum Overshoot Waveform

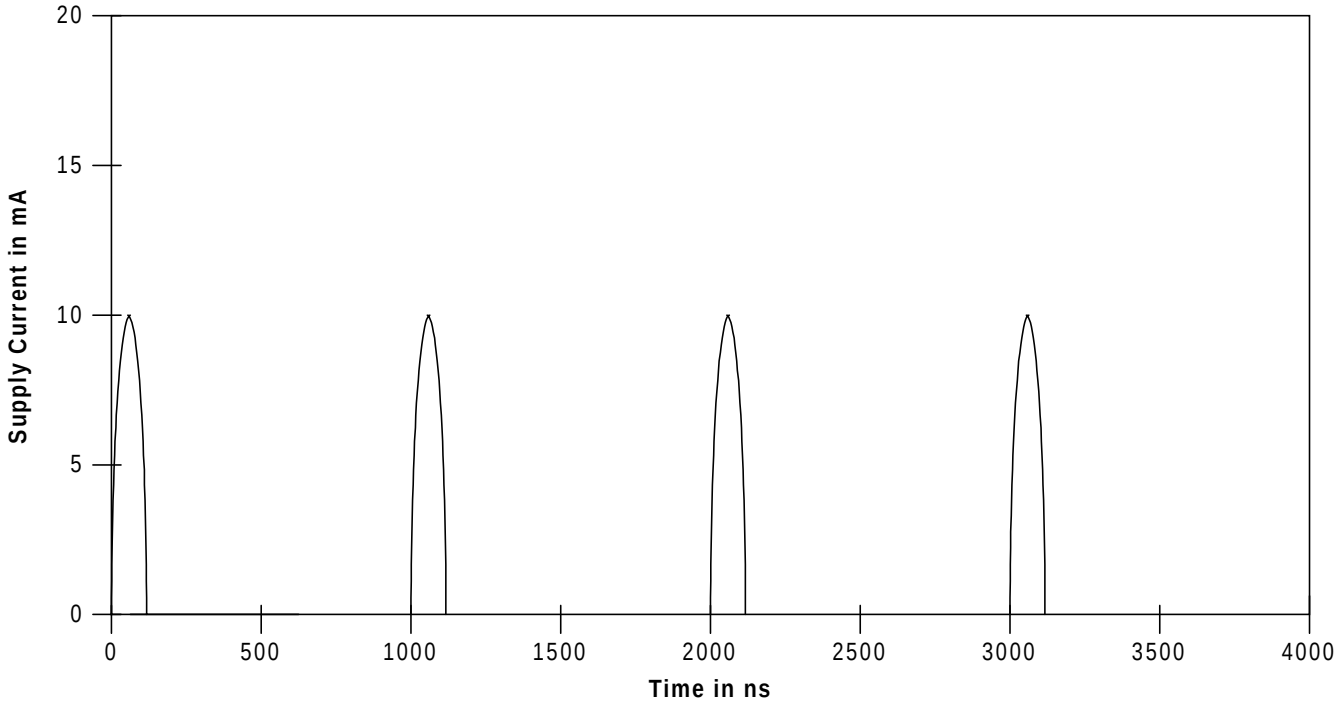
DC CHARACTERISTICS

Parameter	Description	Test Setup [2]		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}				±1.0	µA
I_{LIT}	A[9] Input Load Current	A[9] = 12.5 V				35	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}				±1.0	µA
I_{CC1}	V_{CC} Active Read Current [1]	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		7	12	mA
			1 MHz		2	4	mA
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		7	12	mA
			1 MHz		2	4	mA
I_{CC2}	V_{CC} Active Write Current [3, 4]	CE# = V_{IL}, OE# = V_{IH}			15	30	mA
I_{CC3}	V_{CC} CE# Controlled Deep Standby Current	CE# = V_{CC} ± 0.3 V, RESET# = V_{CC} ± 0.3 V			0.2	5	µA
I_{CC4}	V_{CC} RESET# Controlled Deep Standby Current	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode Current [5,]	V_{IH} = V_{CC} ± 0.3 V, V_{IL} = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC6}	V_{CC} CE# Controlled Normal Standby Current [2]	CE# = RESET# = V_{IH}				1	mA
I_{CC7}	V_{CC} RESET# Controlled Normal Standby Current [2]	RESET# = V_{IL}				1	mA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Electronic ID and Temporary Sector Unprotect	V_{CC} = 3.3V		11.5		12.5	V
V_{OL}	Output Low Voltage	V_{CC} = V_{CC} Min, I_{OL} = 4.0 mA				0.45	V
V_{OH1}	Output High Voltage	V_{CC} = V_{CC} Min, I_{OH} = -2.0 mA		0.85 x V_{CC}			V
V_{OH2}		V_{CC} = V_{CC} Min, I_{OH} = -100 µA		V_{CC} - 0.4			V
V_{LKO}	Low V_{CC} Lockout Voltage [4]			2.3		2.5	V

Notes:
1. The I_{CC} current is listed is typically less than 2 mA/MHz with OE# at V_{IH}. Typical V_{CC} is 3.0 V.
2. All specifications are tested with V_{CC} = V_{CC} Max unless otherwise noted.
3. I_{CC} active while the Automatic Erase or Automatic Program algorithm is in progress.
4. Not 100% tested.
5. Automatic sleep mode is enabled when addresses remain stable for t_{ACC} + 30 ns (typical).

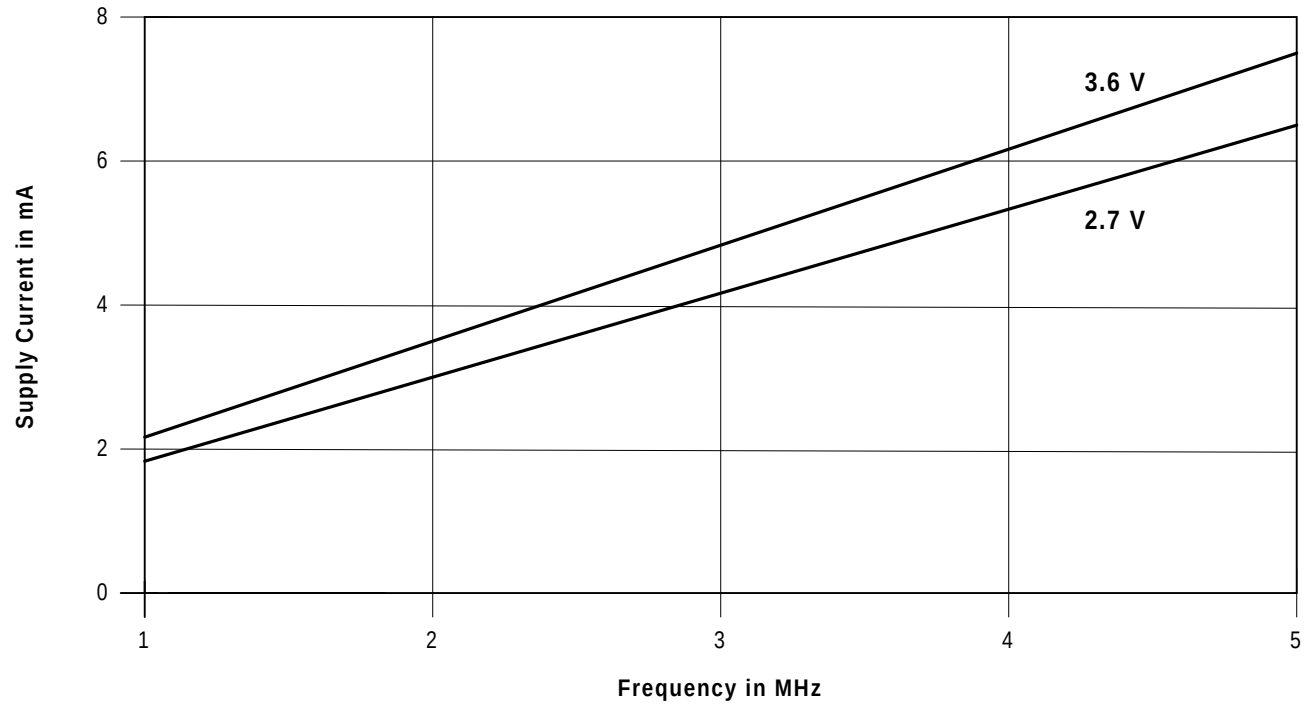
DC CHARACTERISTICS

Zero Power Flash



Note: Addresses are switching at 1 MHz.

Figure 11. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: T = 25 °C.

Figure 12. Typical I_{CC1} Current vs. Frequency

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Centerline is High Impedance State (High Z)

TEST CONDITIONS

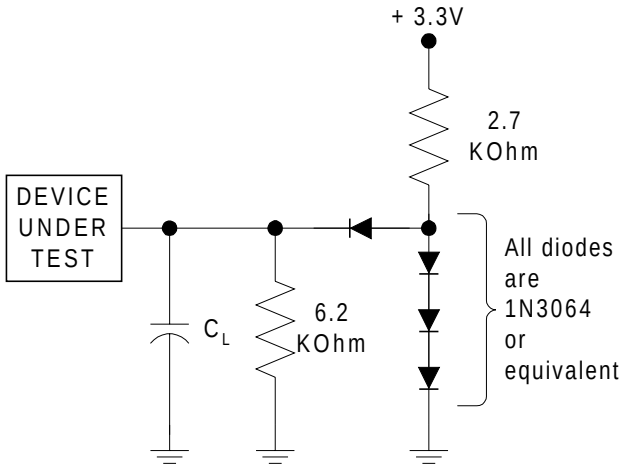


Figure 13. Test Setup

Table 12. Test Specifications

Test Condition	- 55	- 70 - 90	Unit
Output Load	1 TTL Gate		
Output Load Capacitance (C_L)	30	100	pF
Input Rise and Fall Times	5		ns
Input Signal Low Level	0.0		V
Input Signal High Level	3.0		V
Low Timing Measurement Signal Level	1.5		V
High Timing Measurement Signal Level	1.5		V

Note: Timing measurements are made at the reference levels specified above regardless of where the illustrations in the timing diagrams appear to indicate the measurement is made

Figure 14. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Option			Unit
JEDEC	Std					- 55	-70	- 90	
t_{AVAV}	t_{RC}	Read Cycle Time [1]			Min	55	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	55	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	55	70	90	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z [1]			Max	25	25	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		CE# = V_{IL}	Max	30	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z [1]			Max	25	25	30	ns
	t_{OEH}	Output Enable Hold Time [1]	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First [1]			Min	0			ns

Notes:
1. Not 100% tested.

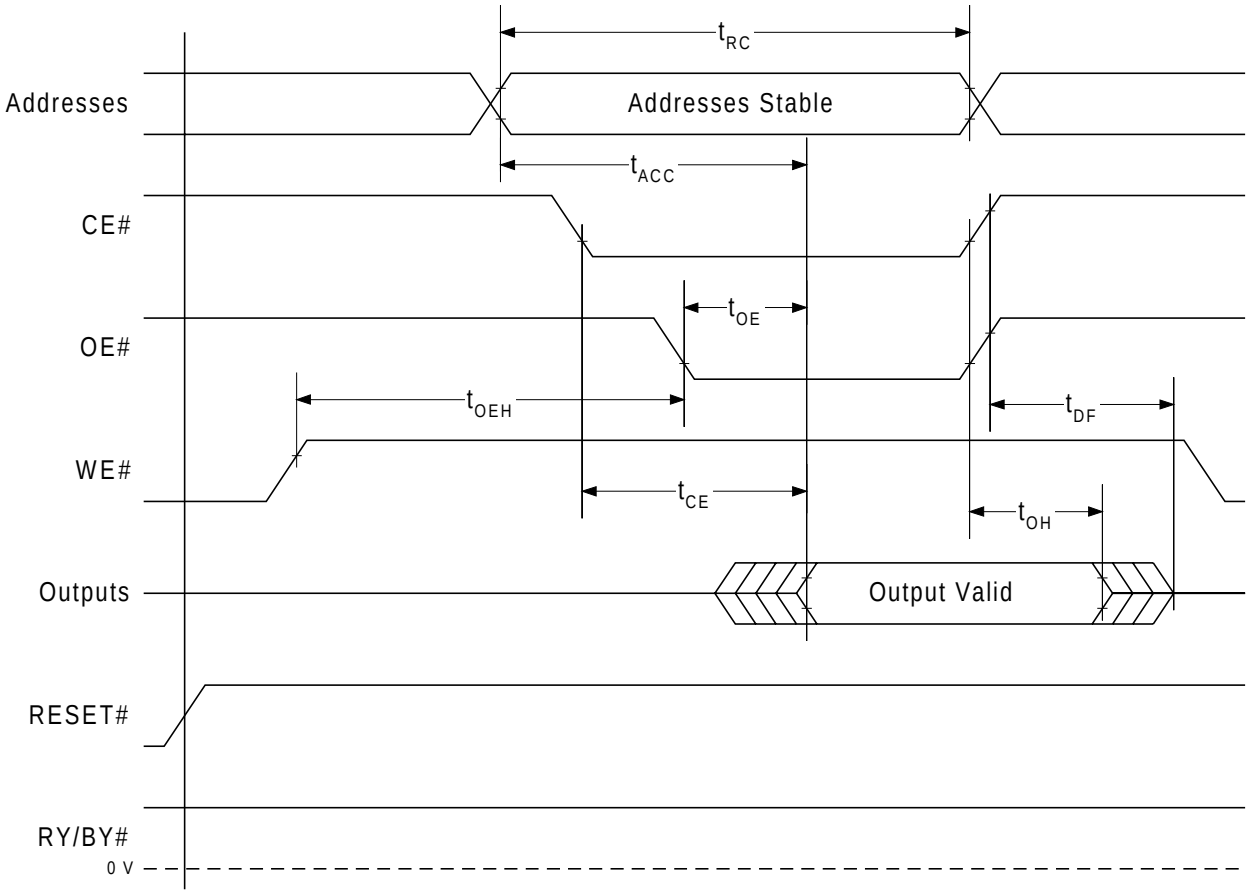


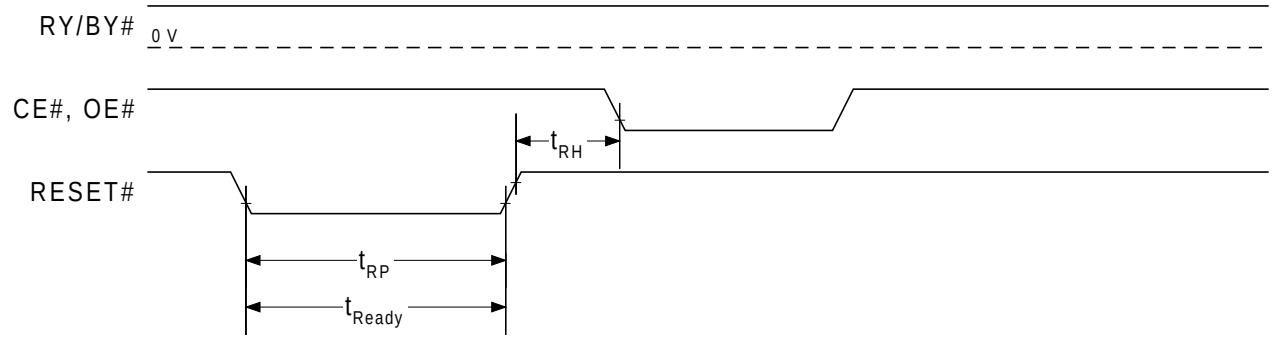
Figure 15. Read Operation Timings

AC CHARACTERISTICS

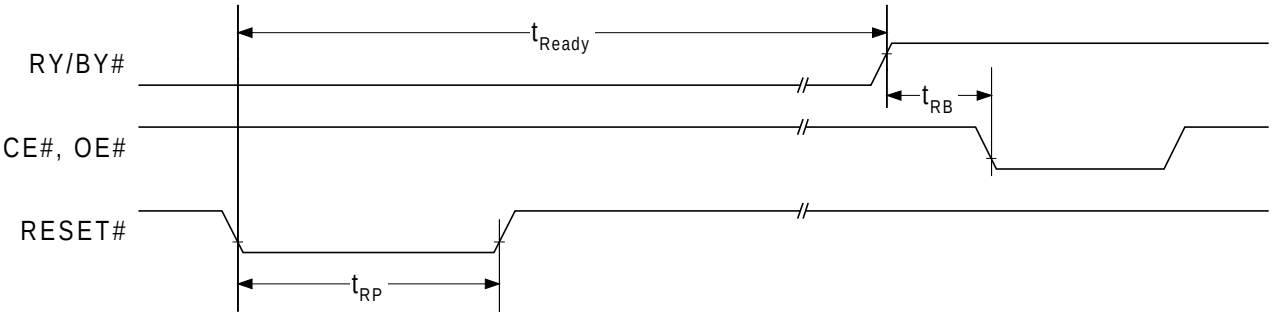
Hardware Reset (RESET#)

Parameter		Description	Test Setup		Speed Option			Unit
JEDEC	Std				- 55	- 70	- 90	
	t_{READY}	RESET# Pin Low (During Automatic Algorithms) to Read or Write [1]		Max	20			µs
	t_{READY}	RESET# Pin Low (NOT During Automatic Algorithms) to Read or Write [1]		Max	500			ns
	t_{RP}	RESET# Pulse Width		Min	500			ns
	t_{RH}	RESET# High Time Before Read [1]		Min	50			ns
	t_{RPD}	RESET# Low to Standby Mode		Max	20			µs
	t_{RB}	RY/BY# Recovery Time		Min	0			ns

Notes:
1. Not 100% tested.



Reset Timings NOT During Automatic Algorithms



Reset Timings During Automatic Algorithms

Figure 16. RESET# Timings

AC CHARACTERISTICS

Word/Byte Configuration (BYTE#)

Parameter		Description		Speed Option			Unit
JEDEC	Std			- 55	- 70	- 90	
	t_{ELFL}	CE# to BYTE# Switching Low	Max	5			ns
	t_{ELFH}	CE# to BYTE# Switching High	Max	5			ns
	t_{FLQZ}	BYTE# Switching Low to Output High-Z	Max	25	25	30	ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	55	70	90	ns

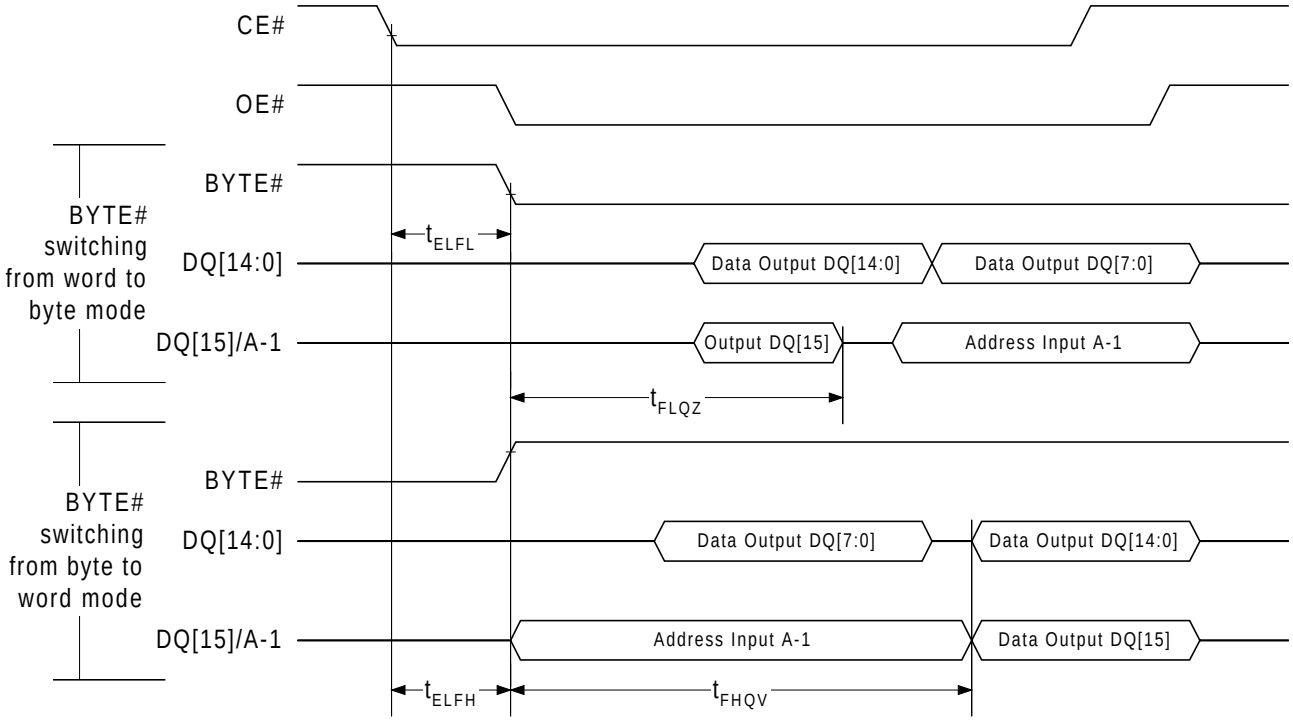
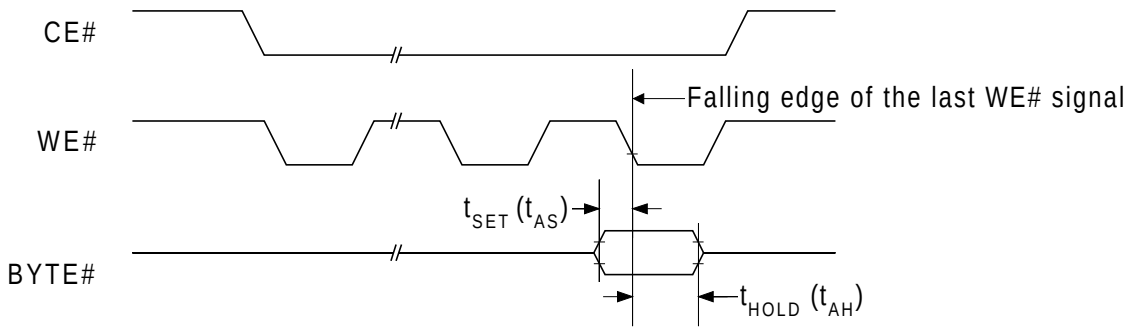


Figure 17. BYTE# Timings for Read Operations



Note: Refer to the Program/Erase Operations table for t_{AS} and t_{AH} specifications.

Figure 18. BYTE# Timings for Write Operations

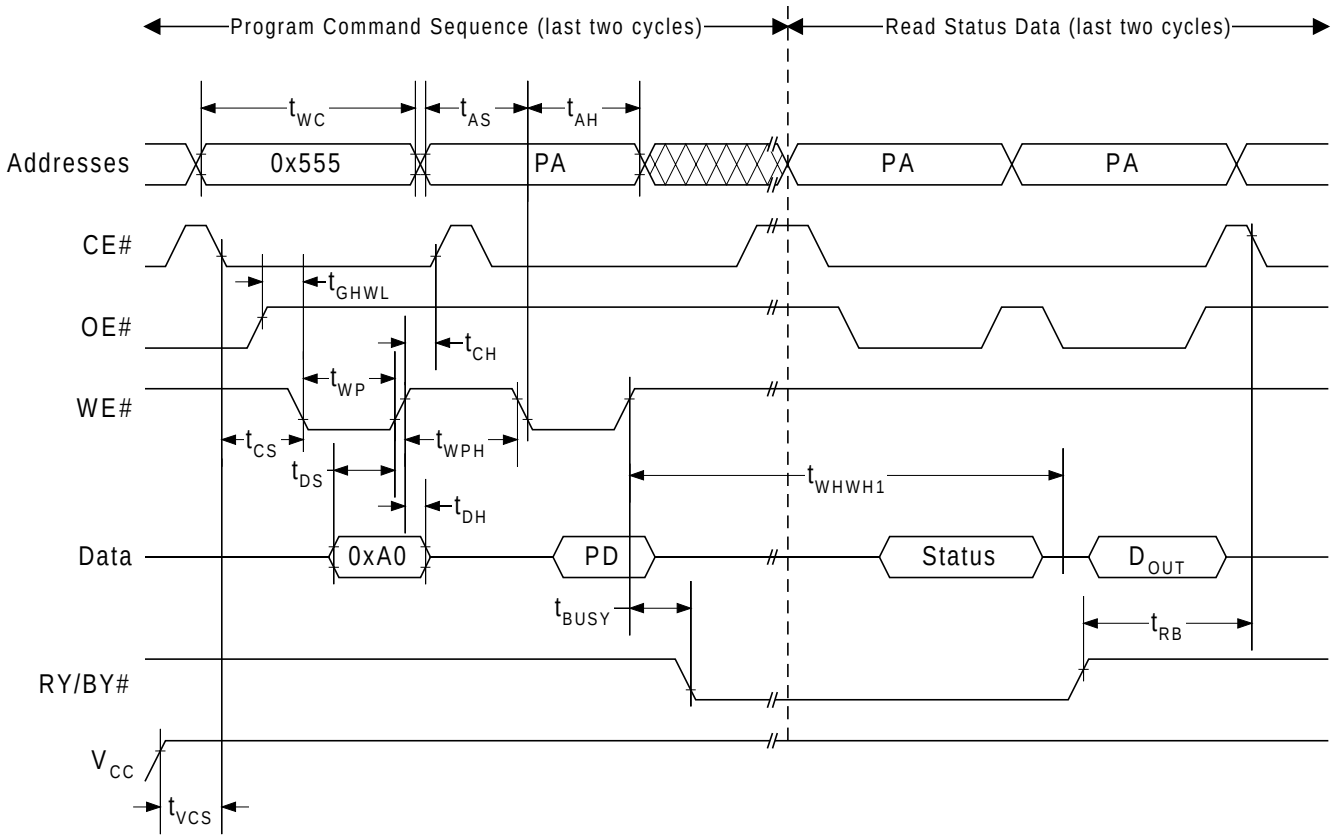
AC CHARACTERISTICS

Program and Erase Operations

Parameter		Description			Speed Option			Unit
JEDEC	Std				- 55	- 70	- 90	
t_{AVAV}	t_{WC}	Write Cycle Time [1]		Min	55	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min		0		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	35	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min		0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min		0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min		0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min		0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min		30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation [1, 2, 3]	Byte Mode	Typ		9		µs
				Max		300		µs
			Word Mode	Typ		11		µs
				Max		360		µs
		Chip Programming Operation [1, 2, 3, 5]	Byte Mode	Typ		4.5		sec
				Max		13.5		sec
			Word Mode	Typ		2.9		sec
				Max		8.7		sec
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation [1, 2, 4]		Typ		0.5		sec
				Max		10		sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation [1, 2, 4]		Typ		5		sec
		Erase and Program Cycle Endurance [1]		Typ		1,000,000		cycles
				Min		100,000		cycles
	t_{VCS}	V_{CC} Setup Time [1]		Min		50		µs
	t_{RB}	Recovery Time from RY/BY#		Min		0		ns
	t_{BUSY}	WE# High to RY/BY# Delay		Min		90		ns

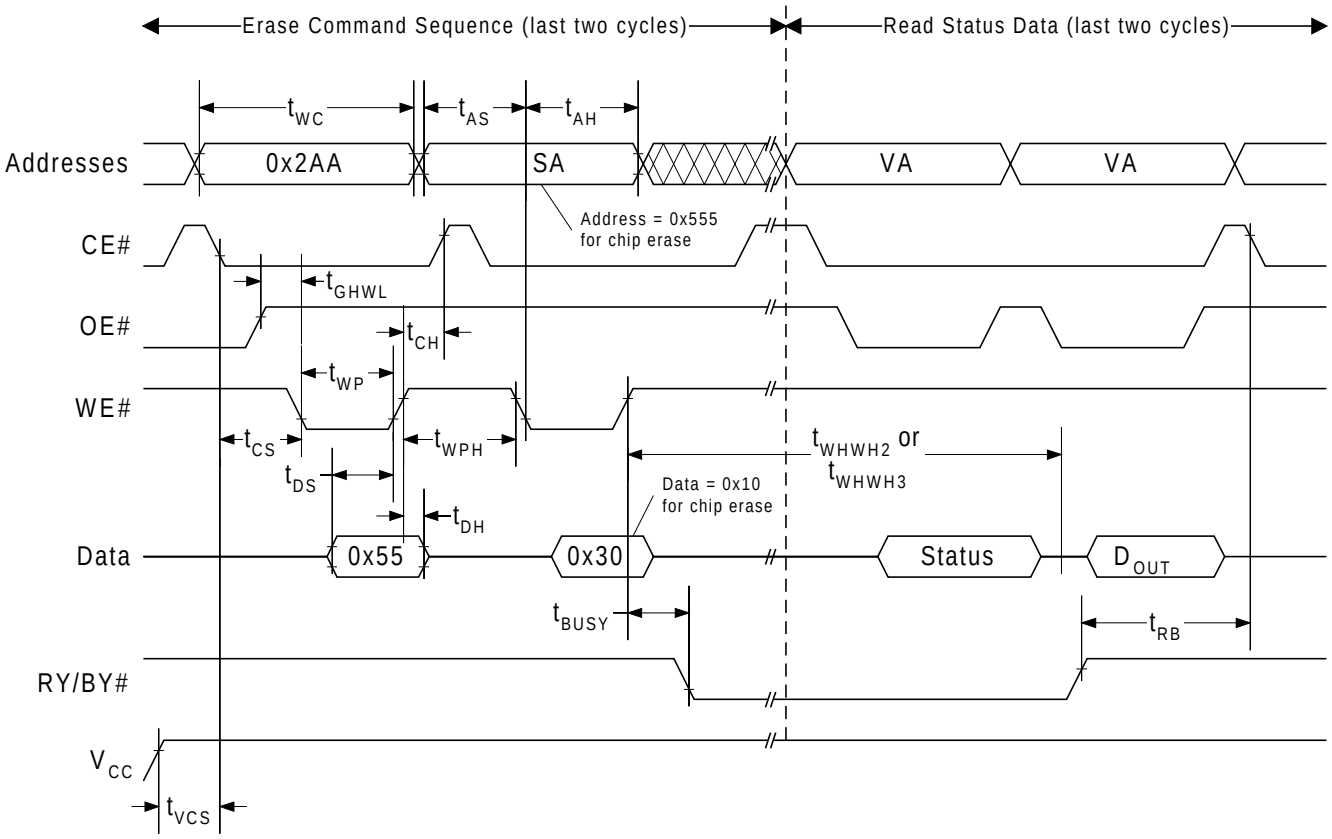
Notes:
1. Not 100% tested.
2. Typical program and erase times assume the following conditions: 25 °C, V_{CC} = 3.0 volts, 100,000 cycles. In addition, programming typicals assume a checkerboard pattern. Maximum program and erase times are under worst case conditions of 90 °C, V_{CC} = 2.7 volts (3.0 volts for - 55 version), 100,000 cycles.
3. Excludes system-level overhead, which is the time required to execute the four-bus-cycle sequence for the program command. See Table 6 for further information on command sequences.
4. Excludes 0x00 programming prior to erasure. In the preprogramming step of the Automatic Erase algorithm, all bytes are programmed to 0x00 before erasure.
5. The typical chip programming time is considerably less than the maximum chip programming time listed since most bytes/words program faster than the maximum programming times specified. The device sets DQ[5] = 1 only If the maximum byte/word program time specified is exceeded. See Write Operation Status section for additional information.

AC CHARACTERISTICS



Notes:
1. PA = Program Address, PD = Program Data, D_{OUT} is the true data at the program address.
2. Commands shown are for Word mode operation.
3. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 19. Program Operation Timings

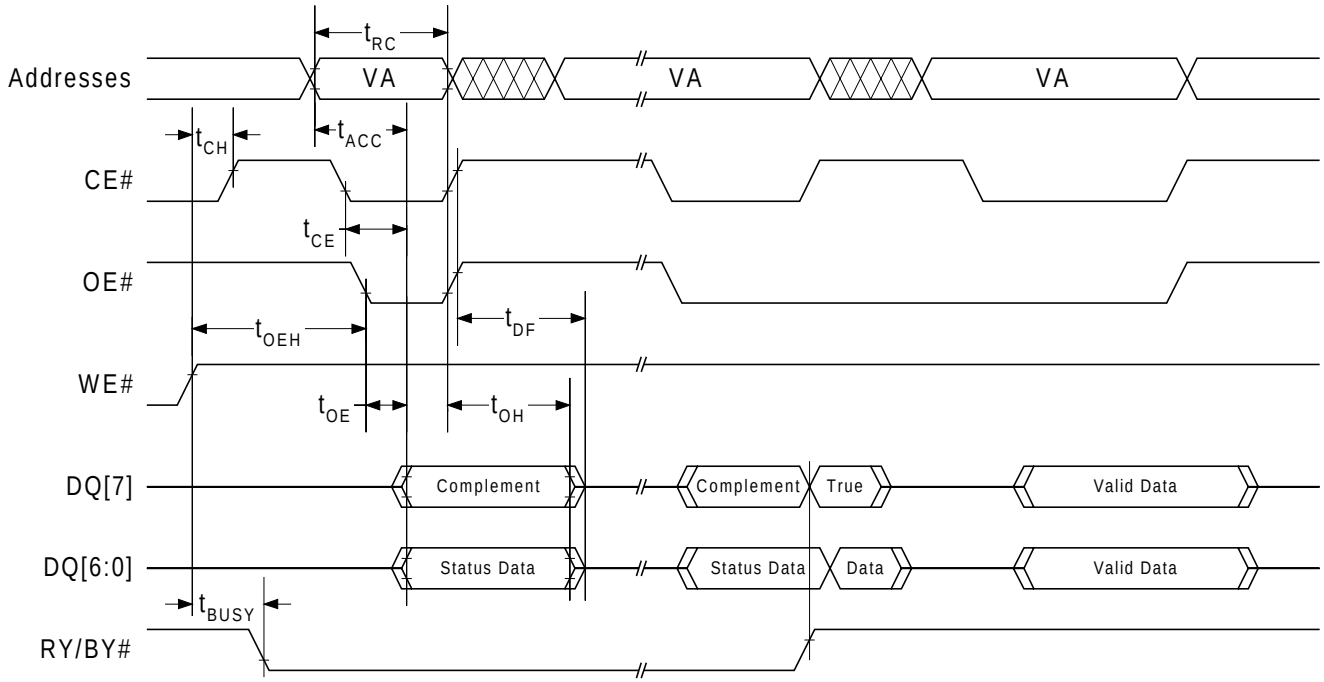


Notes:

1. SA =Sector Address (for sector erase), VA = Valid Address for reading status data (see Write Operation Status section), D_{OUT} is the true data at the read address.(0xFF after an erase operation).
2. Commands shown are for Word mode operation.
3. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

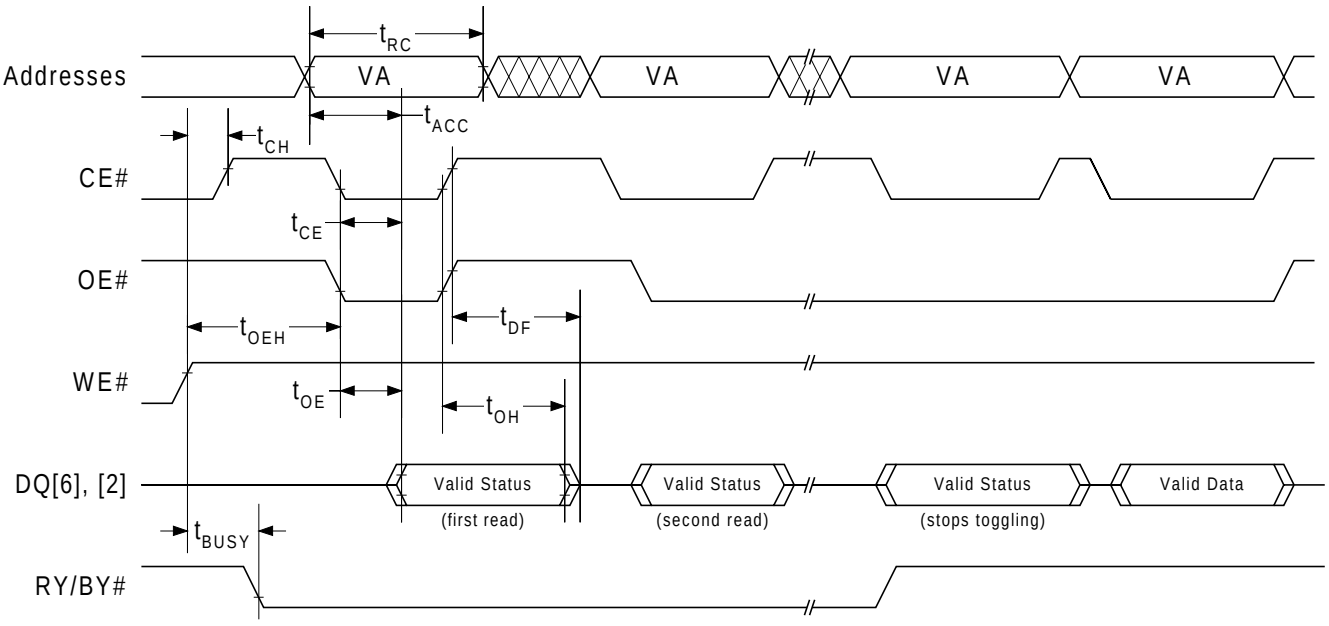
Figure 20. Sector/Chip Erase Operation Timings

AC CHARACTERISTICS



Notes:
1. VA = Valid Address for reading Data# Polling status data (see Write Operation Status section).
2. Illustration shows first status cycle after command sequence, last status read cycle and array data read cycle.

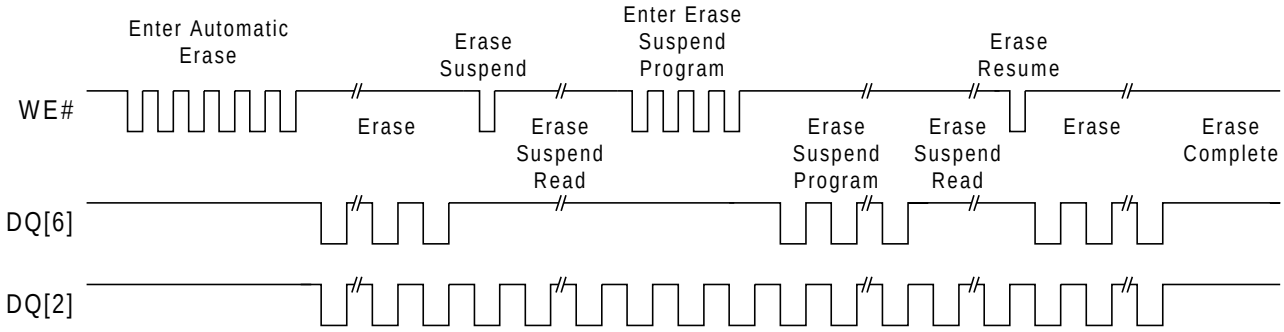
Figure 21. Data# Polling Timings (During Automatic Algorithms)



Notes:
1. VA = Valid Address for reading Toggle Bits (DQ[2], DQ[6]) status data (see Write Operation Status section).
2. Illustration shows first two status read cycles after command sequence, last status read cycle and array data read cycle.

Figure 22. Toggle Polling Timings (During Automatic Algorithms)

AC CHARACTERISTICS



Notes:
1. The system may use CE# or OE# to toggle DQ[2] and DQ[6]. DQ[2] toggles only when read at an address within an erase-suspended sector.

Figure 23. DQ[2] and DQ[6] Operation

Sector Protect and Unprotect, Temporary Sector Unprotect

Parameter		Description		Speed Option			Unit
JEDEC	Std			- 55	- 70	- 90	
	t_{VIDR}	V_{ID} Transition Time for Temporary Sector Unprotect [1]	Min	500			ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4			µs
	t_{VRES}	RESET# Setup Time for Sector Protect and Unprotect	Min	1			µs
	t_{PROT}	Sector Protect Time	Max	150			µs
	t_{UNPR}	Sector Unprotect Time	Max	15			ms

Notes:
1. Not 100% tested.

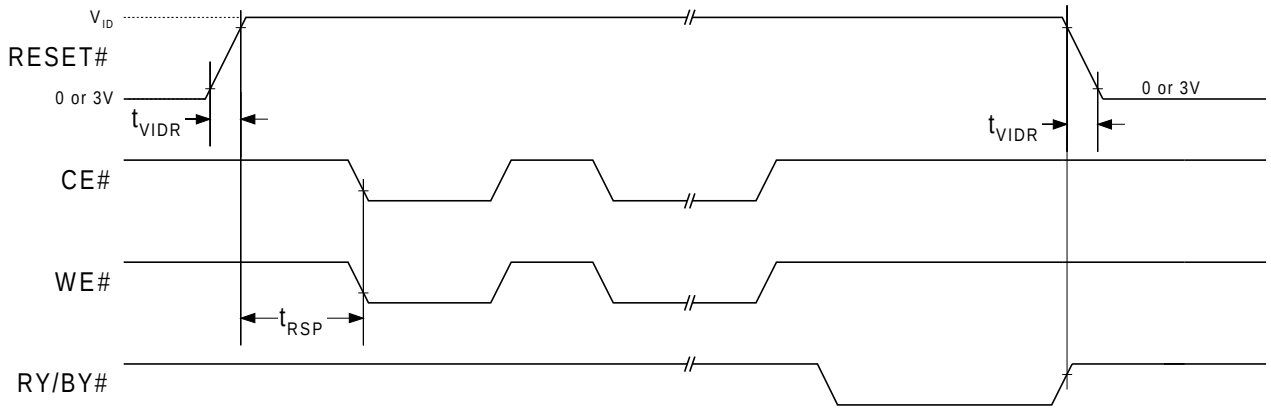
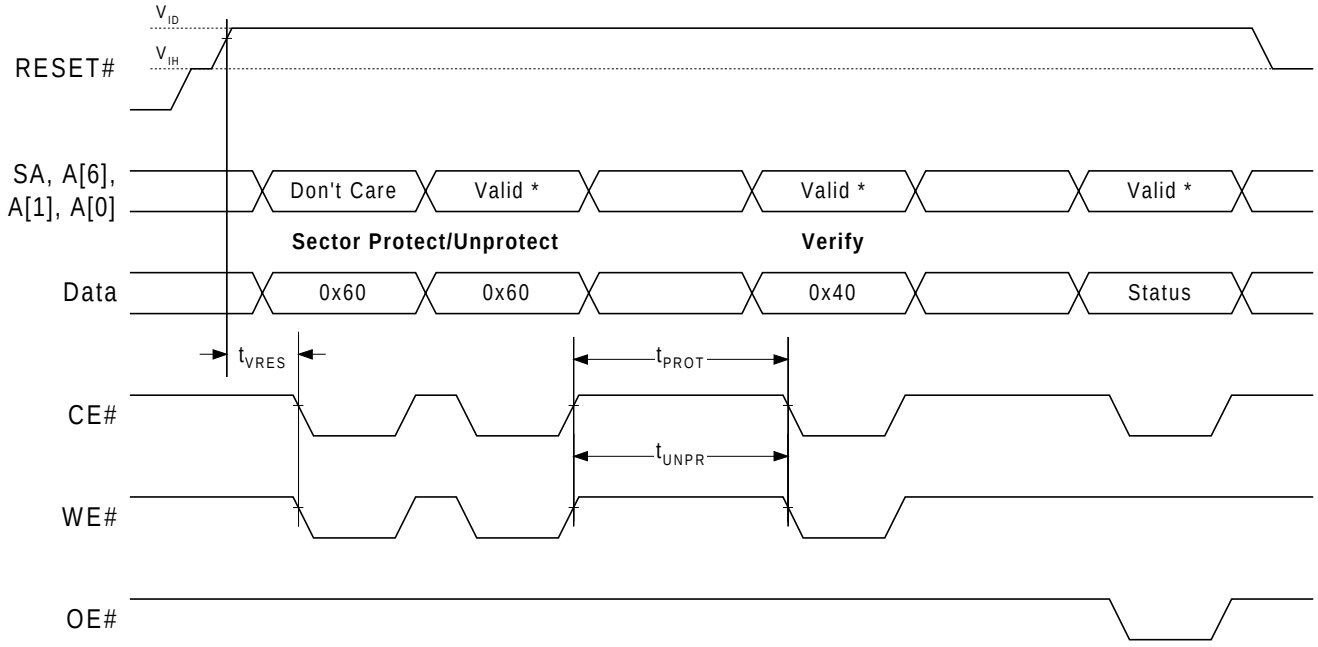


Figure 24. Temporary Sector Unprotect Timings

AC CHARACTERISTICS



Note: For Sector Protect, A[6] = 0, A[1] = 1, A[0] = 0. For Sector Unprotect, A[6] = 1, A[1] = 1, A[0] = 0.

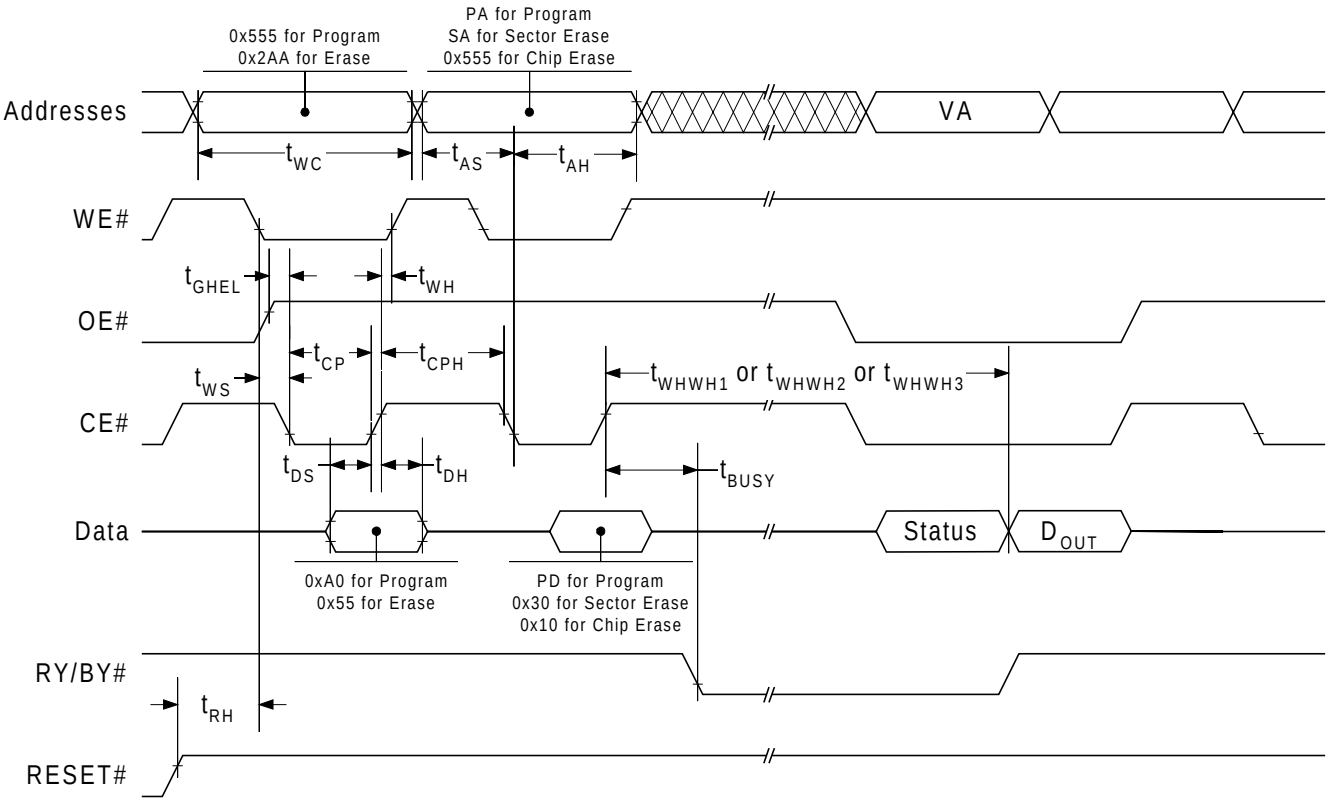
Figure 25. Sector Protect and Unprotect Timings

Alternate CE# Controlled Program and Erase Operations [2]

Parameter		Description		Speed Option			Unit
JEDEC	Std			- 55	- 70	- 90	
t_{AVAV}	t_{WC}	Write Cycle Time [1]	Min	55	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	35	45	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min		0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write	Min		0		ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min		0		ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min		0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	35	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min		30		ns
	t_{BUSY}	CE# to RY/BY# Delay	Min		90		ns

Notes:
1. Not 100% tested.
2. See Program and Erase Operations table for program and erase characteristics.

AC CHARACTERISTICS



Notes:

1. PA = program address, PD = program data, VA = Valid Address for reading program or erase status (see Write Operation Status section), D_{OUT} = array data read at VA.
2. Illustration shows the last two cycles of the program or erase command sequence and the last status read cycle.
3. Word mode addressing shown.
4. RESET# shown only to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

Figure 26. Alternate CE# Controlled Write Operation Timings

Latchup Characteristics

Description	Minimum	Maximum	Unit
Input voltage with respect to V_{SS} on all pins except I/O pins(including A[9], OE# and RESET#)	- 1.0	12.5	V
Input voltage with respect to V_{SS} on all I/O pins	- 1.0	V_{CC} + 1.0	V
V_{CC} Current	- 100	100	mA

Notes:
1. Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0V, one pin at a time.

TSOP and PSOP Pin Capacitance

Symbol	Parameter	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions: T_A = 25 ºC, f = 1.0 MHz.

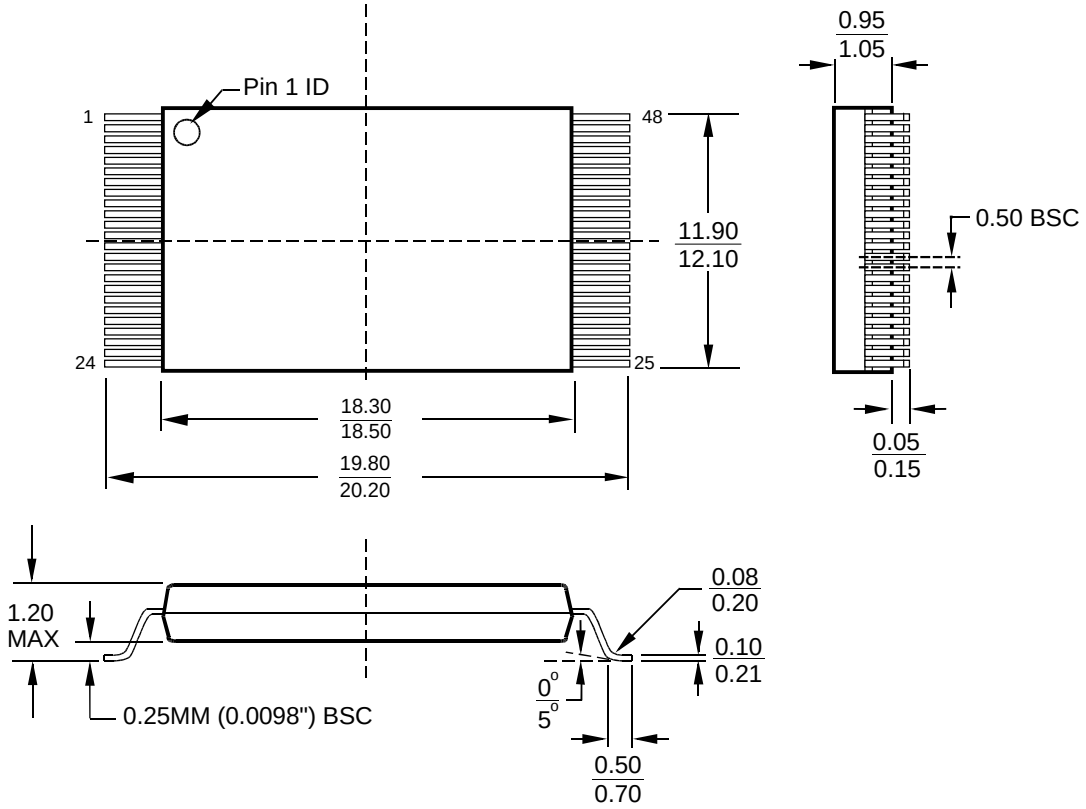
Data Retention

Parameter	Test Conditions	Minimum	Unit
Minimum Pattern Data Retention Time	150 ºC	10	Years
	125 ºC	20	Years

PACKAGE DRAWINGS

Physical Dimensions

TSOP48 - 48-pin Thin Small Outline Package (measurements in millimeters)

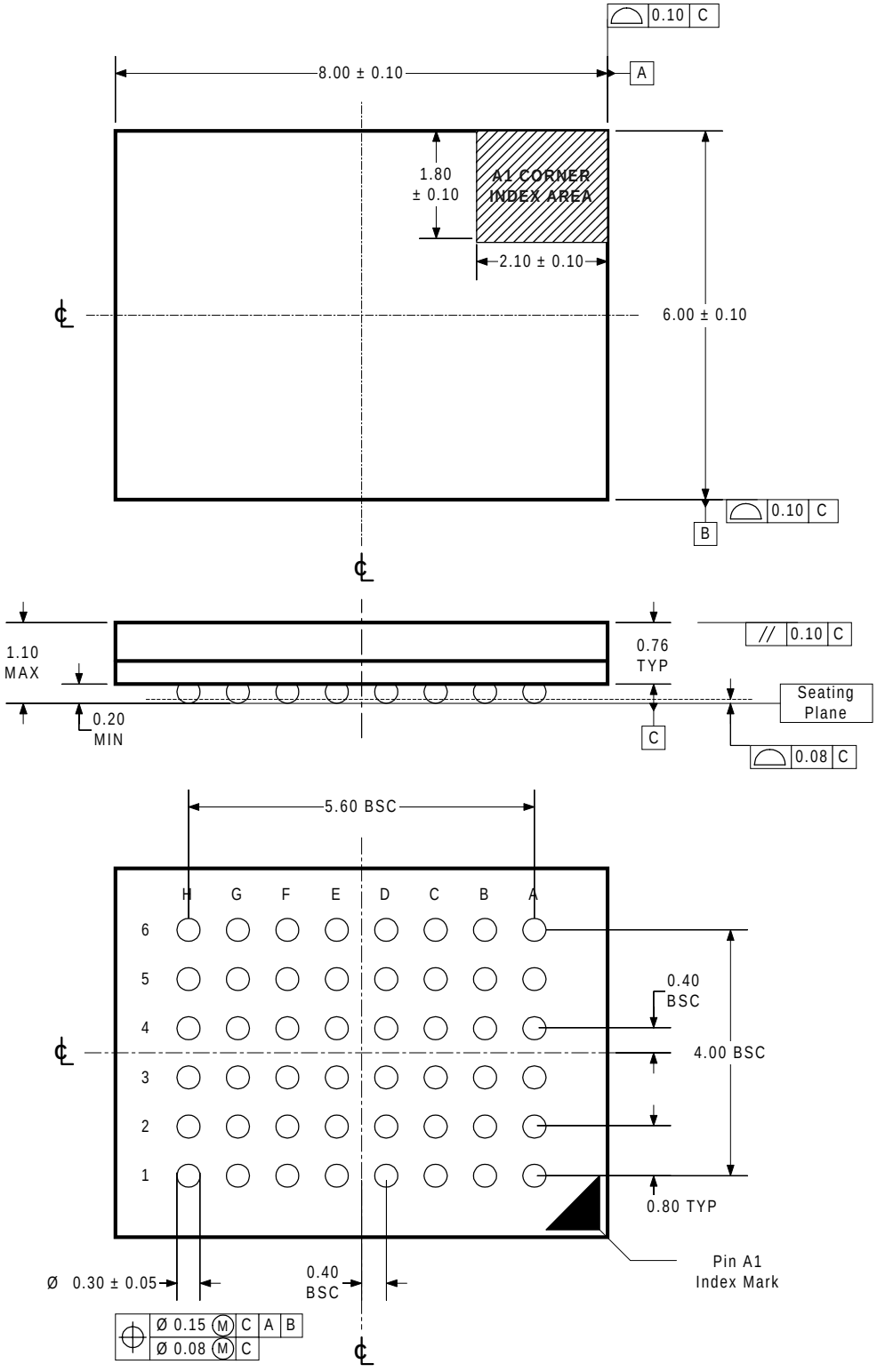


PACKAGE DRAWINGS

Physical Dimensions

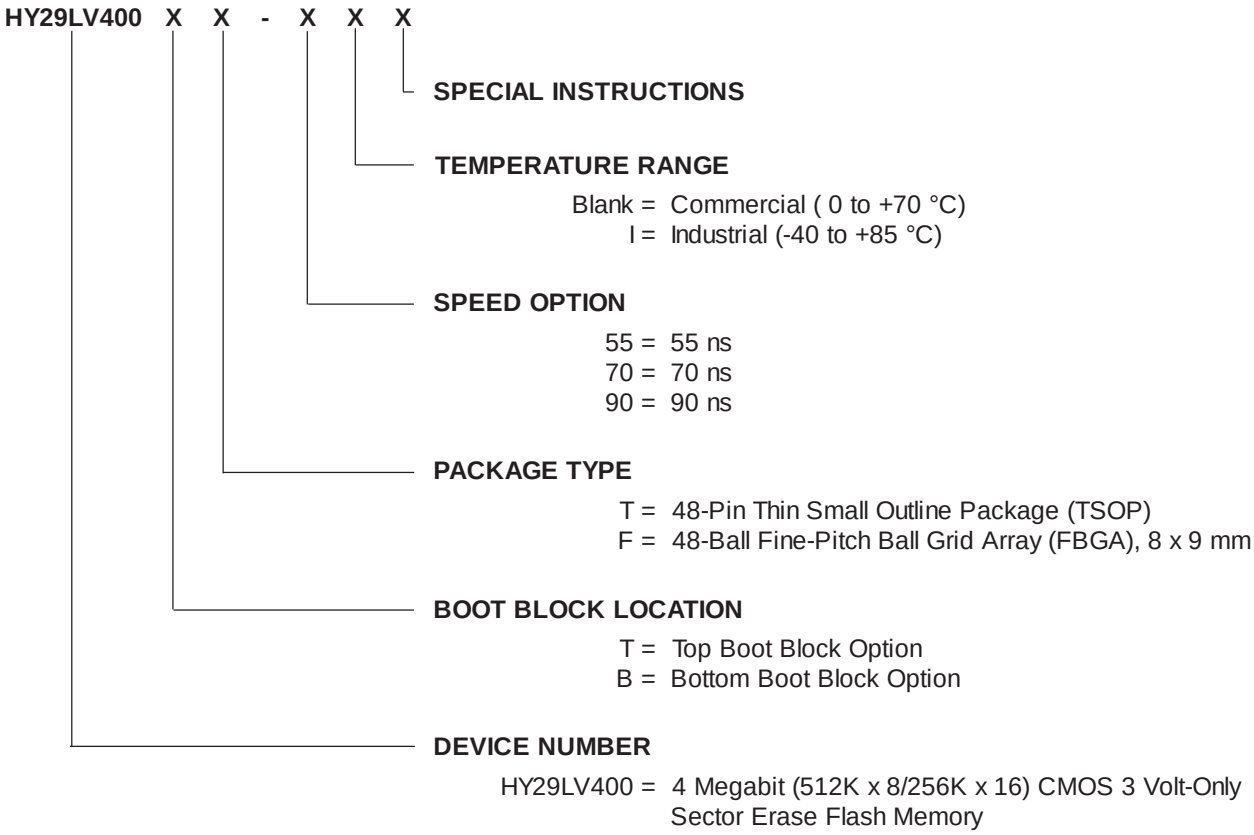
FBGA48 - 48-Ball Fine-Pitch Ball Grid Array, 6 x 8 mm (measurements in millimeters)

Note: Unless otherwise specified, tolerance = ± 0.05



ORDERING INFORMATION

Hynix products are available in several speeds, packages and operating temperature ranges. The ordering part number is formed by combining a number of fields, as indicated below. Refer to the 'Valid Combinations' table, which lists the configurations that are planned to be supported in volume. Please contact your local Hynix representative or distributor to confirm current availability of specific configurations and to determine if additional configurations have been released.



VALID COMBINATIONS

	Package and Speed					
	TSOP			FBGA		
Temperature	**55 ns**	**70 ns**	**90 ns**	**55 ns**	**70 ns**	**90 ns**
Commercial	T-55	T-70	T-90	F-55	F-70	F-90
Industrial	T-55I	T-70I	T-90I	F-55I	F-70I	F-90I

Note:

1. The complete part number is formed by appending the suffix shown in the table above to the Device Number. For example, the part number for a 90 ns, top boot block, Industrial temperature range device in the TSOP package is *HY29LV400TT-90I*.

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Revision Record

Rev.	Date	Details
1.0	10/01	Initial release.

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