Integrated Device Technology, Inc.

# BiCMOS STATIC RAM 64K (16K x 4-BIT)

**PRELIMINARY**
**IDT71B98**

## FEATURES:

- 16K x 4 BiCEMOS™ Static RAM
- High-speed address access time
  - — Commercial: 8/10/12ns
  - — Military: 10/12/15ns
- Fast Output Enable
  - — Commercial: 5/6/7ns
  - — Military: 6/7/8ns
- Multiple Chip Selects
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 24-pin, 300 mil plastic DIP; 24-pin, 300 mil ceramic DIP and 24-pin, 300-mil plastic SOJ

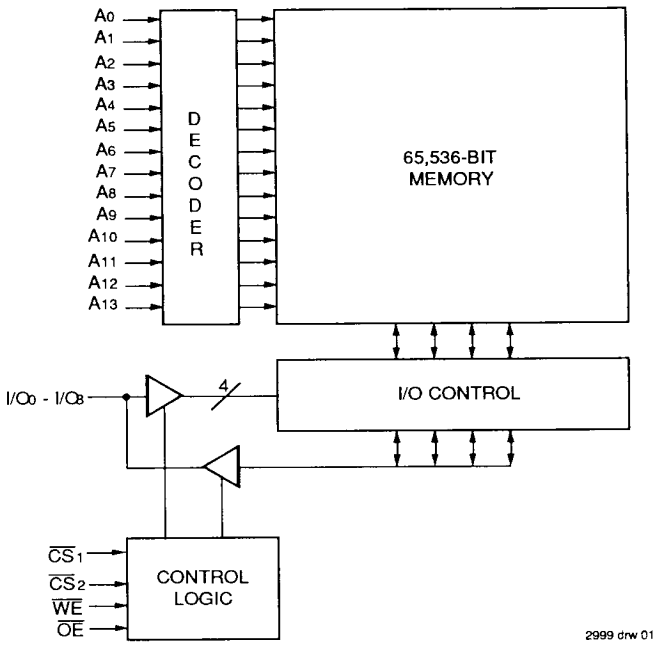
## DESCRIPTION:

The IDT71B98 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 8ns are available with power consumption of only 400mW (typ.). All inputs and outputs of the IDT71B98 are TTL-compatible and operation is from a single 5V supply. Multiple chip selects simplify design and operation.

The IDT61B98 is packaged in a 24-pin, 300 mil plastic DIP; 24-pin, 300 mil ceramic DIP and a 24-pin, 300 mil SOJ.

## FUNCTIONAL BLOCK DIAGRAM

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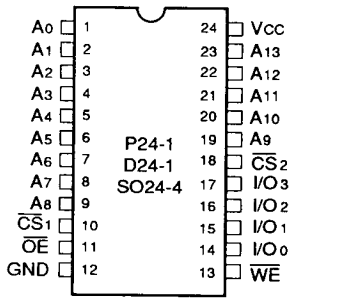
## PIN CONFIGURATION




**DIP/SOJ**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Com'l. | Mil. | Unit |
|---|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | -65 to +125 | °C |
| $P_T$ | Power Dissipation | 1.25 | 1.25 | W |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

2958 tbl 02

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## TRUTH TABLE(1)

| $\overline{CS_1}$ | $\overline{CS_2}$ | $\overline{OE}$ | $\overline{WE}$ | I/O | Function |
|---|---|---|---|---|---|
| X | H | X | X | Hi-Z | Deselect Chip |
| H | X | X | X | Hi-Z | Deselect Chip |
| L | L | L | H | DOUT | Read Cycle |
| L | L | X | L | DIN | Write Cycle |
| L | L | H | H | Hi-Z | Outputs Disabled |

2999 tbl 01

**NOTE:**
1. H = $V_{IH}$, L = $V_{IL}$, X = Don't care.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$(2) | Input Capacitance | $V_{IN}$ = 0V | 8 | pF |
| $C_{OUT}$(1,2) | Output Capacitance | $V_{OUT}$ = 0V | 12 | pF |

2999 tbl 03

**NOTES:**
1. With output deselected.
2. Characterized values, not currently tested.

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | 6.0 | V |
| $V_{IL}$ | Input Low Voltage | -0.5 | — | 0.8 | V |

2999 tbl 04

**NOTE:**
1. 1.5V undershoots are allowed for 10ns once per cycle.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Condition | IDT71B98 Min. | IDT71B98 Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | — | 10 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | — | 10 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 10mA, $V_{CC}$ = Min. | — | 0.5 | V |
| | | $I_{OL}$ = 8mA, $V_{CC}$ = Min. | — | 0.4 | |
| $V_{OH}$ | Output HIgh Voltage | $I_{OH}$ = -4mA, $V_{CC}$ = Min. | 2.4 | — | V |

2999 tbl 05

## DC ELECTRICAL CHARACTERISTICS[1]

($V_{CC}$ = 5.0V ± 10%)

| Symbol | Parameter | 71B98S8 | | 71B98S10 | | 71B98S12 | | 71B98S15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | |
| $I_{CC}$ | Dynamic Operating Current, $\overline{CS}$ = $V_{IL}$ Outputs Open, $V_{CC}$ = Max., f = $f_{MAX}$[2] | 200 | — | 180 | 190 | 160 | 170 | — | 170 | mA |

2999 tbl 05

**NOTES:**
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1A, 1B & 1C |

2999 tbl 06

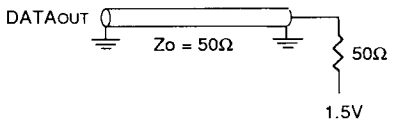



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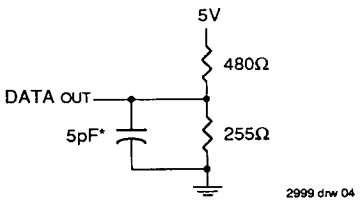
**Figure 1A. AC Test Load**

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*Including jig and scope capacitance.

**Figure 1B.**

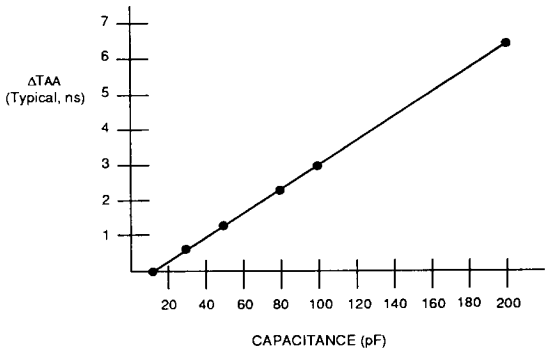


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**Figure 1C. Lumped Capacitive Load, Typical Derating**

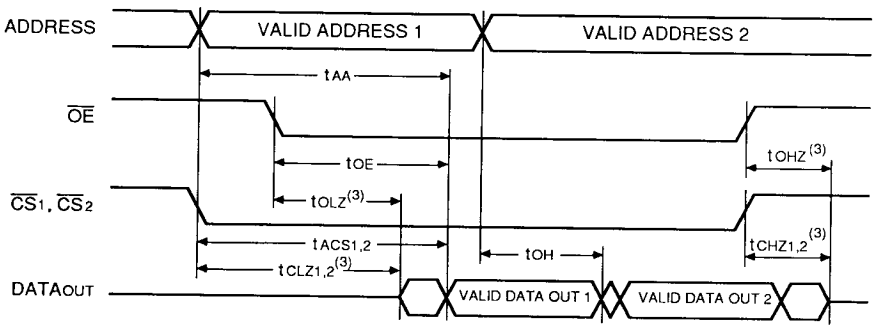
## AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 71B98S8[1] | | 71B98S10 | | 71B98S12 | | 71B98S15[3] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | | | | | |
| tRC | Read Cycle Time | 8 | — | 10 | — | 12 | — | 15 | — | ns |
| tAA | Address Access Time | — | 8 | — | 10 | — | 12 | — | 15 | ns |
| tACS1,2 | $\overline{CS}_{1,2}$ Access Time | — | 6 | — | 7 | — | 7 | — | 8 | ns |
| tOE | $\overline{OE}$ to Output Valid | — | 4 | — | 5 | — | 6 | — | 7 | ns |
| tCLZ1,2[2] | $\overline{CS}_{1,2}$ to Output in Low Z | 3 | — | 3 | — | 3 | — | 4 | — | ns |
| tCHZ1,2[2] | $\overline{CS}_{1,2}$ to Output in High Z | — | 6 | — | 6 | — | 7 | — | 8 | ns |
| tOLZ[2] | $\overline{OE}$ to Output Low Z | 3 | — | 3 | — | 3 | — | 4 | — | ns |
| tOHZ[2] | $\overline{OE}$ to Output High Z | — | 3 | — | 3 | — | 3 | — | 4 | ns |
| tOH | Out Hold from Add Change | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| **Write Cycle** | | | | | | | | | | |
| tWC | Write Cycle Time | 8 | — | 10 | — | 12 | — | 15 | — | ns |
| tAW | Address to End of Write | 8 | — | 8 | — | 9 | — | 10 | — | ns |
| tAS | Address Setup Tme | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWP | Write Pulse Width | 8 | — | 8 | — | 9 | — | 10 | — | ns |
| tCW1,2 | $\overline{CS}_{1,2}$ to End of Write | 8 | — | 8 | — | 9 | — | 10 | — | ns |
| tWR | Write Recovery | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWZ[2] | $\overline{WE}$ to Out in High Z | — | 3 | — | 3 | — | 3 | — | 4 | ns |
| tDW | Data Setup | 5 | — | 5 | — | 6 | — | 8 | — | ns |
| tDH | Data Hold | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tOW[2] | Output from End of Write | 3 | — | 3 | — | 3 | — | 4 | — | ns |

**NOTES:**
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.
3. -55° to +125°C temperature range only.

2999 tbl 08

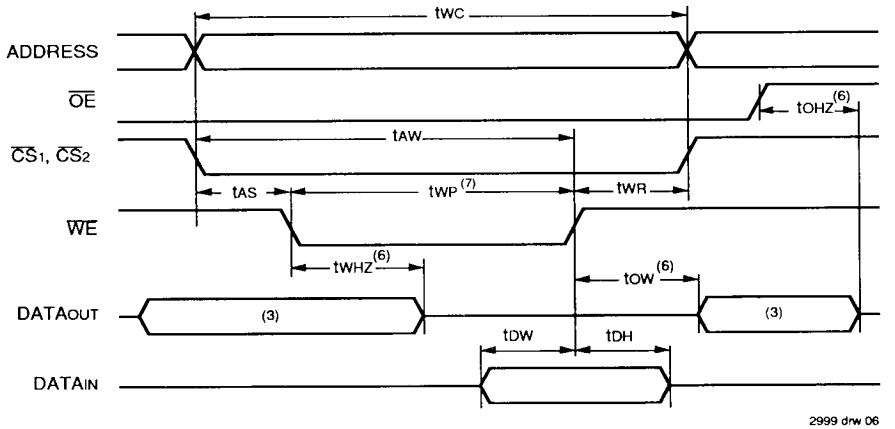
## TIMING WAVEFORM OF READ CYCLE[1,2]



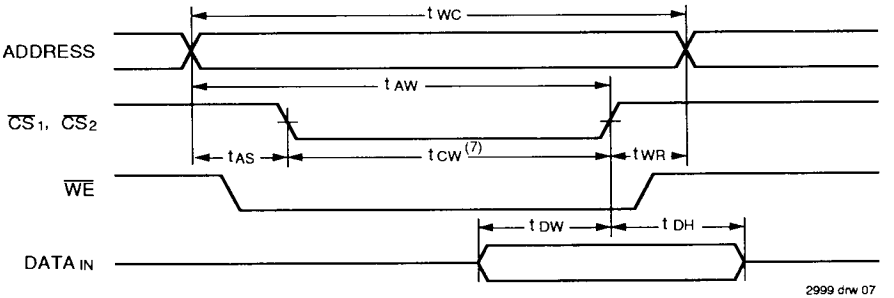

2999 drw 05

**NOTES:**
1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}_{1,2}$ transition low.
3. Transition is measured ±200mV from steady state.

## TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CYCLE)(1,2,4,5)

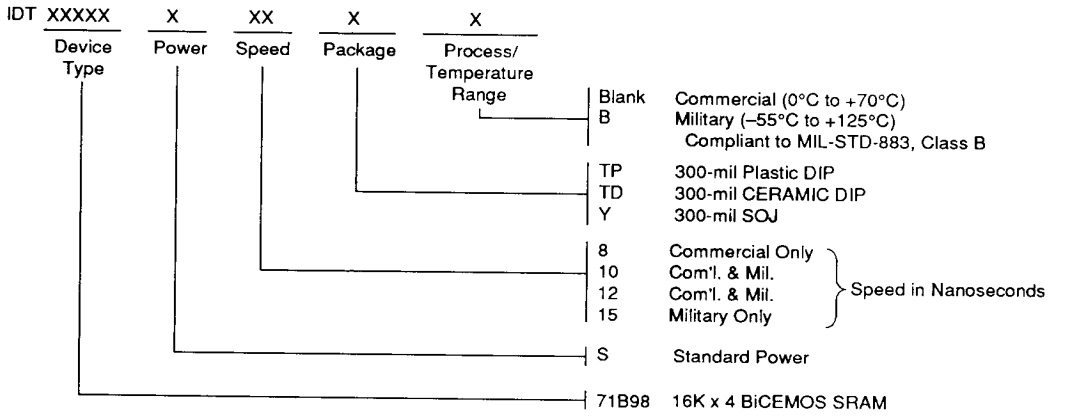



## TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CYCLE)(1,2,4,5,6)




**NOTES:**
1. A write occurs during the overlap (tCW and tWP) of $\overline{CS}_{1,2}$ low and $\overline{WE}$ low.
2. tWP is measured from the earlier of $\overline{CS}_{1,2}$ or $\overline{WE}$ being deasserted.
3. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
4. If $\overline{CS}$ asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
5. If $\overline{CS}$ is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

## ORDERING INFORMATION

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