T-46-23-10

ADVANCED INFORMATION. **CY7C1006**

CYPRESS SEMICONDUCTOR

256K x 4 Static R/W RAM

Features

- **High speed**
  - **— t_{AA} = 15 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 800 mW**
- **Low standby power**
  - **— 250 mW**
- **Low data-retention power**
  - **— 100 µW at 2.0V**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C1006 is a high-performance CMOS static RAM organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

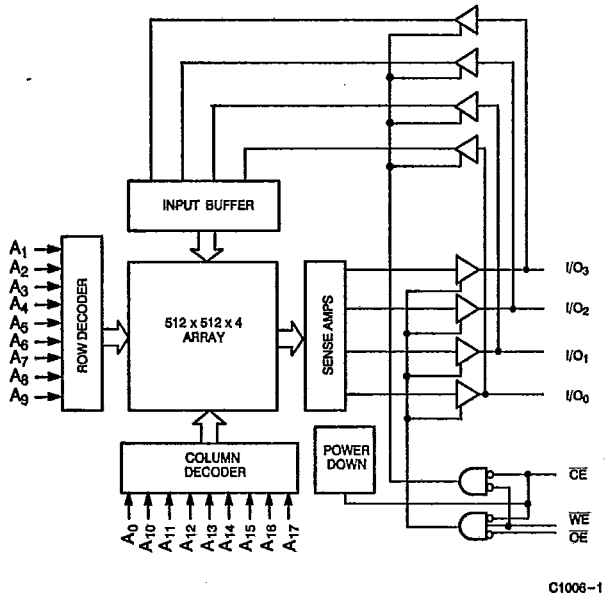
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C1006 is available in standard 300-mil-wide DIPs and SOJs.

Logic Block Diagram



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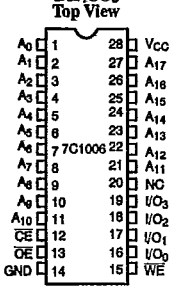
Pin Configuration

DIP/SOJ
Top View



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Selection Guide

		7C1006-15	7C1006-20	7C1006-12
Maximum Access Time (ns)		15	20	25
Maximum Operating Current (mA)	Commercial	145	145	145
	Military		150	150
Maximum Standby Current (mA)	Commercial	45	45	45
	Military		50	50

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