40V Precision Low Power Operational Amplifiers

ISL28117, ISL28217, ISL28417

The ISL28117, ISL28217 and ISL28417 are a family of very high precision amplifiers featuring low noise vs power consumption, low offset voltage, low I_{BIAS} current and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise, and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL28117 single and ISL28217 dual are offered in an 8 Ld SOIC, MSOP and TDFN packages. The ISL28417 is offered in 14 Ld SOIC, 14 Ld TSSOP and 16 Ld QFN packages. All devices are offered in standard pin configurations and operate over the extended temperature range from -40°C to +125°C.

Related Literature

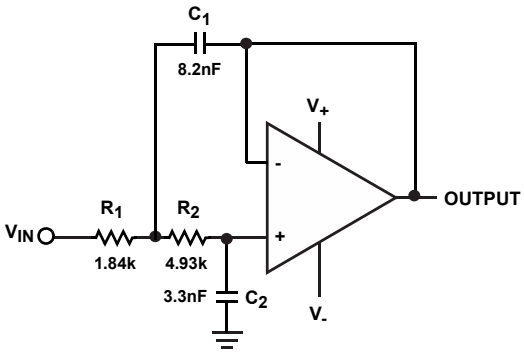
- See AN1508 "ISL281X7SOICEVAL1Z Evaluation Board User's Guide"
- See AN1509 "ISL282X7SOICEVAL2Z Evaluation Board User's Guide"

Features

- Low Input Offset . . . . . ±50µV, Max.
- Superb Offset TC . . . . . 0.6µV/°C, Max.
- Input Bias Current . . . . . ±1nA, Max.
- Input Bias Current TC. . . . . ±5pA/°C, Max.
- Low Current Consumption 440µA
- Voltage Noise 8nV/Hz
- Wide Supply Range . . . . . 4.5V to 40V
- Operating Temperature Range. . . . . -40°C to +125°C
- Small Package Offerings in Single, Dual and Quad
- Pb-Free (RoHS Compliant)

Applications

- Precision Instruments
- Medical Instrumentation
- Spectral Analysis Equipment
- Active Filter Blocks
- Thermocouples and RTD Reference Buffers
- Data Acquisition
- Power Supply Control



SALLEN-KEY LOW PASS FILTER (10kHz)

FIGURE 1. TYPICAL APPLICATION

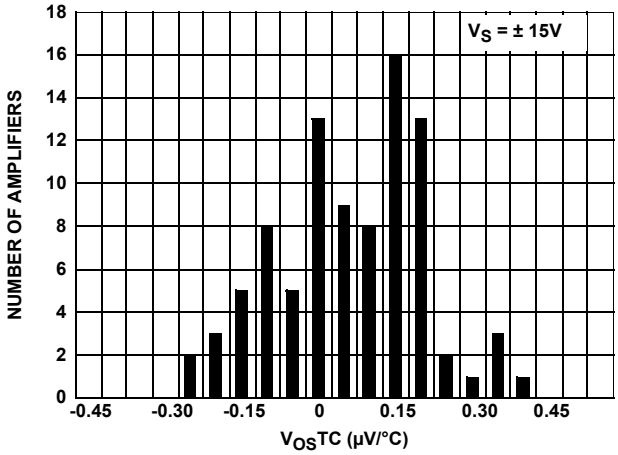


FIGURE 2. V_{OS} TEMPERATURE COEFFICIENT ($V_{OS}TC$)

Ordering Information

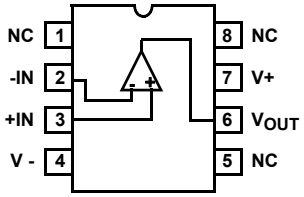
PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OS} (MAX) (µV)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28117FBBZ	28117 FBZ	50 (B Grade)	8 Ld SOIC	M8.15E
ISL28117FBZ	28117 FBZ -C	100 (C Grade)	8 Ld SOIC	M8.15E
ISL28117FUBZ	8117Z	70 (B Grade)	8 Ld MSOP	M8.118
ISL28117FUZ	8117Z -C	150 (C Grade)	8 Ld MSOP	M8.118
ISL28117FRTBZ	8117	75 (B Grade)	8 Ld TDFN	L8.3x3A
ISL28117FRTZ	-C 8117	150 (C Grade)	8 Ld TDFN	L8.3x3A
ISL28217FBBZ	28217 FBZ	50 (B Grade)	8 Ld SOIC	M8.15E
ISL28217FBZ	28217 FBZ -C	100 (C Grade)	8 Ld SOIC	M8.15E
Coming Soon ISL28217FUBZ	8217Z	TBD (B Grade)	8 Ld MSOP	M8.118
ISL28217FUZ	8217Z -C	150 (C Grade)	8 Ld MSOP	M8.118
ISL28217FRTBZ	8217	70 (B Grade)	8 Ld TDFN	L8.3x3A
ISL28217FRTZ	-C 8217	150 (C Grade)	8 Ld TDFN	L8.3x3A
Coming Soon ISL28417FBZ	28417 FBZ	-40 to +125	14 Ld SOIC	M14.15
Coming Soon ISL28417FVZ	28417 FVZ	-40 to +125	14 Ld TSSOP	M14.173
Coming Soon ISL28417FRZ	28 417FRZ	-40 to +125	16 Ld QFN	L16.4x4
ISL28117SOICEVAL1Z	Evaluation Board			
ISL28217SOICEVAL2Z	Evaluation Board			

NOTES:

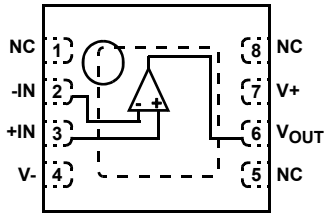
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28117, ISL28217, ISL28417. For more information on MSL please see techbrief TB363.

Pin Configurations

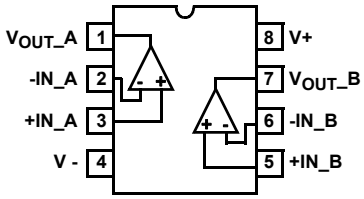
ISL28117
(8 LD SOIC, MSOP)
TOP VIEW



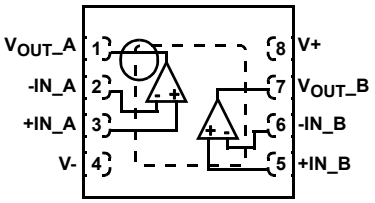
ISL28117
(8 LD TDFN)
TOP VIEW



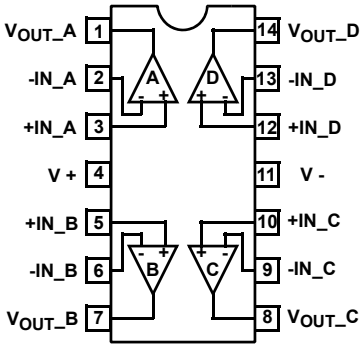
ISL28217
(8 LD SOIC, MSOP)
TOP VIEW



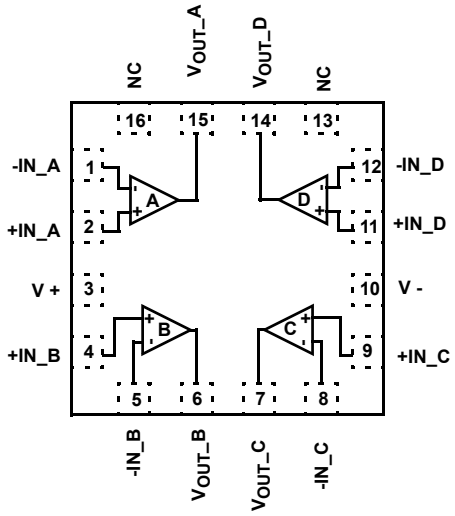
ISL28217
(8 LD TDFN)
TOP VIEW



ISL28417
(14 LD SOIC, TSSOP)
TOP VIEW

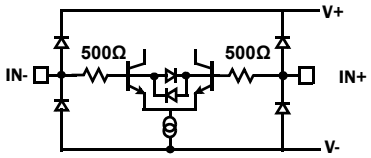


ISL28417
(16 LD QFN)
TOP VIEW

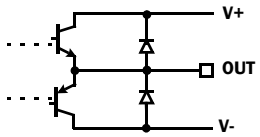


Pin Descriptions

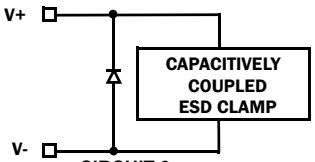
ISL28117 (8 LD SOIC, MSOP, TDFN)	ISL28217 (8 LD SOIC, MSOP, TDFN)	ISL28417 (14 LD SOIC, TSSOP)	ISL28417 (16 LD QFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	-	-	-	+IN	Circuit 1	Amplifier non-inverting input
-	3	3	2	+IN_A		
-	5	5	4	+IN_B		
-	-	10	9	+IN_C		
-	-	12	11	+IN_D		
4	4	11	10	V-	Circuit 3	Negative power supply
2	-	-	-	-IN	Circuit 1	Amplifier inverting input
-	2	2	1	-IN_A		
-	6	6	5	-IN_B		
-	-	9	8	-IN_C		
-	-	13	12	-IN_D		
7	8	4	3	V+	Circuit 3	Positive power supply
6	-	-	-	V_{OUT}	Circuit 2	Amplifier output
-	1	1	15	V_{OUT_A}		
-	7	7	6	V_{OUT_B}		
-	-	8	7	V_{OUT_C}		
-	-	14	14	V_{OUT_D}		
1, 5, 8	-	-	13, 16	NC	-	No internal connection
PD	PD	-	PD	PD	-	Thermal Pad - TDFN and QFN packages only. Connect thermal pad to ground or most negative potential.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage 42V
Min/Max Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
Max/Min Input current for Input Voltage >V+ or <V- . . . . . ±20mA
Output Short-Circuit Duration (1 output at a time). . . . . Indefinite
ESD Rating
- Human Body Model 4.5kV
- Machine Model 500V
- Machine Model (ISL28217 MSOP only) 300V
- Charged Device Model 1.5kV

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . .-40°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC ISL28117 (Notes 4, 7)	120	60
8 Ld SOIC ISL28217 (Notes 4, 7)	105	50
8 Ld MSOP ISL28117 (Notes 4, 7)	155	50
8 Ld MSOP ISL28217 (Notes 4, 7)	160	55
8 Ld TDFN ISL28117 (Notes 5, 6).	48	7
8 Ld TDFN ISL28217 (Notes 5, 6).	43	2
14 Ld SOIC	TBD	TBD
14 Ld TSSOP	TBD	TBD
16 Ld QFN	TBD	TBD

Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . .+150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_S ± 15V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OS}	Input Offset Voltage, SOIC Package	ISL28x17 B Grade	-50	8	50	µV
			-110		**110**	µV
		ISL28x17 C Grade	-100	4	100	µV
			-190		**190**	µV
	Input Offset Voltage, MSOP Package	ISL28117 B Grade	-70	-10	70	µV
			-150		**150**	µV
		ISL28117 C Grade	-150	4	150	µV
			-250		**250**	µV
		ISL28217 C Grade	-150	10	150	µV
			-250		**250**	µV
	Input Offset Voltage, TDFN Package	ISL28117 B Grade	-75	-10	75	µV
			-160		**160**	µV
		ISL28217 B Grade	-70	10	70	µV
			-140		**140**	µV
		ISL28x17 C Grade	-150	10	150	µV
			-250		**250**	µV

Electrical Specifications $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
TCV_{OS}	Input Offset Voltage Temperature Coefficient; SOIC Package	ISL28x17 B Grade	**-0.6**	**0.14**	**0.6**	µV/°C
		ISL28x17 C Grade	**-0.9**	**0.14**	**0.9**	µV/°C
	Input Offset Voltage Temperature Coefficient; MSOP Package	ISL28117 B Grade	**-0.8**	**0.1**	**0.8**	µV/°C
		ISL28117 C Grade	**-1**	**0.14**	**1**	µV/°C
		ISL28217 C Grade	**-1**	**0.14**	**1**	µV/°C
	Input Offset Voltage Temperature Coefficient; TDFN Package	ISL28117 B Grade	**-0.9**	**0.1**	**0.9**	µV/°C
		ISL28217 B Grade	**-0.7**	**0.1**	**0.7**	µV/°C
		ISL28x17 C Grade	**-1**	**0.1**	**1**	µV/°C
I_B	Input Bias Current		-1	0.08	1	nA
			-1.5		**1.5**	nA
TCI_B	Input Bias Current Temperature Coefficient		**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current		-1.5	0.08	1.5	nA
			-1.85		**1.85**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	**-13**		**13**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -13V to +13V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	13.5	13.7		V
			13.2			V
		R_L = 2kΩ to ground	13.3	13.55		V
			13.1			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-13.7	-13.5	V
					-13.2	V
		R_L = 2kΩ to ground		-13.55	-13.3	V
					-13.1	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit			43		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**± 2.25**		**± 20**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{nVp-p}	Voltage Noise V_{P-P}	0.1Hz to 10Hz		0.25		$µV_{P-P}$
e_n	Voltage Noise Density	f = 10Hz		10		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		8.2		nV/√Hz

Electrical Specifications $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
e_n	Voltage Noise Density	f = 1kHz		8		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
THD + N	Total Harmonic Distortion	1kHz, G = 1, $V_O = 3.5V_{RMS}$, $R_L = 2k\Omega$		0.0009		%
		1kHz, G = 1, $V_O = 3.5V_{RMS}$, $R_L = 10k\Omega$		0.0005		%
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	$A_V = 11$, $R_L = 2k\Omega$, $V_O = 4V_{P-P}$		0.5		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		130		ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		21		µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		24		µs
	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		13		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		18		µs
t_{OL}	Output Positive Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$, $R_L = 2k\Omega$ to V_{CM}		5.6		µs
	Output Negative Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$, $R_L = 2k\Omega$ to V_{CM}		10.6		µs

Electrical Specifications $V_S \pm 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OS}	Input Offset Voltage, SOIC Package	ISL28x17 B Grade	-50	8	50	µV
			-110		**110**	µV
		ISL28x17 C Grade	-100	4	100	µV
			-190		**190**	µV
	Input Offset Voltage, MSOP Package	ISL28117 B Grade	-70	-10	70	µV
			-150		**150**	µV
		ISL28117 C Grade	-150	4	150	µV
			-250		**250**	µV
		ISL28217 C Grade	-150	10	150	µV
			-250		**250**	µV
	Input Offset Voltage, TDFN Package	ISL28117 B Grade	-75	-10	75	µV
			-160		**160**	µV
		ISL28217 B Grade	-70	10	70	µV
			-140		**140**	µV
		ISL28x17 C Grade	-150	10	150	µV
			-250		**250**	µV

Electrical Specifications V_S ± 5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
TCV_{OS}	Input Offset Voltage Temperature Coefficient; SOIC Package	ISL28x17 B Grade	**-0.6**	**0.14**	**0.6**	µV/°C
		ISL28x17 C Grade	**-0.9**	**0.14**	**0.9**	µV/°C
	Input Offset Voltage Temperature Coefficient; MSOP Package	ISL28117 B Grade	**-0.8**	**0.1**	**0.8**	µV/°C
		ISL28117 C Grade	**-1**	**0.14**	**1**	µV/°C
		ISL28217 C Grade	**-1**	**0.14**	**1**	µV/°C
	Input Offset Voltage Temperature Coefficient; TDFN Package	ISL28117 B Grade	**-0.9**	**0.1**	**0.9**	µV/°C
		ISL28217 B Grade	**-0.7**	**0.1**	**0.7**	µV/°C
		ISL28x17 C Grade	**-1**	**0.1**	**1**	µV/°C
I_B	Input Bias Current		-1	0.18	1	nA
			-1.5		**1.5**	nA
TCI_B	Input Bias Current Temperature Coefficient		**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current		-1.5	0.3	1.5	nA
			-1.85		**1.85**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient		**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range		**-3**		**3**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -3V to +3V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	120	145		dB
			120			dB
A_{VOL}	Open-Loop Gain	V_O = -3.0V to +3.0V R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.7		V
			3.2			V
		R_L = 2kΩ to ground	3.3	3.55		V
			3.1			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-3.7	-3.5	V
					-3.2	V
		R_L = 2kΩ to ground		-3.55	-3.3	V
					-3.1	V
I_S	Supply Current/Amplifier			0.44	0.53	mA
					0.68	mA
I_{SC}	Short-Circuit			43		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ		1.5		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		0.25		$µV_{P-P}$
e_n	Voltage Noise Density	f = 10Hz		12		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		8.6		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz		8		nV/√Hz

Electrical Specifications $V_S \pm 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
e_n	Voltage Noise Density	f = 10kHz		8		nV/√Hz
in	Current Noise Density	f = 1kHz		0.1		pA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V=11, $R_L = 2k\Omega$, $V_O = 4V_{P-P}$		0.5		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		130		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		130		ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		12		µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM}		19		µs
t_{OL}	Output Positive Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$ $R_L = 2k\Omega$ to V_{CM}		7		µs
	Output Negative Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$ $R_L = 2k\Omega$ to V_{CM}		5.8		µs

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves $V_S = \pm 15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified.

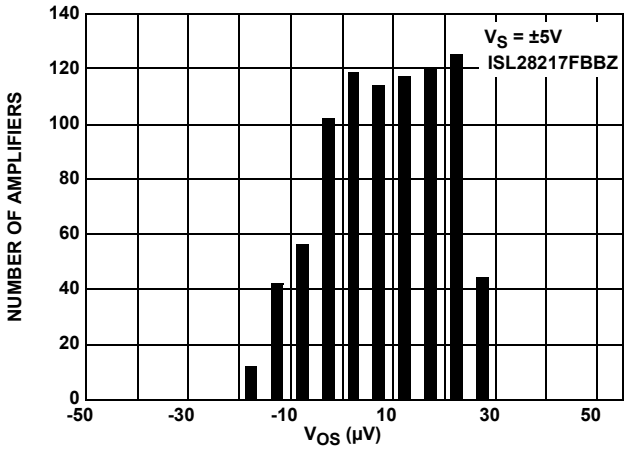


FIGURE 3. V_{OS} DISTRIBUTION FOR GRADE B

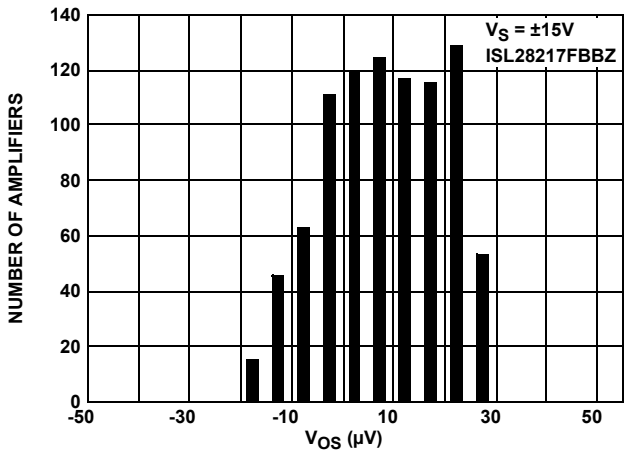


FIGURE 4. V_{OS} DISTRIBUTION FOR GRADE B

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

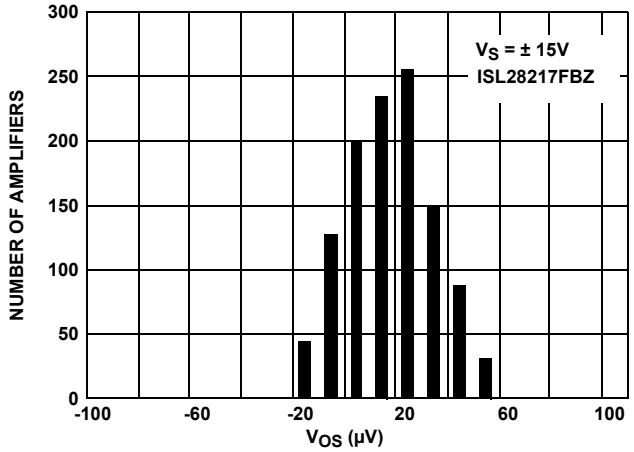


FIGURE 5. V_{OS} DISTRIBUTION FOR GRADE C

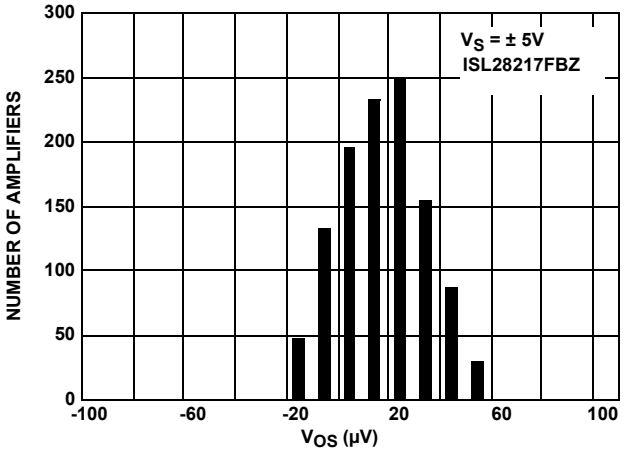


FIGURE 6. V_{OS} DISTRIBUTION FOR GRADE C

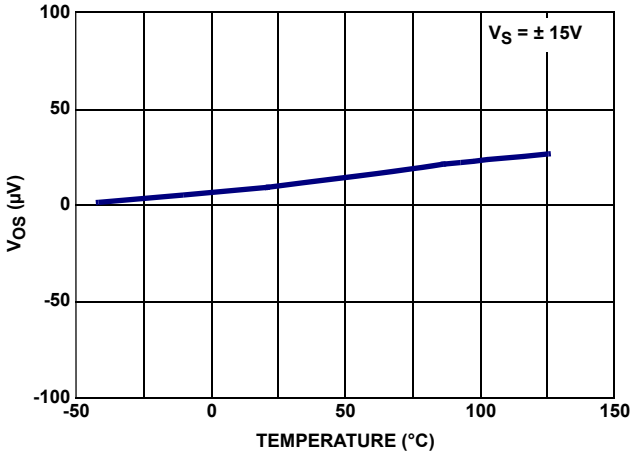


FIGURE 7. V_{OS} RANGE vs TEMPERATURE

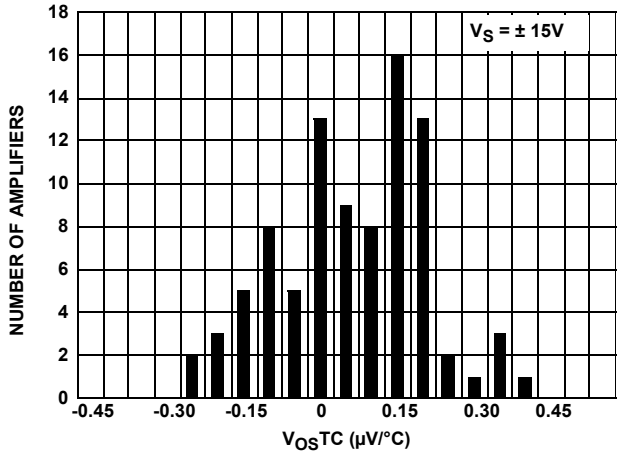


FIGURE 8. TCV_{OS} vs NUMBER OF AMPLIFIERS

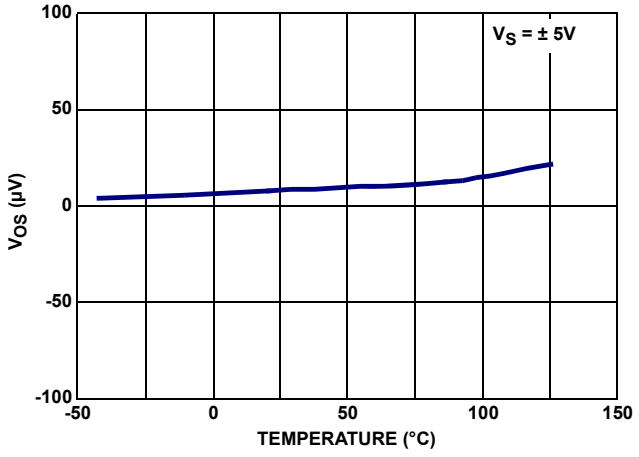


FIGURE 9. V_{OS} RANGE vs TEMPERATURE

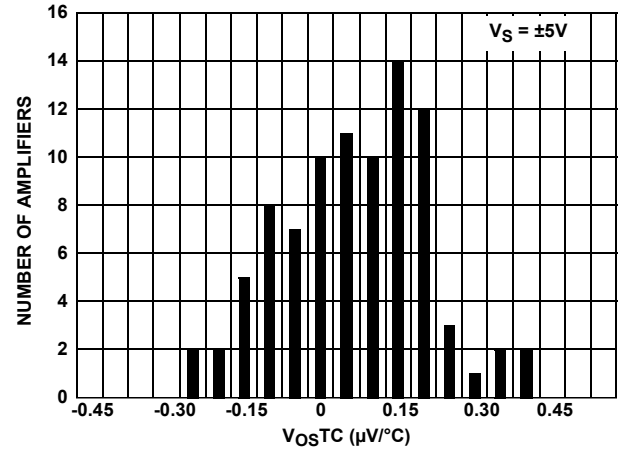


FIGURE 10. TCV_{OS} vs NUMBER OF AMPLIFIERS

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

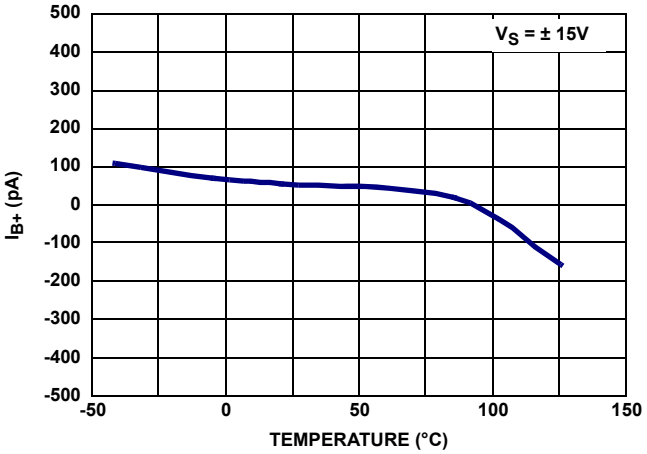


FIGURE 11. I_B+ RANGE vs TEMPERATURE

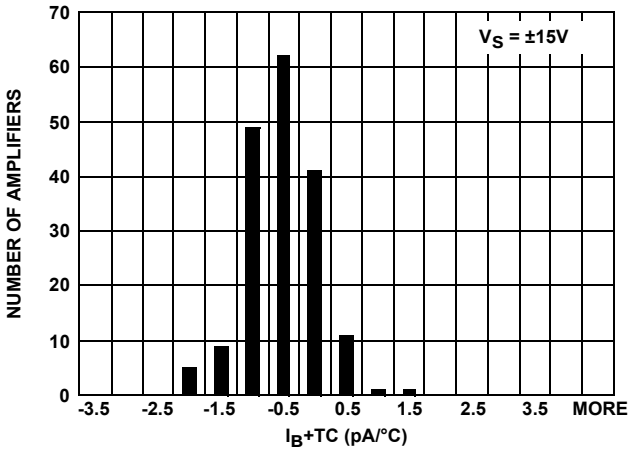


FIGURE 12. TCI_B+ vs NUMBER OF AMPLIFIERS

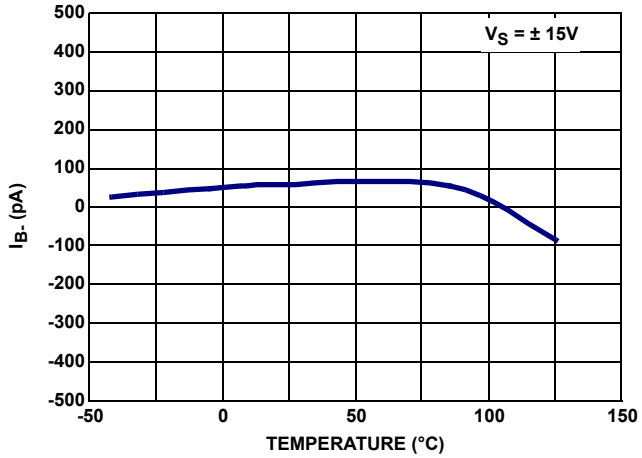


FIGURE 13. I_B- RANGE vs TEMPERATURE

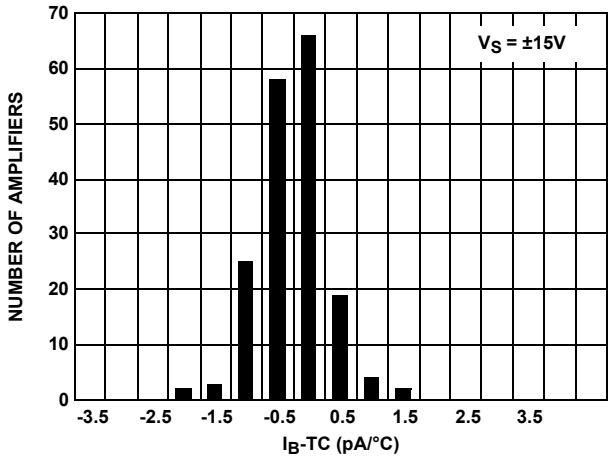


FIGURE 14. TCI_B- vs NUMBER OF AMPLIFIERS

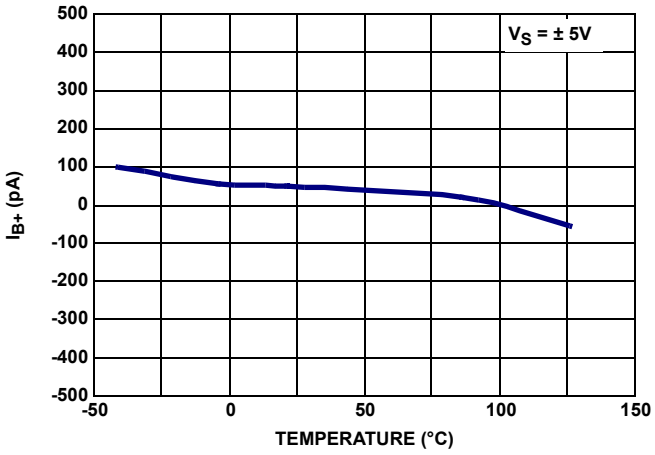


FIGURE 15. I_B+ RANGE vs TEMPERATURE

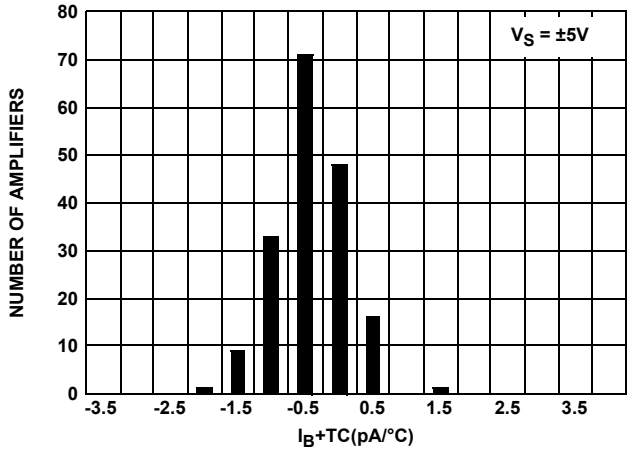


FIGURE 16. TCI_B+ vs NUMBER OF AMPLIFIERS

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

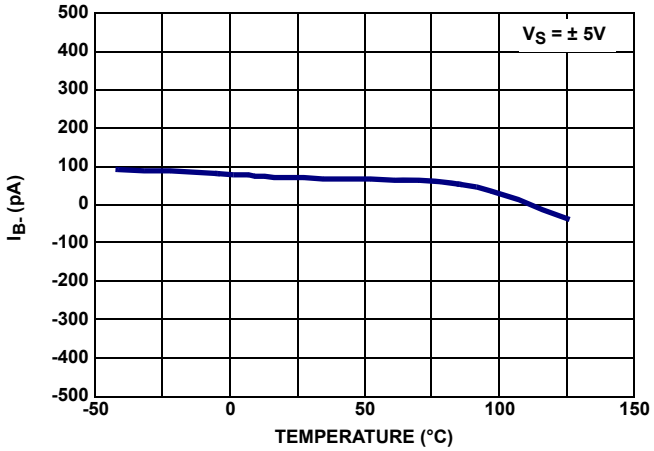


FIGURE 17. I_{B-} RANGE vs TEMPERATURE

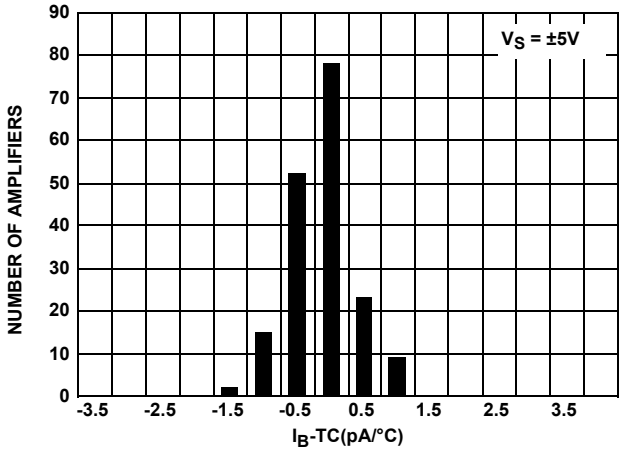


FIGURE 18. TCI_{B-} vs NUMBER OF AMPLIFIERS

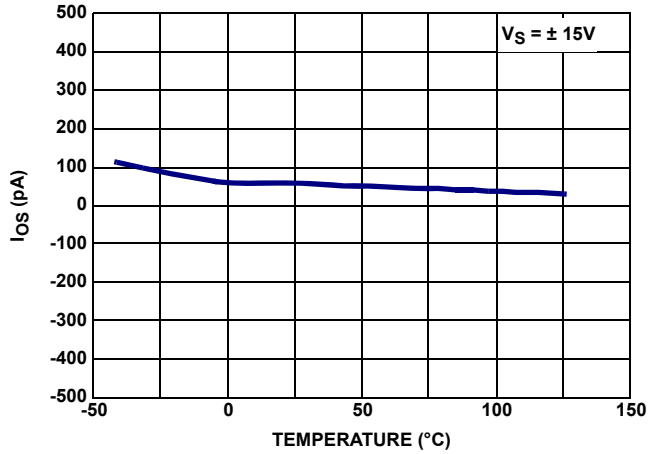


FIGURE 19. I_{OS} RANGE vs TEMPERATURE

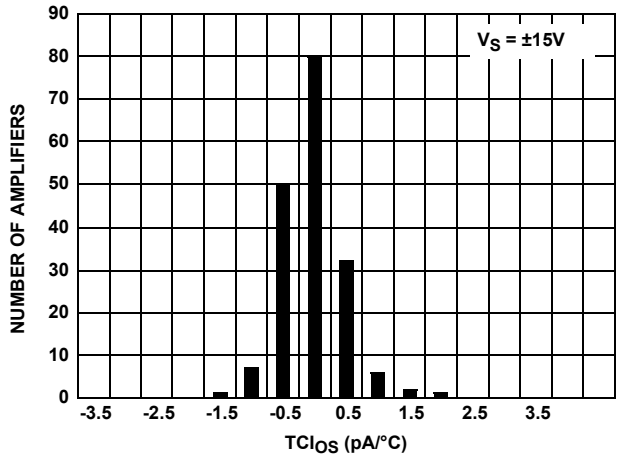


FIGURE 20. $I_{OS}TC$ vs NUMBER OF AMPLIFIERS

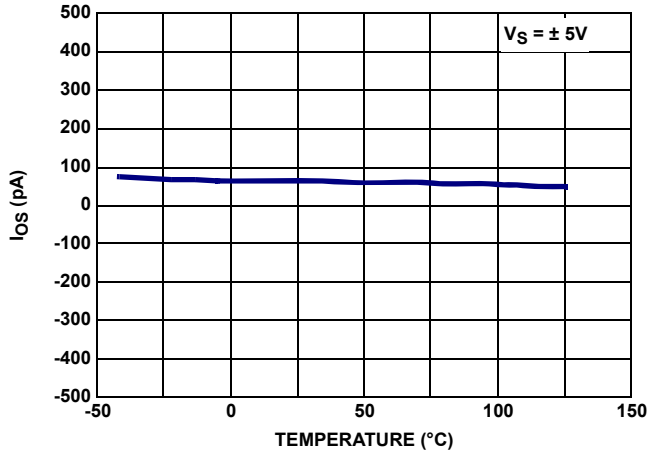


FIGURE 21. I_{OS} RANGE vs TEMPERATURE

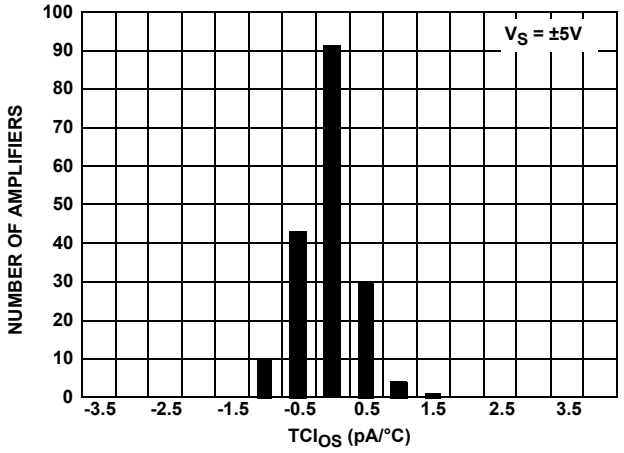


FIGURE 22. $I_{OS}TC$ vs NUMBER OF AMPLIFIERS

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

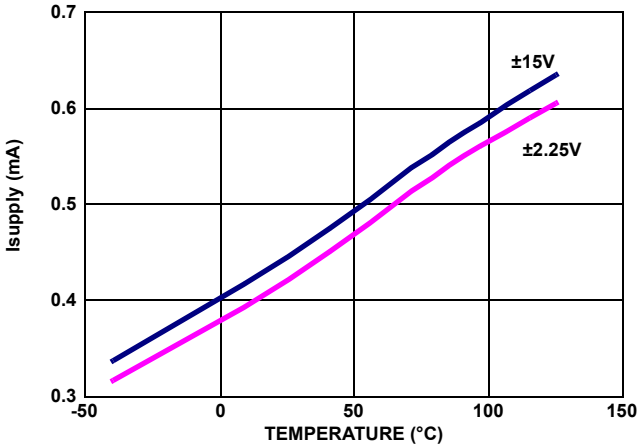


FIGURE 23. SUPPLY CURRENT PER AMP vs TEMPERATURE

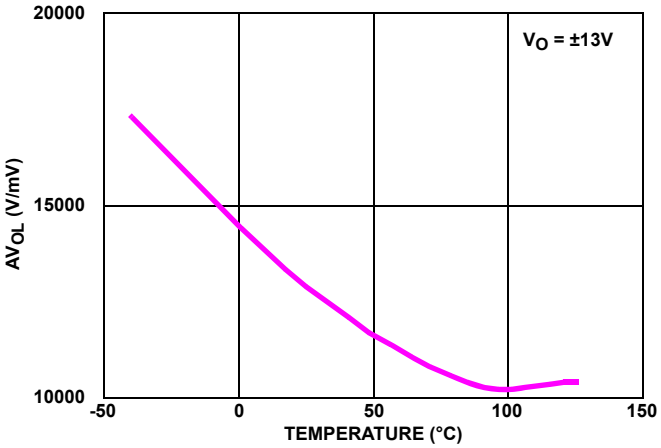


FIGURE 24. AV_{OL} vs TEMPERATURE

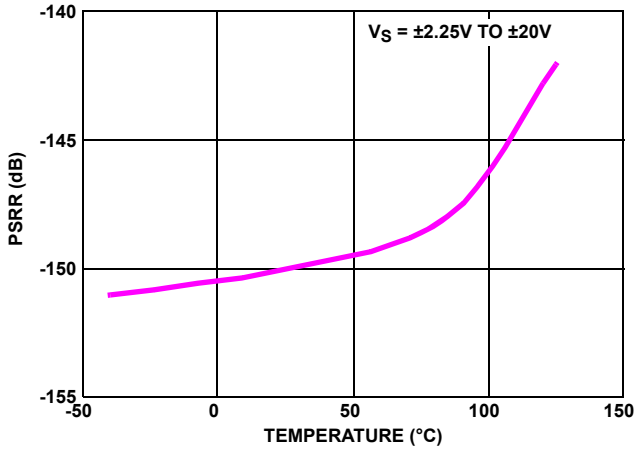


FIGURE 25. PSRR vs TEMPERATURE

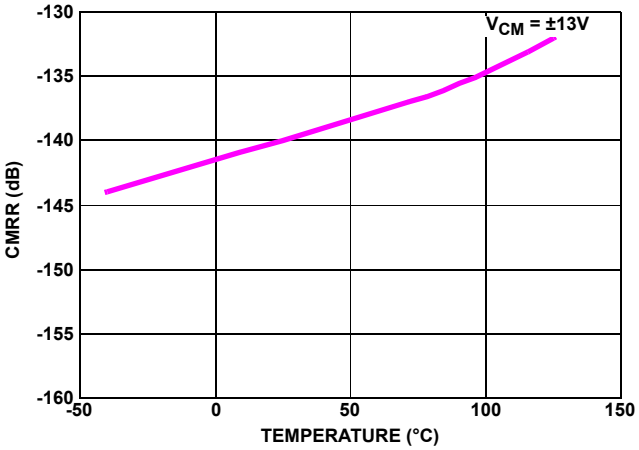


FIGURE 26. CMRR vs TEMPERATURE

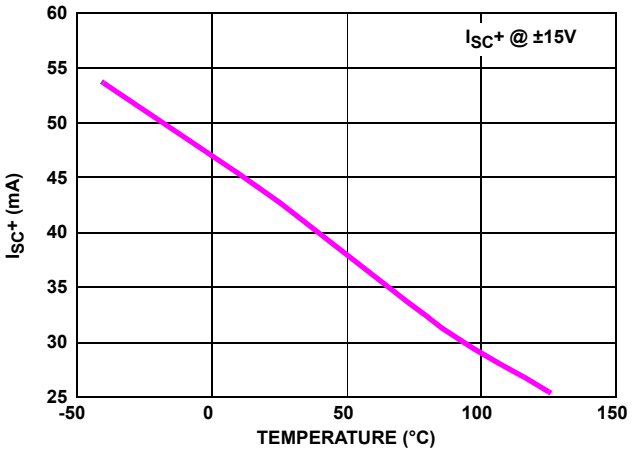


FIGURE 27. SHORT CIRCUIT CURRENT vs TEMPERATURE

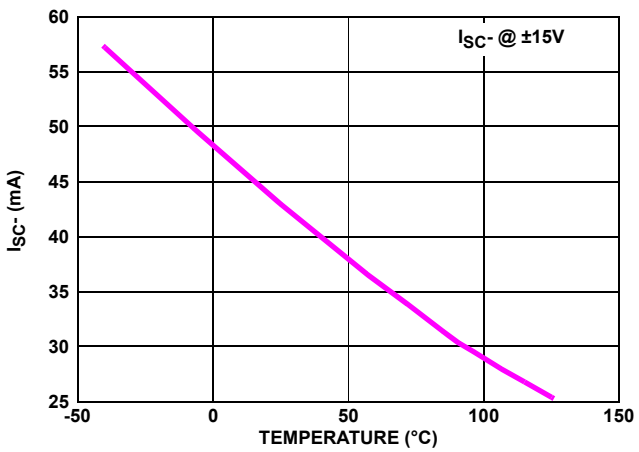


FIGURE 28. SHORT CIRCUIT CURRENT vs TEMPERATURE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

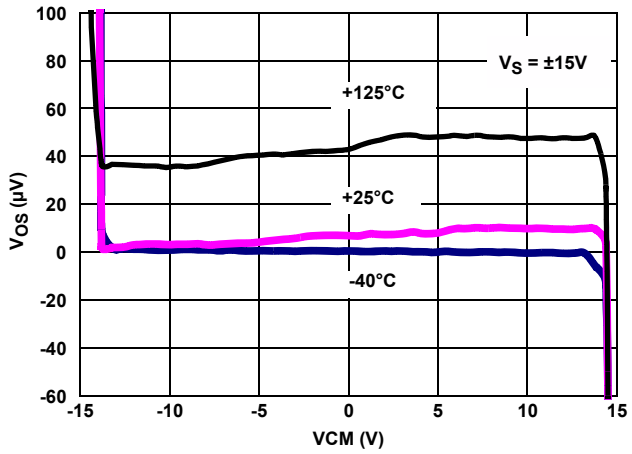


FIGURE 29. INPUT V_{OS} vs INPUT COMMON MODE VOLTAGE, V_S = ±15

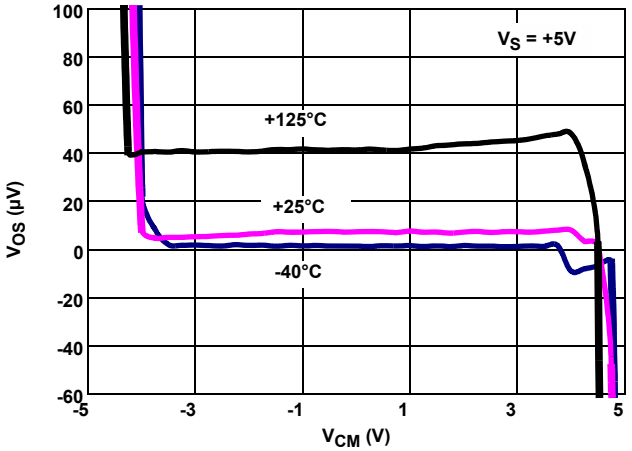


FIGURE 30. INPUT V_{OS} vs INPUT COMMON MODE VOLTAGE, V_S = ±5V

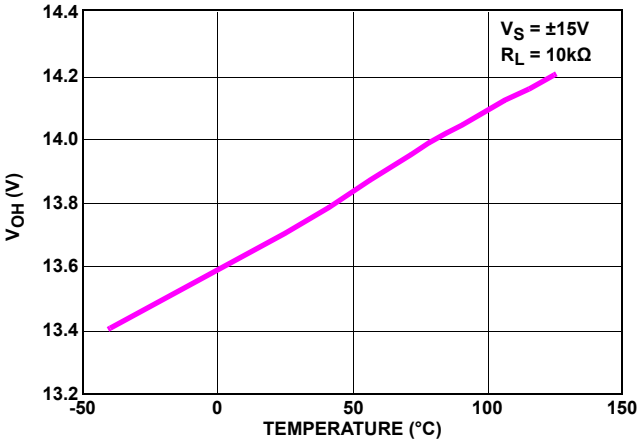


FIGURE 31. V_{OUT} vs TEMPERATURE

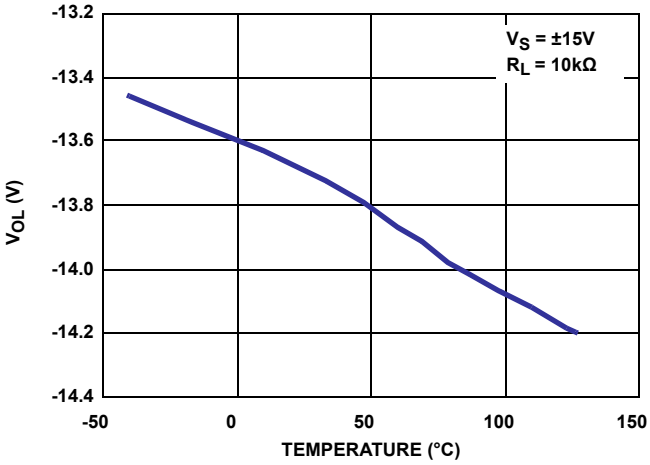


FIGURE 32. V_{OUT} vs TEMPERATURE

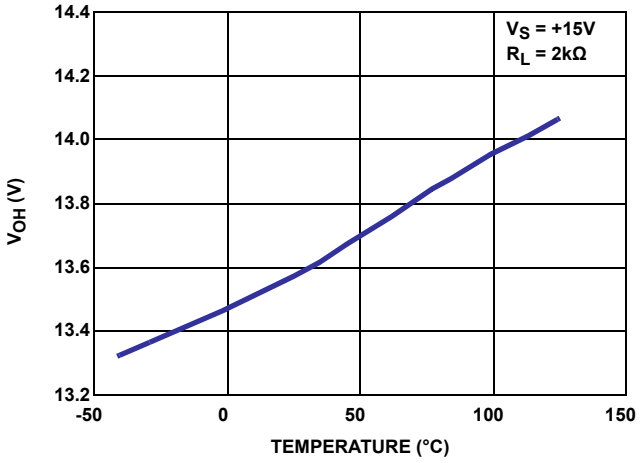


FIGURE 33. V_{OUT} vs TEMPERATURE

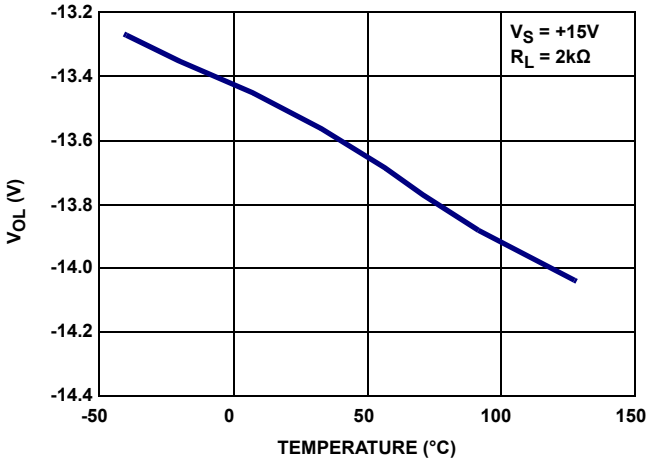


FIGURE 34. V_{OUT} vs TEMPERATURE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

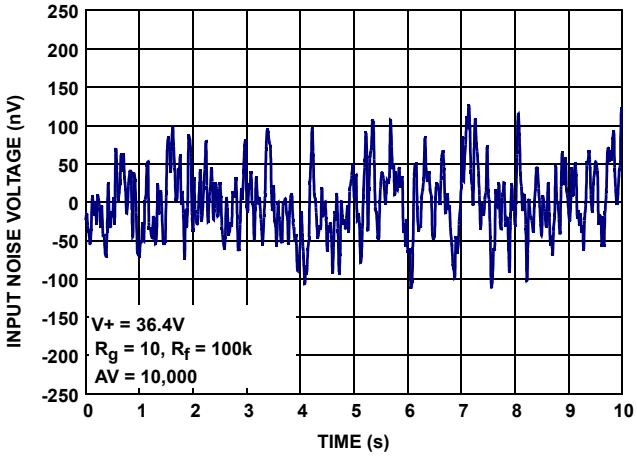


FIGURE 35. INPUT NOISE VOLTAGE 0.1Hz to 10Hz

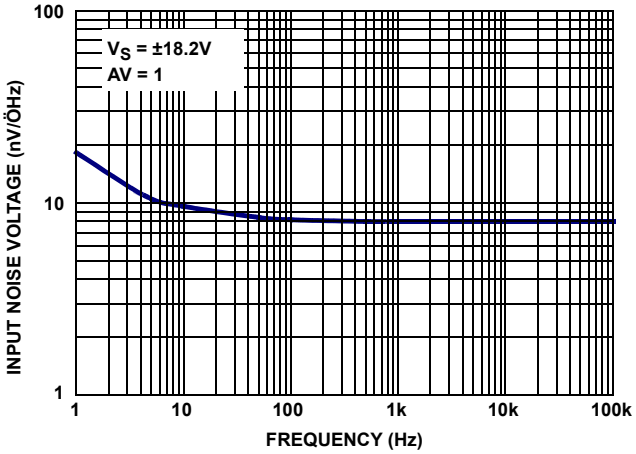


FIGURE 36. INPUT NOISE VOLTAGE SPECTRAL DENSITY

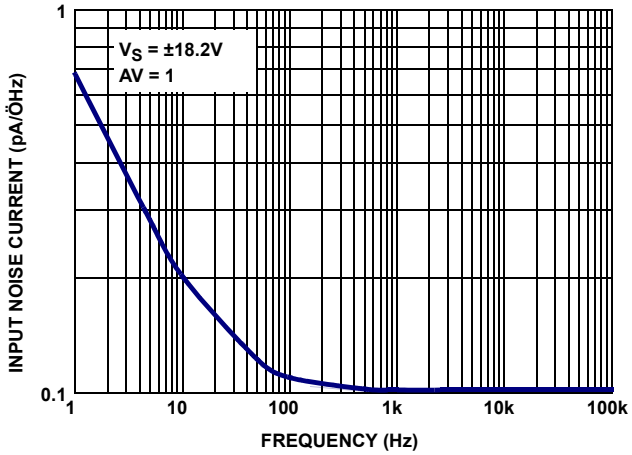


FIGURE 37. INPUT NOISE CURRENT SPECTRAL DENSITY

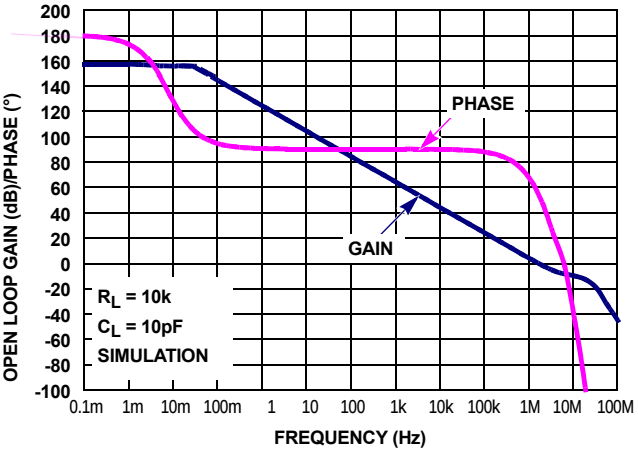


FIGURE 38. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 10pF

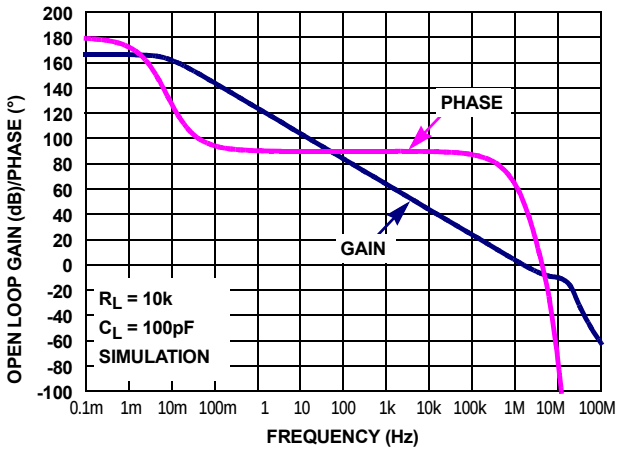


FIGURE 39. OPEN-LOOP GAIN, PHASE vs FREQUENCY, R_L = 10kΩ, C_L = 100pF

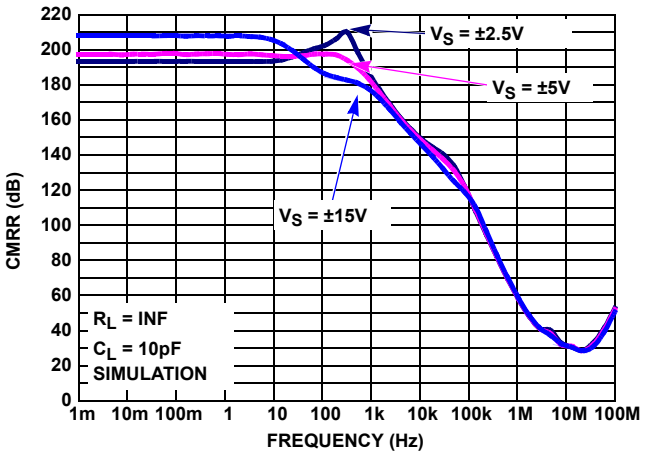


FIGURE 40. CMRR vs FREQUENCY, V_S = ±2.25, ±5V, ±15V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

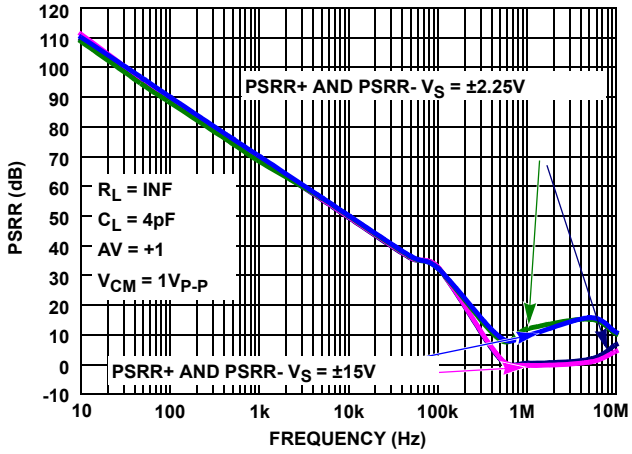


FIGURE 41. PSRR vs FREQUENCY, V_S = ±5V, ±15V

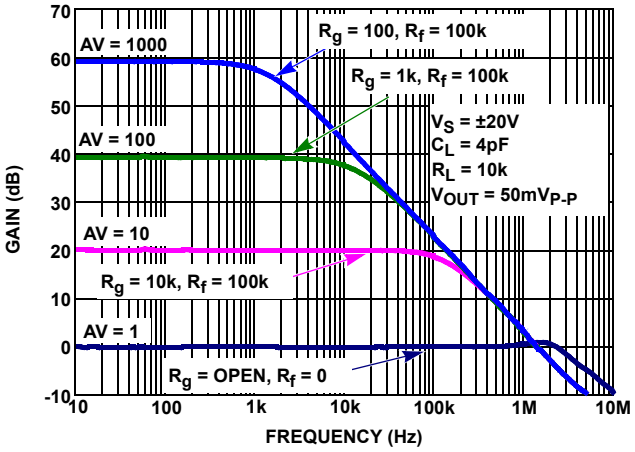


FIGURE 42. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

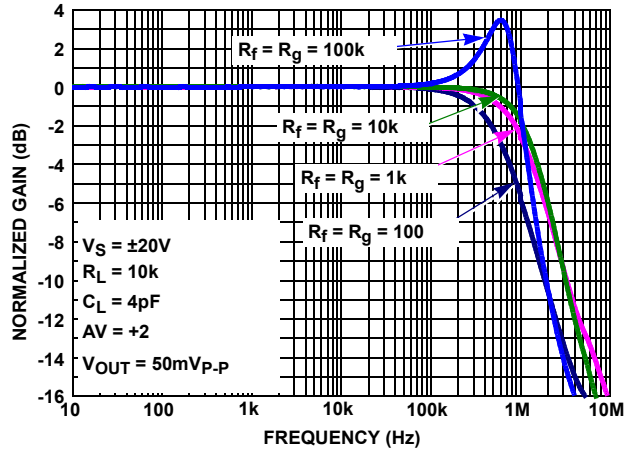


FIGURE 43. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f/R_g

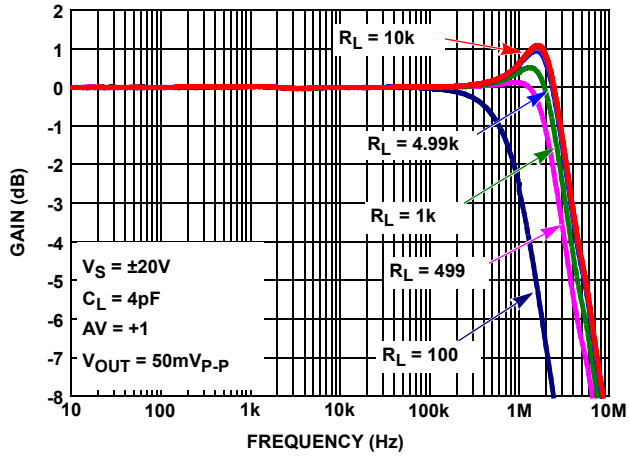


FIGURE 44. GAIN vs FREQUENCY vs R_L

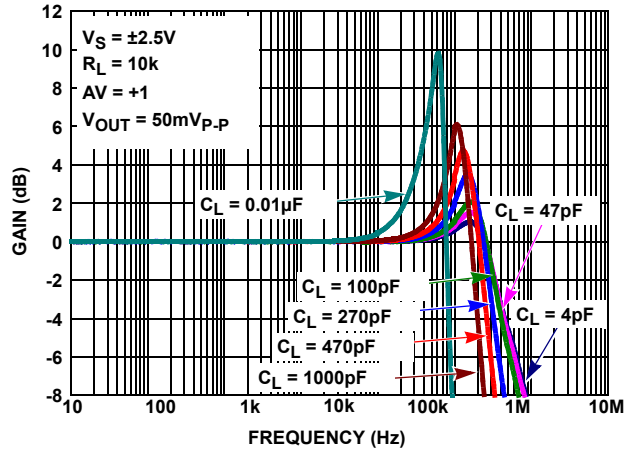


FIGURE 45. GAIN vs FREQUENCY vs C_L

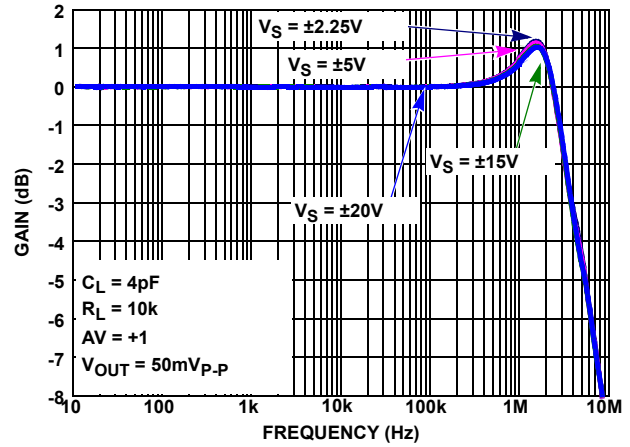


FIGURE 46. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

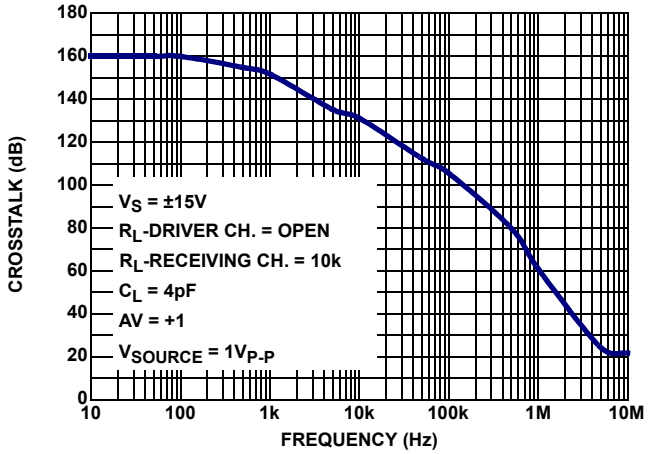


FIGURE 47. CROSSTALK, V_S = ±15V

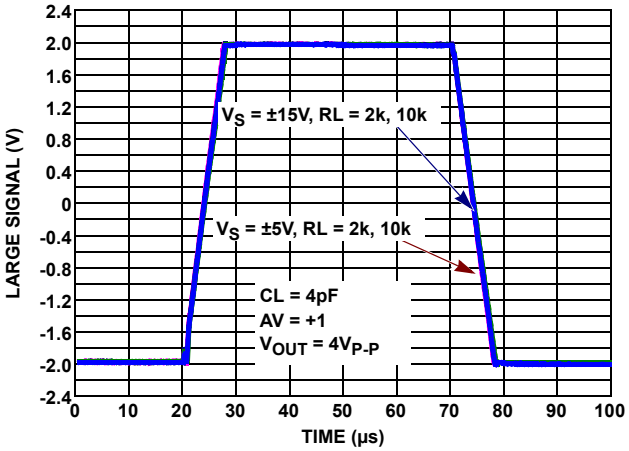


FIGURE 48. LARGE SIGNAL TRANSIENT RESPONSE vs R_L V_S = ±5V, ±15V

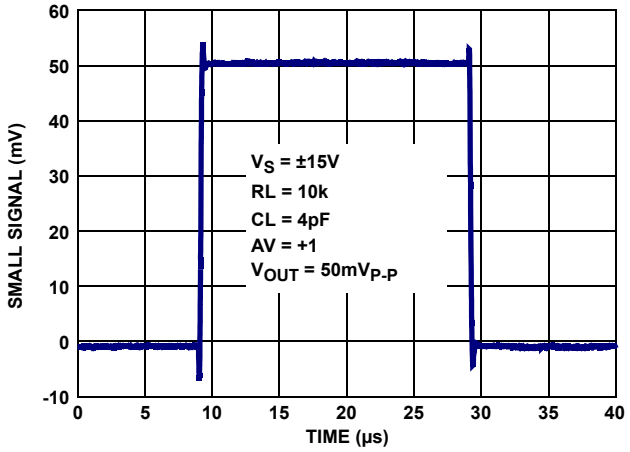


FIGURE 49. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

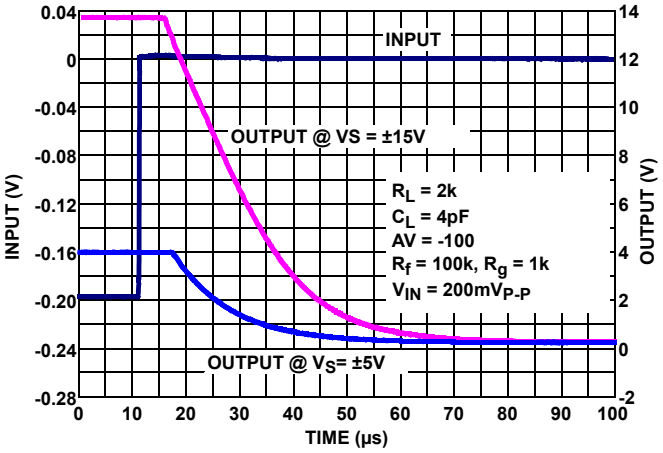


FIGURE 50. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V, ±15V

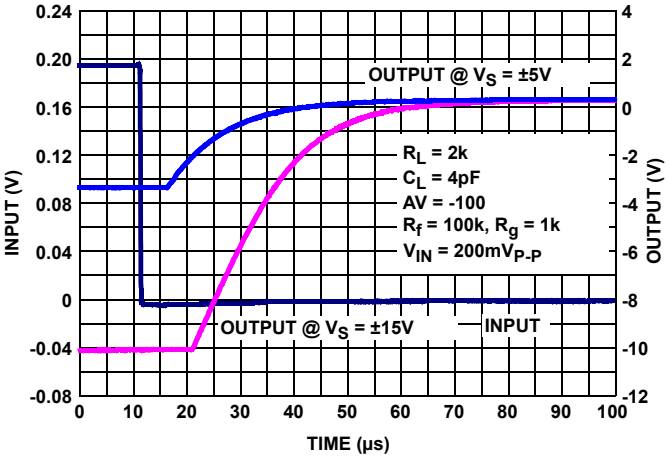


FIGURE 51. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V, ±15V

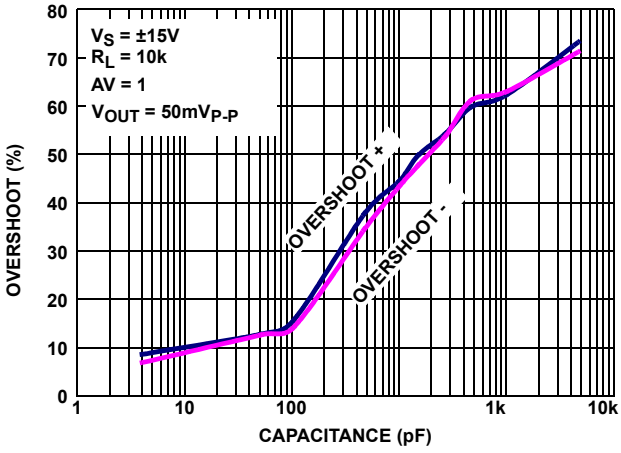


FIGURE 52. % OVERSHOOT vs LOAD CAPACITANCE, V_S = ±15V

Applications Information

Functional Description

The ISL28117, ISL28217 and ISL28417 are single, dual and quad, low noise precision op amps. Both devices are fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (180pA typical), low input offset voltage (13µV typical), low input noise voltage (8nV/√Hz), and low 1/f noise corner frequency (~8Hz). These amplifiers also feature high open loop gain (18kV/mV) for excellent CMRR (145dB) and THD+N performance (0.0005% @ 3.5V_{RMS}, 1kHz into 2kΩ). A complimentary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The devices are designed to operate over the 4.5V (±2.25V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). The Power Supply Rejection Ratio typically exceeds 140dB over the full operating voltage range and 120dB minimum over the -40°C to +125°C temperature range. The worst case common mode input voltage range over temperature is 2V to each rail. With ±15V supplies, CMRR performance is typically >130dB over-temperature. The minimum CMRR performance over the -40°C to +125°C temperature range is >120dB for power supply voltages from ±5V (10V) to ±15V (30V).

Input Performance

The super-beta NPN input pair provides excellent frequency response while maintaining high input precision. High NPN beta (>1000) reduces input bias current while maintaining good frequency response, low input bias current and low noise. Input bias cancellation circuits provide additional bias current reduction to <1nA, and excellent temperature stabilization. Figures 11 through 18 show the high degree of bias current stability at ±5V and ±15V supplies that is maintained across the -40°C to +125°C temperature range. The low bias current TC also produces very low input offset current TC, which reduces DC input offset errors in precision, high impedance amplifiers.

The +25°C maximum input offset voltage (V_{OS}) for the "B" grade is 50µV and 100µV for the "C" grade. Input offset voltage temperature coefficients ($V_{OS}TC$) are a maximum of ±0.6µV/°C for the "B" and ±0.9µV/°C for the "C" grade. Figures 3 through 6 show the typical gaussian-like distribution over the ±5V to ±15V supply range and over the full temperature range. The V_{OS} temperature behavior is smooth (Figures 7 through 10) maintaining constant TC across the entire temperature range.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 500Ω current limiting resistors and an anti-parallel diode pair across the inputs (Figure 53).

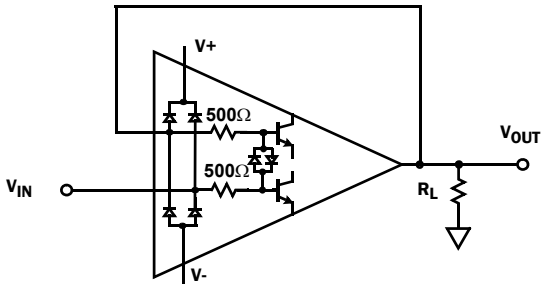


FIGURE 53. INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

The series resistors limit the high feed-through currents that can occur in pulse applications when the input dV/dT exceeds the 0.5V/µs slew rate of the amplifier. Without the series resistors, the input can forward-bias the anti-parallel diodes causing current to flow to the output resulting in severe distortion and possible diode failure. Figure 48 provides an example of distortion free large signal response using a 4V_{P-P} input pulse with an input rise time of <1ns. The series resistors enable the input differential voltage to be equal to the maximum power supply voltage (40V) without damage.

In applications where one or both amplifier input terminals are at risk of exposure to high voltages beyond the power supply rails, current limiting resistors may be needed at the input terminal to limit the current through the power supply ESD diodes to 20mA max.

Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability. Figures 27 and 28 show the current limit variation with temperature.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28117, ISL28217 and ISL28417 are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})

- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

ISL28117, ISL28217 and ISL28417 SPICE Model

Figure 54 shows the SPICE model schematic and Figure 55 shows the net list for the ISL28117, ISL28217 and ISL28417 SPICE model for a Grade “B” part. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise, Slew Rate, CMRR, Gain and Phase. The DC parameters are VOS, IOS, total supply current and output voltage swing. The model uses typical parameters given in the “Electrical Specifications” Table beginning on page 5. The AVOL is adjusted for 155dB with the dominate pole at 0.02Hz. The CMRR is set (210dB, f_{cm} = 10Hz). The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 56 through 66 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Closed Loop Gain vs RL, Large Signal Step Response, Open Loop Gain Phase and Simulated CMRR vs Frequency.

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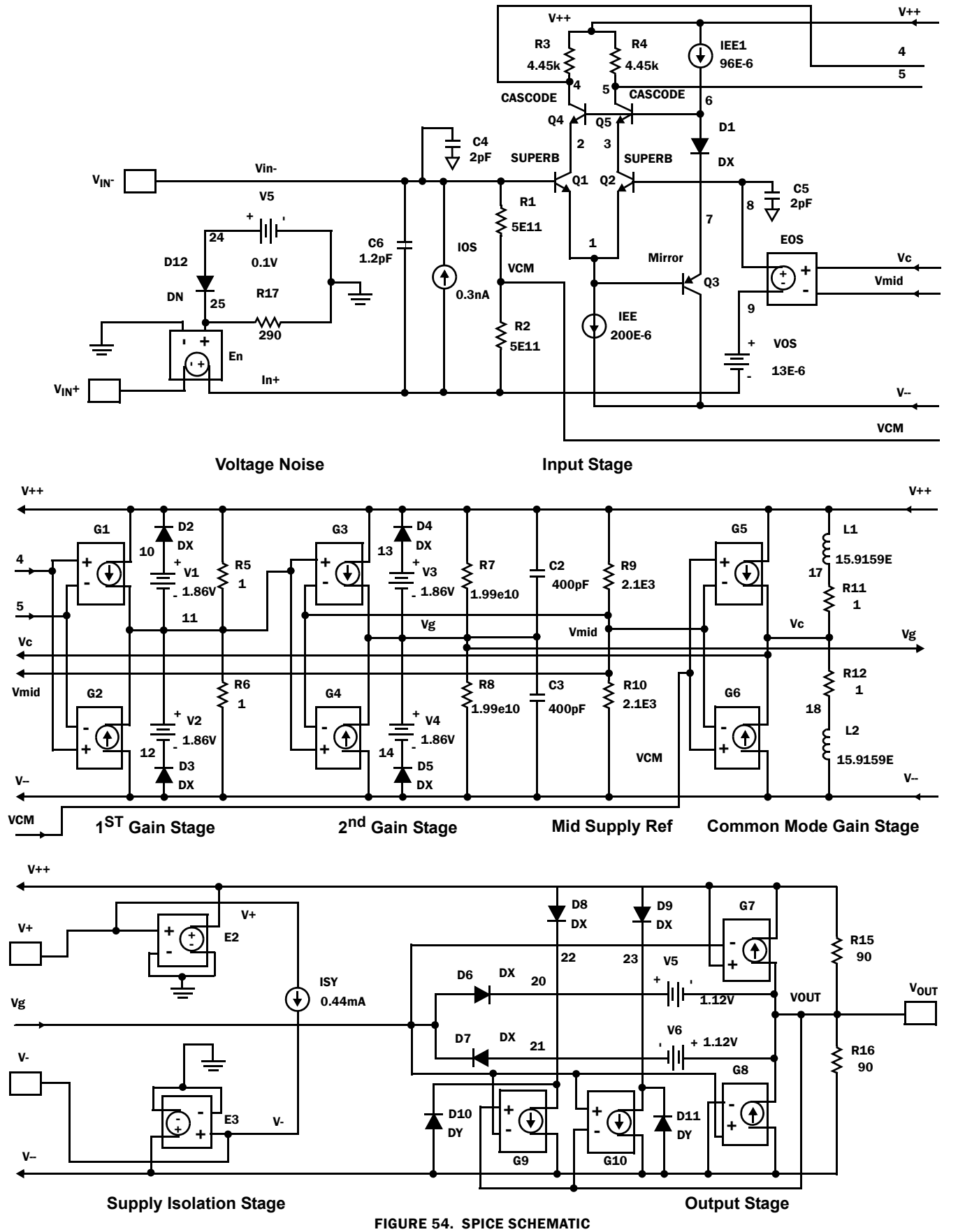


FIGURE 54. SPICE SCHEMATIC

```
* source ISL28117_SPICEmodel
* Revision B, November 20th 2009 LaFontaine
* Model for Grade B Noise, supply currents, 210dB
f=10Hz CMRR, 155dB f=0.02Hz AOL, SR = 0.5V/µsec
*Copyright 2009 by Intersil Corporation
*Refer to data sheet “LICENSE STATEMENT” Use of
*this model indicates your acceptance with the
*terms and provisions in the License Statement.
* Connections: +input
*               |    -input
*               |    |    +Vsupply
*               |    |    |    -Vsupply
*               |    |    |    |    output
*               |    |    |    |    |
.subckt ISL28117subckt Vin+ Vin-V+ V- VOUT
* source ISL28107subckt
*
*Voltage Noise
E_En          IN+ VIN+ 25 0 1
R_R17          25 0 290
D_D12          24 25 DN
V_V7          24 0 0.1
*
*Input Stage
I_IOS          IN+ VIN- DC 0.08E-9
C_C6          IN+ VIN- 1.2E-12
R_R1          VCM VIN-  5e11
R_R2          IN+ VCM  5e11
Q_Q1          2 VIN- 1 SuperB
Q_Q2          3 8 1 SuperB
Q_Q3          V-- 1 7 Mirror
Q_Q4          4 6 2 Cascode
Q_Q5          5 6 3 Cascode
R_R3          4 V++ 4.45e3
R_R4          5 V++ 4.45e3
C_C4 VIN- 0  2e-12
C_C5 8 0  2e-12
D_D1          6 7 DX
I_IEE          1 V-- DC 200e-6
I_IEE1          V++ 6 DC 96e-6
V_VOS          9 IN+ 8e-6
E_EOS          8 9 VC VMID 1
*
*1st Gain Stage
G_G1          V++ 11 4 5 8.129384e-2
G_G2          V-- 11 4 5 8.129384e-2
R_R5          11 V++ 1
R_R6          V-- 11  1
D_D2          10 V++ DX
D_D3          V-- 12 DX
V_V1          10 11 1.86
V_V2          11 12 1.86
*
*2nd Gain Stage
G_G3          V++ VG 11 VMID 2.83e-3
G_G4          V-- VG 11 VMID 2.83e-3
R_R7          VG V++ 1.99e10
R_R8          V-- VG 1.99e10
C_C2          VG V++ 4e-10
C_C3          V-- VG 4e-10
D_D4          13 V++ DX
D_D5          V-- 14 DX
V_V3          13 VG 1.86
V_V4          VG 14 1.86
*
*Mid supply Ref
R_R9          VMID V++ 2.1E3
R_R10          V-- VMID  2.1E3
I_ISY     V+ V- DC 0.44E-3
E_E2          V++ 0 V+ 0 1
E_E3          V-- 0 V- 0 1
*
*Common Mode Gain Stage with Zero
G_G5          V++ VC VCM VMID 3.162277
G_G6          V-- VC VCM VMID 3.162277
R_R11          VC 17  1
R_R12          18 VC  1
L_L1          17 V++ 15.9159E-3
L_L2          18 V-- 15.9159E-3
*
*Output Stage with Correction Current Sources
G_G7          VOUT V++ V++ VG 1.11e-2
G_G8          V-- VOUT VG V-- 1.11e-2
G_G9          22 V-- VOUT VG 1.11e-2
G_G10          23 V-- VG VOUT 1.11e-2
D_D6          VG 20 DX
D_D7          21 VG DX
D_D8          V++ 22 DX
D_D9          V++ 23 DX
D_D10          V-- 22 DY
D_D11          V-- 23 DY
V_V5          20 VOUT 1.12
V_V6          VOUT 21 1.12
R_R15          VOUT V++ 9E1
R_R16          V-- VOUT  9E1
*
.model SuperB npn
+ is=184E-15 bf=30e3 va=15 ik=70E-3 rb=50
+ re=0.065 rc=35 cje=1.5E-12 cjc=2E-12
+ kf=0 af=0
.model Cascode npn
+ is=502E-18 bf=150 va=300 ik=17E-3 rb=140
+ re=0.011 rc=900 cje=0.2E-12 cjc=0.16E-12f
+ kf=0 af=0
.model Mirror pnp
+ is=4E-15 bf=150 va=50 ik=138E-3 rb=185
+ re=0.101 rc=180 cje=1.34E-12 cjc=0.44E-12
+ kf=0 af=0
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28117subckt
```

FIGURE 55. SPICE NET LIST

Characterization vs Simulation Results

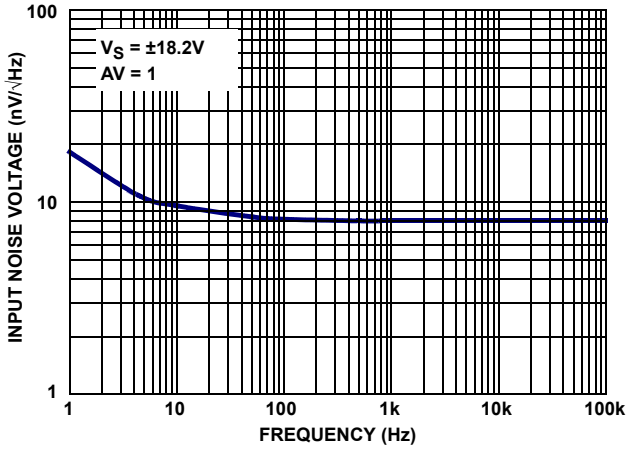


FIGURE 56. CHARACTERIZED INPUT NOISE VOLTAGE

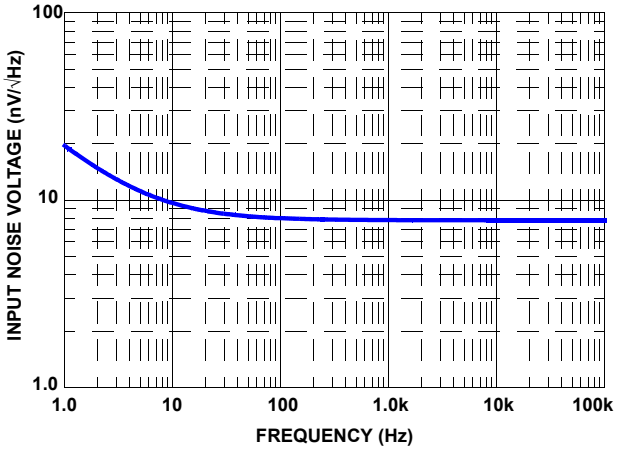


FIGURE 57. SIMULATED INPUT NOISE VOLTAGE

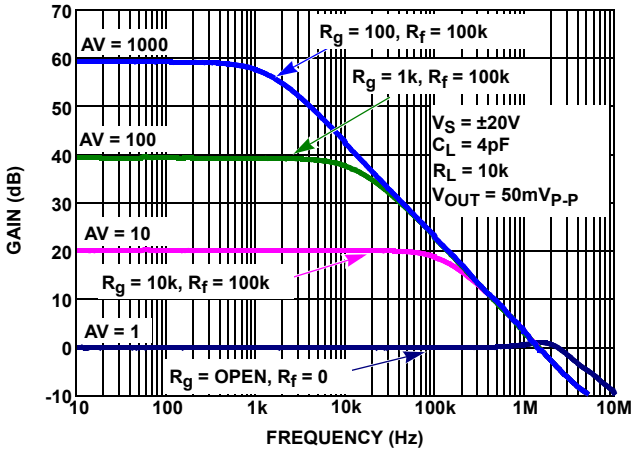


FIGURE 58. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

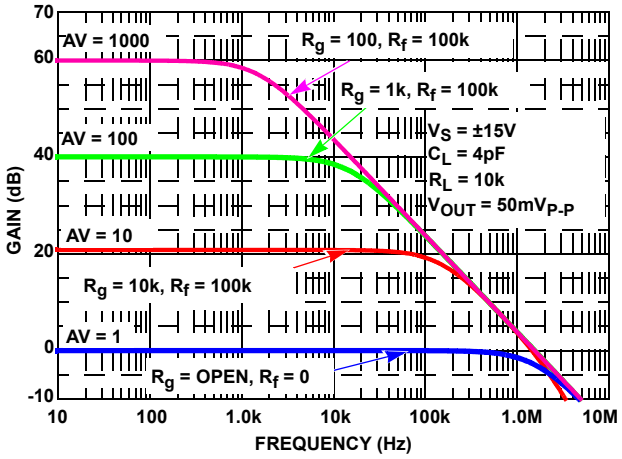


FIGURE 59. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

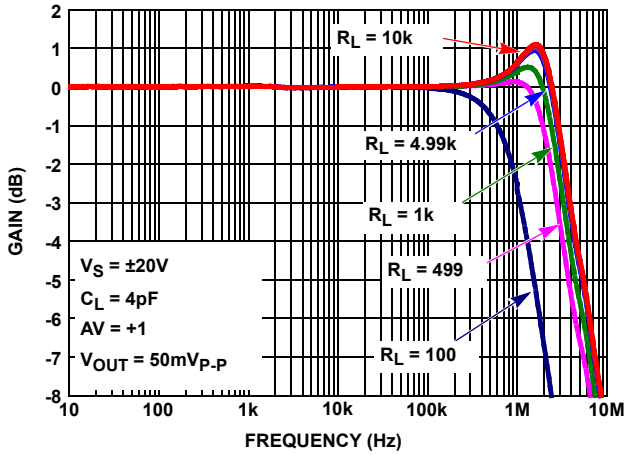


FIGURE 60. CHARACTERIZED CLOSED LOOP GAIN vs R_L

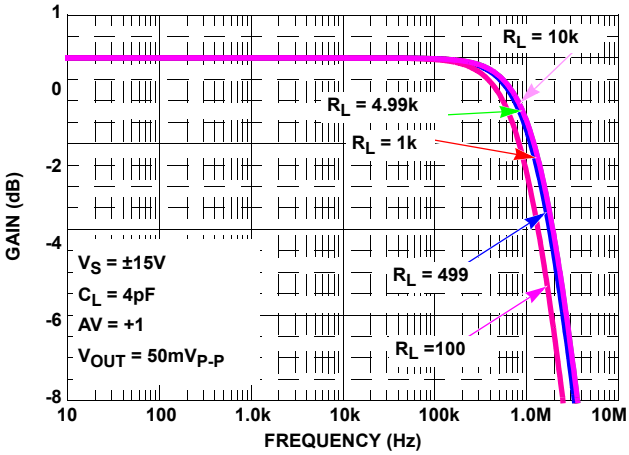


FIGURE 61. SIMULATED CLOSED LOOP GAIN vs R_L

Characterization vs Simulation Results (Continued)

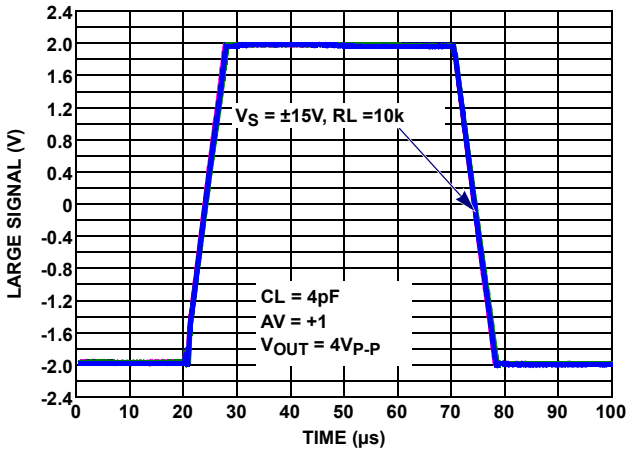


FIGURE 62. CHARACTERIZED LARGE SIGNAL TRANSIENT RESPONSE vs R_L V_S = ±15V

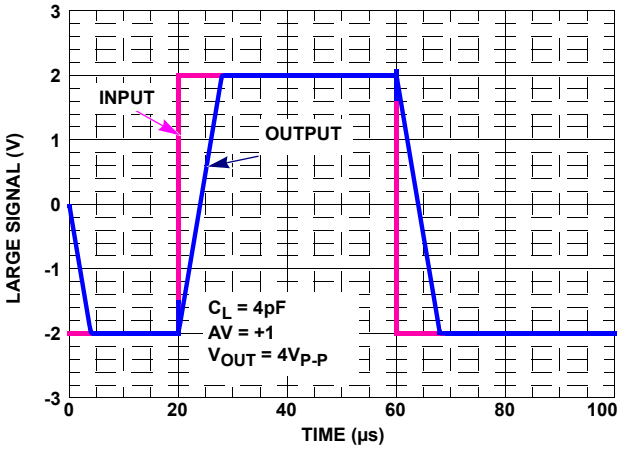


FIGURE 63. SIMULATED LARGE SIGNAL 10V STEP RESPONSE

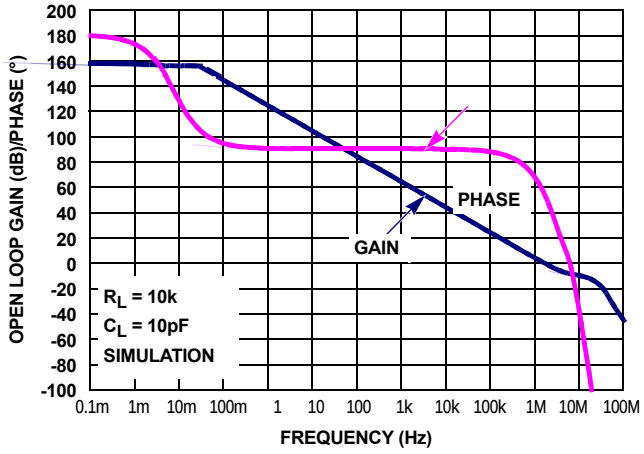


FIGURE 64. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

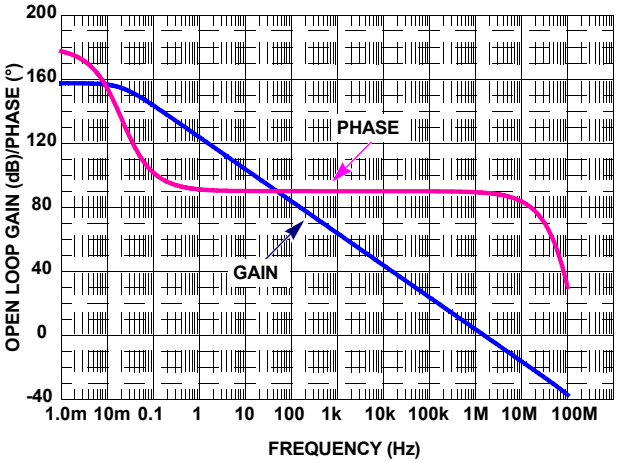


FIGURE 65. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

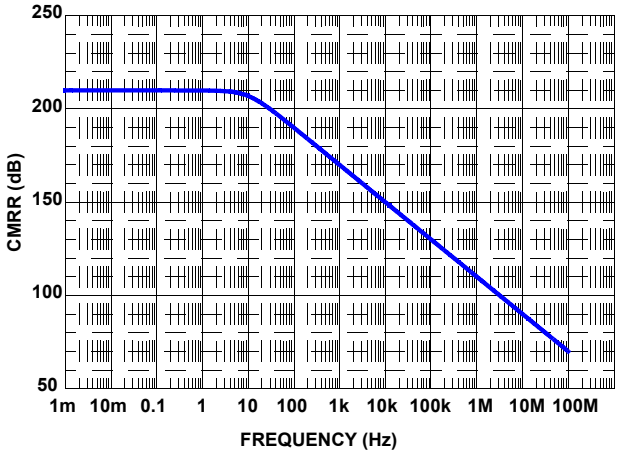


FIGURE 66. SIMULATED CMRR vs FREQUENCY

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
7/12/11	FN6632.7	1. Releasing ISL28217FUZ MSOP Grade C package. Remove 'Coming Soon' from Order Information Table 2. Page 5, added: Machine Model (ISL28217 MSOP only). . . . . 300V 3. Under Electrical Spec ±15V and ±5V tables, changed Typical Rise Time and Fall Time from: Rise Time 100ns, Fall Time 120ns, to: Rise Time 130ns, Fall Time 130ns. 4. Under Electrical Spec ±15V and ±5V table for Vos and TCVos, added in row for ISL28217 MSOP Grade C package. Added Vos and TCVos limits for 25C and Full Temp. 5. For Typical performance curves for Vos Histograms, added note that histogram is based on ISL28217FBBZ for Grade B figures and ISL28217FBZ for Grade C figures. (Figures 3-6, added part number label to graph below Vs) 6. Under Electrical Spec ±15V and ±5V tables, changed TYP for Open Loop Gain from 18,000V/mV to 14,000V/mV
12/2/10	FN6632.6	1.Updated “Ordering Information” table on page 2. Removed Coming Soon for ISL28117FRTBZ and ISL28117FUBZ parts. Added in the Vos (MAX) numbers in those rows (75 and 70 respectively). 2.Corrected part marking in “Ordering Information” table on page 2 for ISL28117FRTZ from 8117 -C to -C 8117 3.Corrected part marking in “Ordering Information” table on page 2 for ISL28217FRTZ from 8217 -C to -C 8217 4.Updated Tape & Reel note in “Ordering Information” table on page 2 from "Add "-T7", "-T7A" or "-T13" suffix for tape and reel." to new standard "Add "-T*" suffix for tape and reel." The "*" covers all possible tape and reel options 5.Updated “Electrical Specifications” Table for “V_{OS}” on page 5 and “TCVOS” on page 6 a.Added data row for Offset Voltage; MSOP Grade B Package; ISL28117 b.Added data row for Offset Voltage; TDFN Grade B Package; ISL28117 c.Added data row for Input Offset Voltage Temperature Coefficient; MSOP Grade B Package; ISL28117 d.Added data row for Input Offset Voltage Temperature Coefficient; TDFN Grade B Package; ISL28117 6.Removed "Temperature data established by characterization" from common conditions of spec table. Removed note "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." from Min Max columns of spec table. Replaced with new standard note in Min Max columns, “Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.”
8/31/10	FN6632.5	1.General changes: a.Added in Quad devices to the datasheet for SOIC, TSSOP and QFN packages. b.Added in TDFN packages for single and dual devices. c.Added in new VOS and TCVOS limits for TDFN packages d.Added Tja and Tjc Notes for TDFN Package which are “direct attach (Tja) ” and “bottom (Tjc)” 2.Specific changes: a. Added in ISL28417 to title and front page info on page 1 b. Added in ISL28117FRTZ, ISL28117FRTBZ, ISL28217FRTZ, ISL28217FRTBZ, ISL28417FBZ, ISL28417FVZ, and ISL28417FRZ packages to Ordering information on page 2 and page 2. Added in -T7 and -T7A tape and reel extensions where applicable. c. Added in TDFN, 14 Ld SOIC, 14 Ld TSSOP and 16 Ld QFN to pin configurations on page 3 and page 3. d. Updated Pin Descriptions tables with new added in packages on page 4. e. Abs Max Table added in thermal packaging info for TDFN packages on page 5. f. Electrical Specifications Table - Added two new line items for VOS spec. TDFN package ISL28217 Grade B limits ±70uV 25C and ±140uV full temp. TDFN package ISL28x17 Grade C limits ±150uV 25C and ±250uV full temp on page 5 and page 7. g. Electrical Specifications Table - Added two new line items for TCVOS spec. TDFN package ISL28217 Grade B limits ±0.7uV/C full temp. TDFN package ISL28x17 Grade C limits ±1uV/C on page 6 and page 8. h. Added in PODs for L8.3x3A, M14.15, M14.173, and L16.4x4

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev. **(Continued)**

DATE	REVISION	CHANGE
3/18/10	FN6632.4	1. Updated “Ordering Information” on page 2 by adding two rows for MSOP packages ISL28117FUBZ and ISL28117FUZ, which are scheduled to release Q2 2010. Added Pinout accordingly. 2. Added POD for MSOP M8.118 to the end of datasheet 3. In “Ordering Information” on page 2, Separated each part number with it's own specific -T7 and -T13 suffix and removed “Add “-T7” or “-T13” suffix for Tape and Reel.” from Note 1. 4. Updated ±15 and ±5V Electrical Specification table with the following edits: A) Separated VOS specs for SOIC and MSOP Grade C packages. Added new VOS specs for MSOP Grade C package. B) Separated TCVOS specs for SOIC and MSOP Grade C packages. Added new TCVOS specs for MSOP Grade C package. 5. Added “Thermal Information” on page 5 for ISL28117 MSOP package.
3/3/10		Added “Related Literature” on page 1. Added Evaluation Boards to “Ordering Information” on page 2. Added Theta JC values to “Thermal Information” on page 5. Added applicable Theta JC Note 7. Updated Theta JA for ISL28217 8 Ld SOIC from 115°C/W to 105°C/W.
1/21/10		Part marking in “Ordering Information” on page 2 changed as follows: ISL28117FBBZ changed from "28117 FBZ -B" to "28117 FBZ" ISL28117FBZ changed from "28117 FBZ" to "28117 FBZ -C" ISL28217FBBZ changed from "28217 FBZ -B" to "28217 FBZ" ISL28217FBZ changed from "28217 FBZ" to "28217 FBZ -C"
12/24/09		On page 9: Changed label in Figure 3 from “V_S = +5V” to “V_S = ±5V” On page 9: Changed label in Figure 4 from “V_S = +15V” to “V_S = ±15V”
11/25/09		Changed Typical VOS spec from “13” to “8” (B Grade), “19” to “4” (C Grade), IB from “0.18” to “0.08, IOS from “0.3” to “0.08”. Edited Spice Schematic - L1 from “95.4957” to “15.9159E”, R1 from “6k” to 1, R9 from “1” to “2.1E3”, R10 from “1” to “2.1E3, R12 from “6k” to “1”, L2 from “95.4957” to “15.9159E”. Edited Spice Net List - Changed Revision from “A” to “B”, Date change from “October 29th 2009” to “November 20th 2009”, added after AOL “SR = 0.5V/µsec, Input Stage changed in I_IOS from “0.3E-9” to 0.08E-9”, V_VOS “13e-6” to “8e-6”, Mid supply Ref R_R9 and R_R10 changed “1” to “2.1E3”, Common Mode Gain Stage with Zero change in G_G5 and G_G6 “5.27046e-15” to “3.162277”, R_R11 and R_R12 “6.3” to “1”, L_L1 and L_L2 “95.4957” to “15.9159E-3”
11/12/09	FN6632.3	Updated Typical Performance Curves Figure 5, 7, 9, 11, 13, 15, 17 and 19. Added Spice Model and license statement. Replaced typical application schematic .
10/16/09	FN6632.2	On page 2 “Ordering Information”, changed the following: a) corrected part marking for ISL28117FBBZ from "28117 -B FBZ" to "28117 FBZ -B". Corrected part marking for ISL28217FBBZ from "28217-B FBZ" to "28217 FBZ -B" B) Updated package outline drawing to most recent revision (no changes were made to package dimensions; land pattern was added and dimensions were moved from table onto drawing) c) Added "Add “-T7” or “-T13” suffix for tape and reel." to the tape and reel Note 1. d) added Note 3 callout to all parts (Note 3 reads: "For Moisture Sensitivity Level (MSL), please see device information page for ISL28117, ISL28217. For more information on MSL please see techbrief TB363.") e) removed "Coming Soon" from ISL28117FBBZ, ISL28117FBZ & ISL28217FBBZ devices
10/08/09	FN6632.1	1. Removed “very” from “...low noise..” 1st sentence, page 1. 2. Removed “Low” from 6th bullet under features, page 1. 3. Modified typical characteristics curves to show conservative performance. Specific channel designations removed. On temperature curves, changed formatting to indicate range from typical value. Changes include: a. Removed former Figures 1, 3, 5, 7, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37 & 38 (all Channel A curves) b. Replaced former Figures 19, 20, 23, 24, 27, 28, 31, 32, 35, 36, 39 & 40 with new Figures 9 thru 20 (all “conservative channels”) c. Added Figures 30, 31, 32 4. Updated TCVos histogram on page 1 to match TCVos histogram Figure 6 on page 7 (same graphic) 5. Added temp labels to Figures 28 & 29
09/03/09	FN6632.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28117, ISL28217, ISL28417

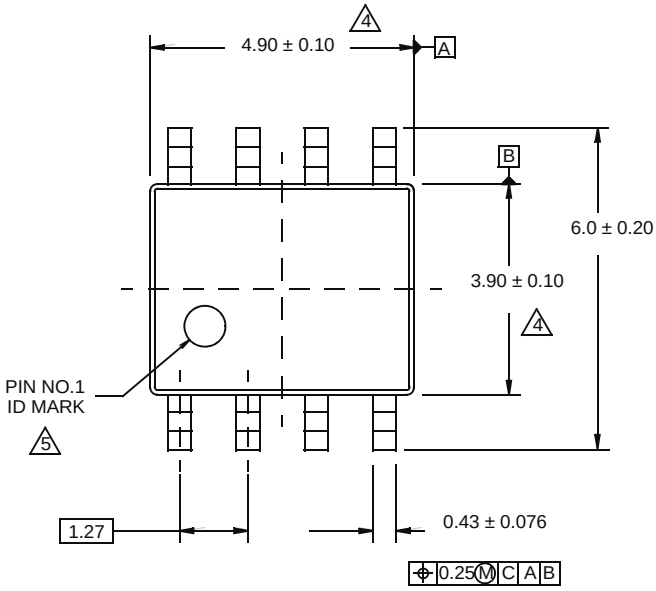
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

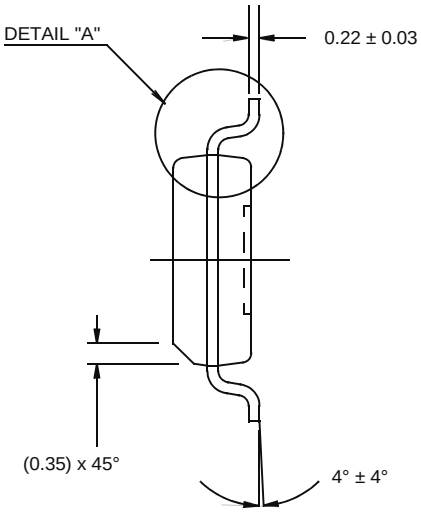
Package Outline Drawing

M8.15E

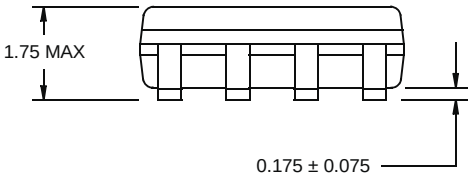
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



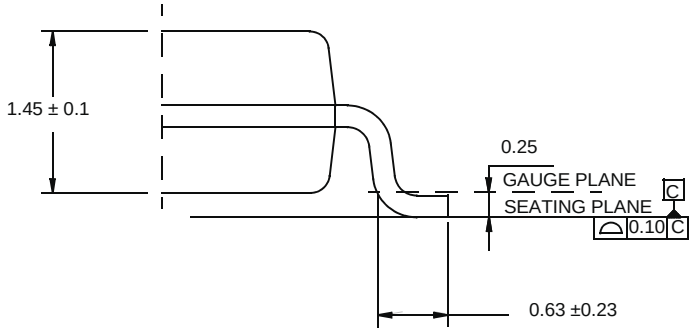
TOP VIEW



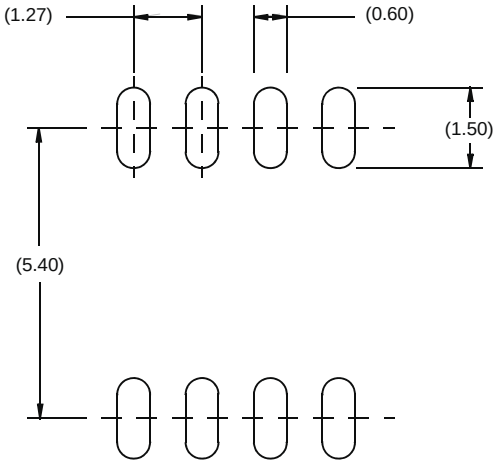
SIDE VIEW “B”



SIDE VIEW “A”



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

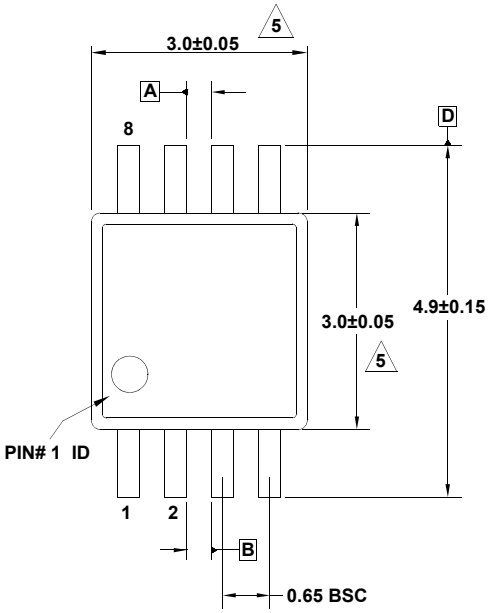
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

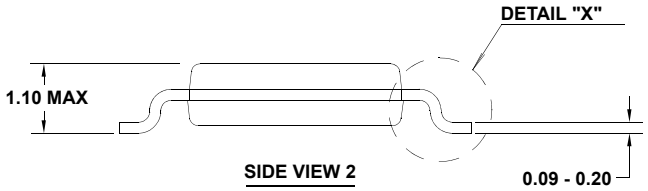
Package Outline Drawing

M8.118

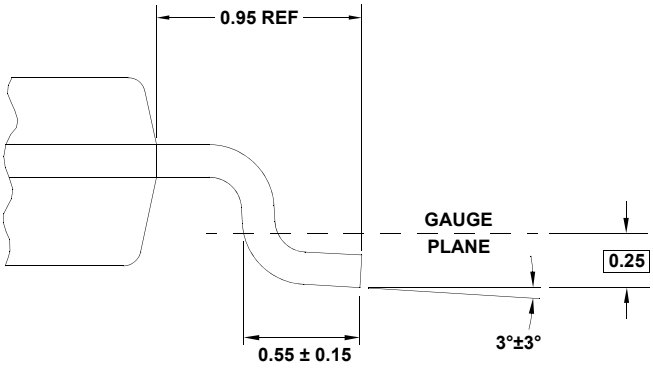
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 3, 3/10



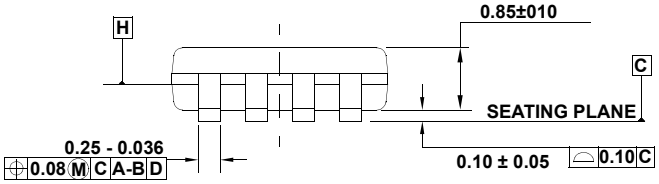
TOP VIEW



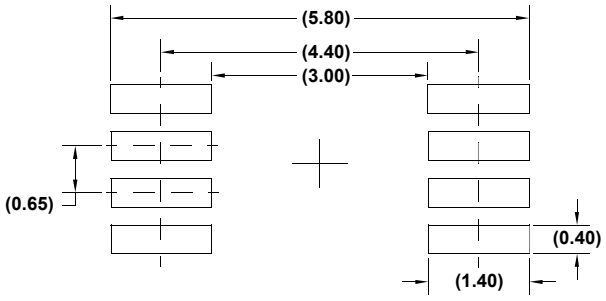
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

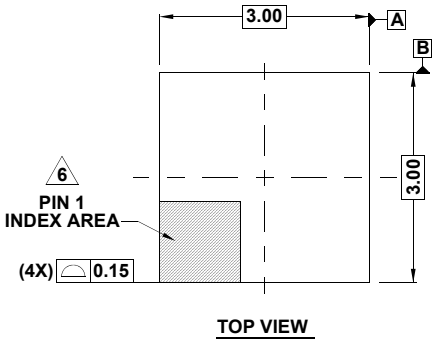
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

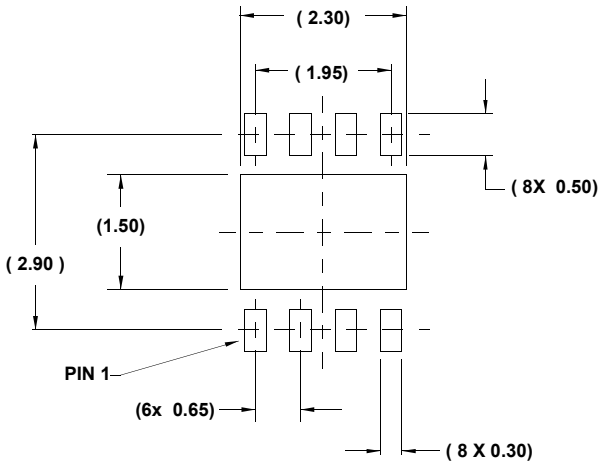
Package Outline Drawing

L8.3x3A

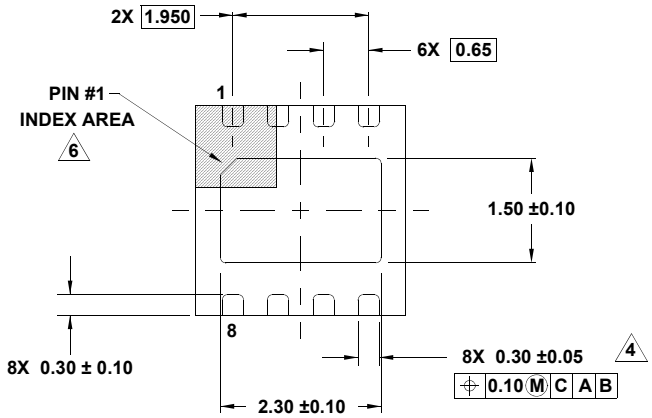
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 2/10



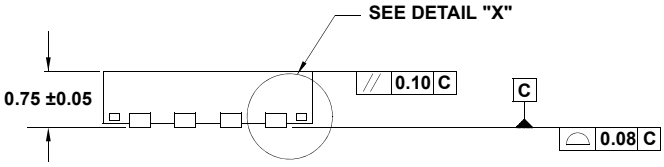
TOP VIEW



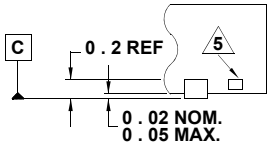
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

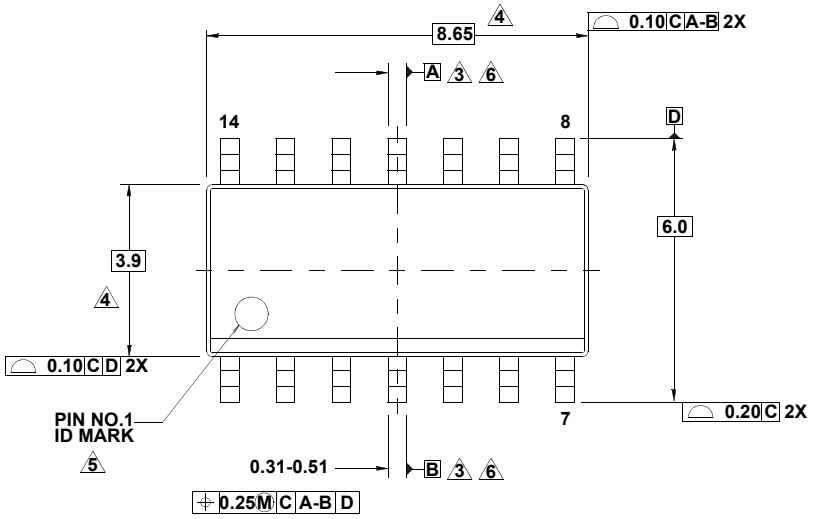
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

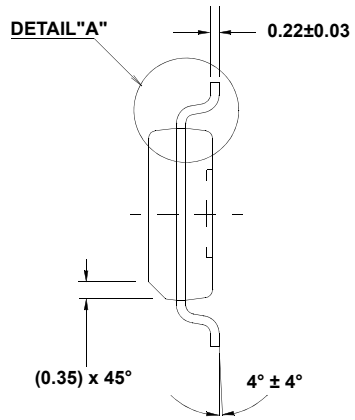
Package Outline Drawing

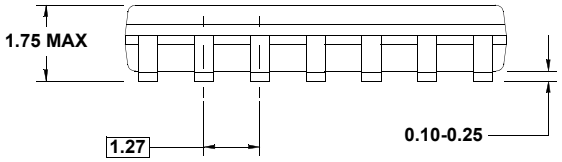
M14.15

14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 1, 10/09

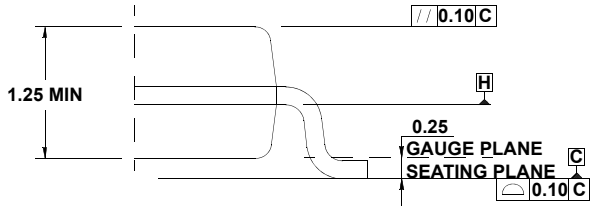


TOP VIEW

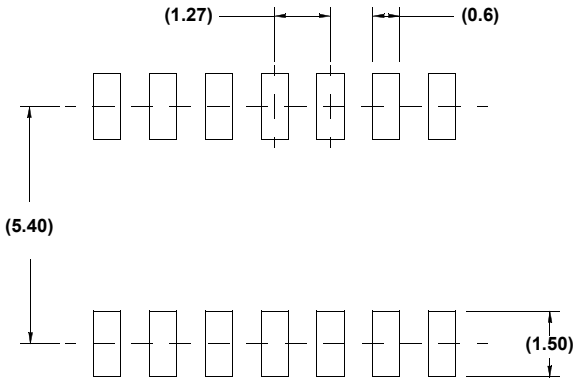




SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

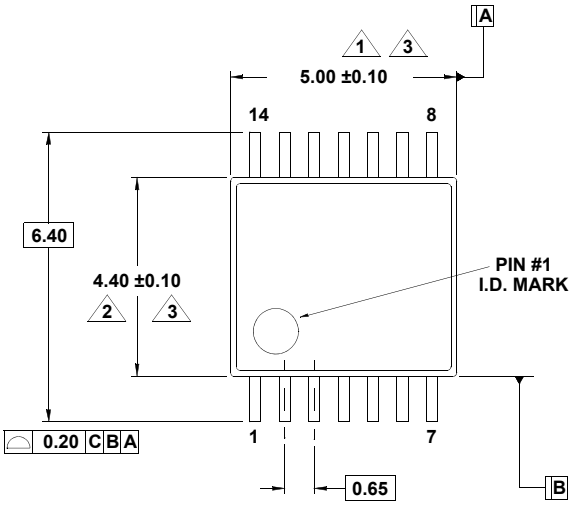
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 indentifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

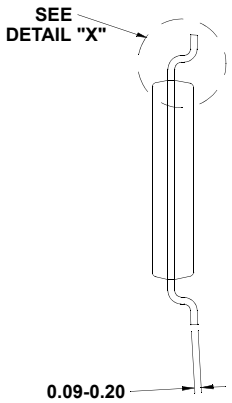
Package Outline Drawing

M14.173

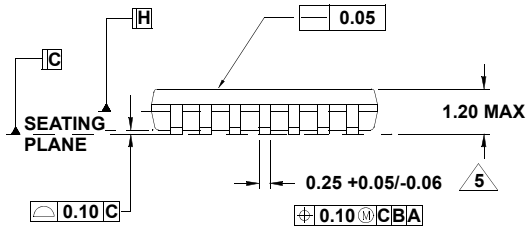
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 3, 10/09



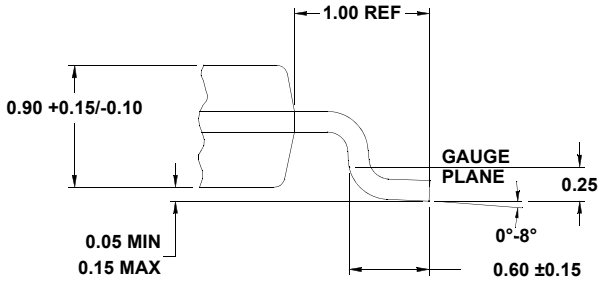
TOP VIEW



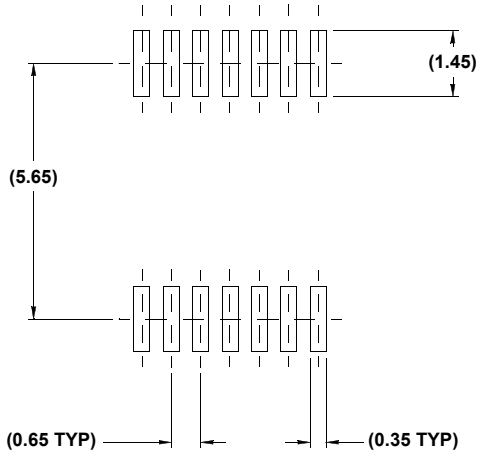
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

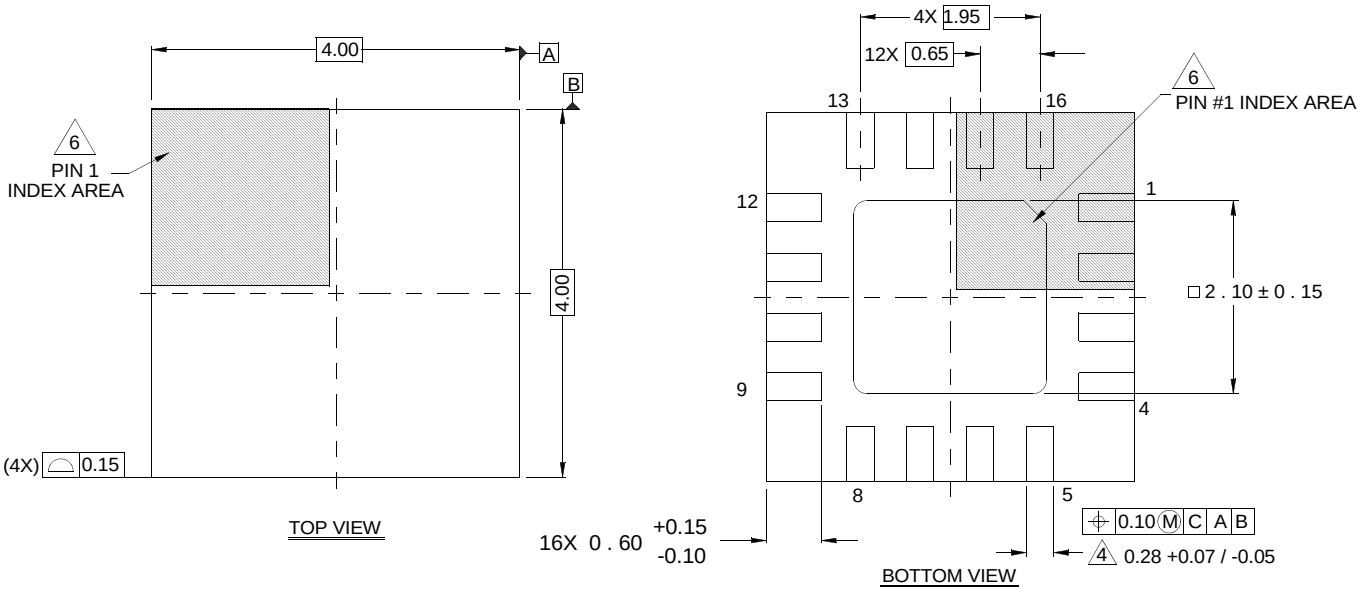
NOTES:

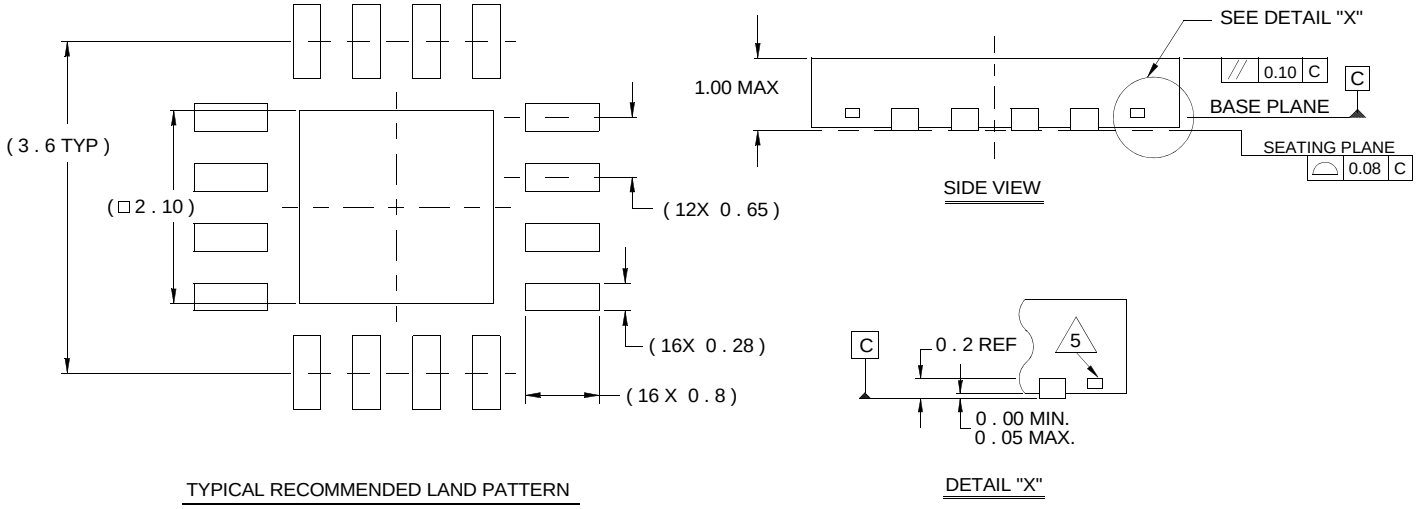
1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.

Package Outline Drawing

L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 6, 02/08





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.