Octal 8-Bit TrimDACs with Power Shutdown

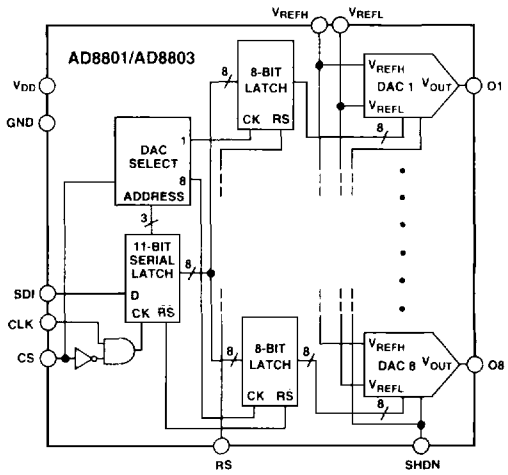
AD8801/AD8803

FEATURES
Low Cost
Replaces Eight Potentiometers
Eight Individually Programmable Outputs
Three-Wire Serial Input
Power Shutdown ≤ 25 µW Including I_{DD} and I_{REF}
Midscale Preset, AD8801
Separate V_{REFL} Range Setting, AD8803
+3 V to +5 V Single Supply Operation

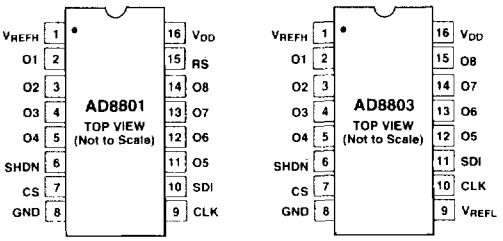
APPLICATIONS
Automatic Adjustment
Trimmer Potentiometer Replacement
Video and Audio Equipment Gain and Offset Adjustment
Portable and Battery Operated Equipment

FUNCTIONAL BLOCK DIAGRAM

(DACs 2–7 Omitted for Clarity)



PIN CONFIGURATIONS



GENERAL DESCRIPTION

The AD8801/AD8803 provides eight digitally controlled dc voltage outputs. This potentiometer divider TrimDAC® allows replacement of the mechanical trimmer function in new designs. The AD8801/AD8803 is ideal for dc voltage adjustment applications.

Easily programmed by serial interfaced microcontroller ports, the AD8801 with its midscale preset is ideal for potentiometer replacement where adjustments start at a nominal value. Applications such as gain control of video amplifiers, voltage controlled frequencies and bandwidths in video equipment, geometric correction and automatic adjustment in CRT computer graphic displays are a few of the many applications ideally suited for these parts. The AD8803 provides independent control of both the top and bottom end of the potentiometer divider allowing a separate zero-scale voltage setting determined by the V_{REFL} pin. This is helpful for maximizing the resolution of devices with a limited allowable voltage control range.

Internally the AD8801/AD8803 contain eight voltage output digital-to-analog converters, sharing a common reference voltage input.

Each DAC has its own DAC register that holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register that is loaded from a standard three-wire serial input digital interface. Eleven data bits make up the data word clocked into the serial input register. This data word is decoded where the first 3 bits determine the address of the DAC register to be loaded with the last 8 bits of data. The AD8801/AD8803 consumes only 5 µA from 5 V power supplies. In addition, in shutdown mode reference input current consumption is also reduced to 5 µA while saving the DAC latch settings for use after return to normal operation.

The AD8801/AD8803 is available in 16-pin plastic DIP and the 1.5 mm height SO-16 surface mount packages.

ORDERING GUIDE

Model	FTN	Temperature	Package Description	Package Option*
AD8801AN	$\overline{RS}$	-40°C to +85°C	P-DIP-16	N-16
AD8801AR	$\overline{RS}$	-40°C to +85°C	SO-16	R-16A
AD8803AN	REFL	-40°C to +85°C	P-DIP-16	N-16
AD8803AR	REFL	-40°C to +85°C	SO-16	R-16A

*For outline information see Package Information section.

See the AD8802/AD8804 for a twelve channel version of this product.
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AD8801/AD8803–SPECIFICATIONS (V_{DD} = +3 V ± 10% or +5 V ± 10%, V_{REFH} = +V_{DD}, V_{REFL} = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
STATIC ACCURACY						
Specifications Apply to All DACs						
Resolution	N		8			Bits
Integral Nonlinearity Error	INL		-1.5	±1/2	+1.5	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic	-1	±1/4	+1	LSB
Full-Scale Error	G_{FSE}		-4	-2.8	+0.5	LSB
Zero-Code Error	V_{ZSE}		0.5	±0.1	+0.5	LSB
DAC Output Resistance	R_{OUT}		3	5	8	kΩ
Output Resistance Match	$\Delta R/R_O$			1		%
REFERENCE INPUT						
Voltage Range[2]	V_{REFH}		0		V_{DD}	V
	V_{REFL}	Pin Available on AD8803 Only	0		V_{DD}	V
Input Resistance	R_{REFH}	Digital Inputs = 55_H, V_{REFH} = V_{DD}		2		kΩ
Reference Input Capacitance[3]	C_{REFO}	Digital Inputs All Zeros		25		pF
	C_{REFI}	Digital Inputs All Ones		25		pF
DIGITAL INPUTS						
Logic High	V_{IH}	V_{DD} = +5 V	2.4			V
Logic Low	V_{IL}	V_{DD} = +5 V			0.8	V
Logic High	V_{IH}	V_{DD} = +3 V	2.1			V
Logic Low	V_{IL}	V_{DD} = +3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V			±1	µA
Input Capacitance[3]	C_{IL}			5		pF
POWER SUPPLIES[4]						
Power Supply Range	V_{DD} Range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	V_{IH} = V_{DD} or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)	I_{DD}	V_{IH} = 2.4 V or V_{IL} = 0.8 V, V_{DD}= +5.5 V		1	4	mA
Shutdown Current	I_{REFH}	$\overline{SHDN}$ = 0		0.01	5	µA
Power Dissipation	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = 0 V, V_{DD} = +5.5 V			27.5	µW
Power Supply Sensitivity	PSRR	V_{DD} = 5 V ± 10%, V_{REFH} = +4.5 V		0.001	0.002	%/%
Power Supply Sensitivity	PSRR	V_{DD} = 3 V ± 10%, V_{REFH} = +2.7 V		0.01		%/%
DYNAMIC PERFORMANCE[5]						
V_{OUT} Settling Time (Positive or Negative)	t_S	±1/2 LSB Error Band		0.6		µs
Crosstalk	CT	See Note 5, f = 100 kHz		50		dB
SWITCHING CHARACTERISTICS[3,6]						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	15			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		10			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		10			ns
Reset Pulse Width	t_{RS}		60			ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		15			ns
$\overline{CS}$ Rise to Next Rising Clock	t_{CSI}		10			ns

NOTES

[1]Typical values represent average readings measured at +25°C.

[2]V_{REFH} can be any value between GND and V_{DD}, for the AD8803 V_{REFL} can be any value between GND and V_{DD}.

[3]Guaranteed by design and not subject to production test.

[4]Digital Input voltages V_{IN} = 0 V or V_{DD} for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from (I_{DD} × V_{DD}).

[5]Measured at a V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change.

[6]See timing diagram for location of measured values. All input control voltages are specified with t_R = t_F = 2 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.