FAIRCHILD SEMICONDUCTOR®

June 2011

FAN7319
LCD Backlight Inverter Drive IC

Features

- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range: 10V to 24V
- Backlight Lamp Ballast and Soft Dimming
- Minimal Required External Components
- Precision Voltage Reference Trimmed to 2%
- ZVS or ZCS Push-Pull & Full-Bridge Topology
- PWM Control at Fixed Frequency
- ZCS Control by Sensing Resonant Tank Current
- External Pulse Burst Dimming Function - Positive
- Analog Dimming Function - Positive
- Programmable Striking Frequency
- Open-Lamp Protection
- Open-Lamp Regulation
- Short-Lamp Protection
- CMP-High Protection
- Dynamic Contrast Ratio Mode
- Thermal Shutdown
- 20-Pin SOP

Applications

- LCD TV
- LCD Monitor

Description

The FAN7319 is a LCD backlight inverter drive IC that controls N-N push-pull topology or N-N full-bridge topology using a proprietary phase-shift method.

The FAN7319 provides a low-cost solution and reduces external components by integrating full-wave rectifiers for open-lamp protection and regulation. The operating voltage range is wide, so an external regulator isn't necessary to supply voltage to the IC.

The FAN7319 provides various protections, such as open-lamp regulation, open-lamp protection, short-lamp protection, CMP-high protection, and FB-high protection, to increase the system reliability. The FAN7319 provides burst dimming function and analog dimming.

The FAN7319 is available in a 20-Lead Small Outline Integrated Circuit (SIOC) package.

Ordering Information

Part Number	Operating Temperature	Package	Packing Method
FAN7319M	-25 to +85°C	20-Lead, SOIC, JEDEC MS-013, .300 Inch, Wide Body	Rail
FAN7319MX	-25 to +85°C		Tape & Reel

Block Diagram

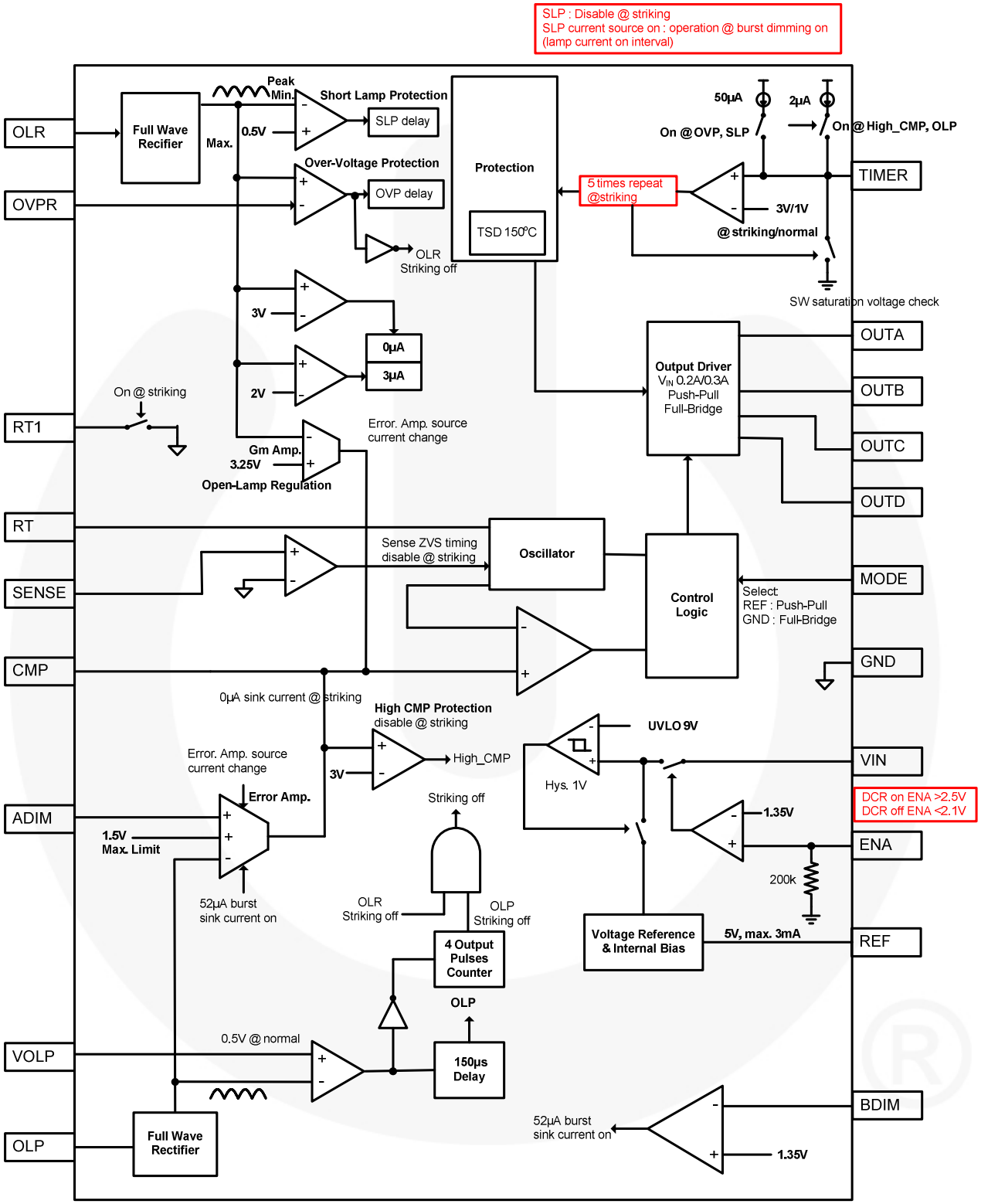
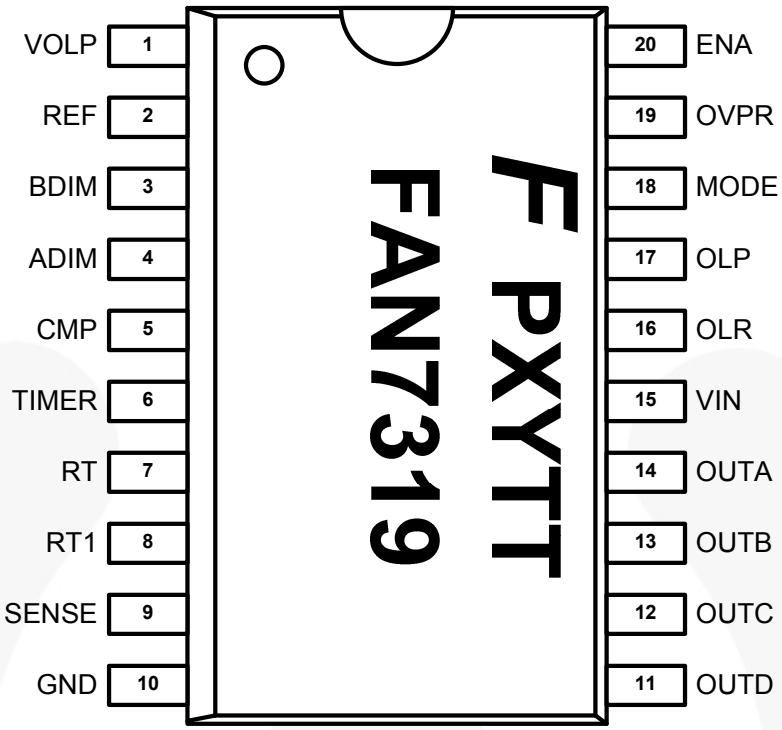


Figure 1. Internal Block Diagram

Pin Configuration



F: Fairchild Logo
P: Assembly Site Code
XY: Year & Weekly Code
TT: Die Run Code
FAN7319: Device Name

Figure 2. Pin Diagram with Top Mark

Pin Definitions

Pin #	Name	Description
1	VOLP	This pin is for reference voltage of open-lamp protection level in striking mode.
2	REF	This pin is 5V reference output.
3	BDIM	This pin is the input for burst dimming. Input type is PWM pulse signal, not DC voltage. Dimming polarity is positive.
4	ADIM	This pin is for positive analog dimming.
5	CMP	Error amplifier output. Typically, a compensation capacitor is connected to this pin from the ground.
6	TIMER	This pin is for protection delay setting. Typically, a capacitor is connected to this pin from ground. OVP/OLP/High_CMP/SLP protection time is set by this capacitor value.
7	RT	This pin is for programming the normal switching frequency. Typically, a resistor is connected to this pin from ground.
8	RT1	This pin is for programming the striking switching frequency. In striking mode, this pin is connected to ground. Typically, a resistor is connected to this pin from the RT pin.
9	SENSE	This pin is for sensing Zero Voltage Switching (ZVS) timing. If voltage cross 0V, CT voltage is reset; and operating frequency is changed by ZVS timing. If this pin is not used, it must be connected to REF.
10	GND	This pin is the ground.
11	OUTD	This pin is lower NMOS gate-drive output 2. (Push-Pull : Disabled)
12	OUTC	This pin is upper NMOS gate-drive output 2. (Push-Pull : Disabled)
13	OUTB	This pin is lower NMOS gate-drive output 1. (Push-Pull : NMOS gate-drive output 2)
14	OUTA	This pin is upper NMOS gate-drive output 1. (Push-Pull : NMOS gate-drive output 1)
15	VIN	This pin is the supply voltage of the IC.
16	OLR	This pin is for open-lamp regulation. It is connected to the full-wave rectifier internally. If two feedbacks are available, sum of feedback is inputted to this pin. When OLR input is between 2V and 3V, the error amplifier output current is limited to 3μA. When OLR input reaches 3V, the error amplifier output current is 0A and its output voltage maintains constant. OLR input is inputted to the negative of another error amplifier for feedback control of lamp voltage. When OLR input is more than 3.3V, another error amplifier for OLR is operating and lamp voltage is regulated.
17	OLP	This pin is for open-lamp protection and feedback control of lamp currents. It is connected to the full-wave rectifier internally. If two feedbacks are available, sum of rectified feedback is inputted to this pin. In striking mode, if OLP input is less than 1V; or in normal mode, if OLP input is less than 0.5V; the IC shuts down to protect the system in open-lamp condition. Shutdown time is programmed by the capacitor value connected to the TIMER pin. OLP input is inputted to the negative of the error amplifier for feedback control of lamp current.
18	MODE	This pin is for topology selection. If this pin is connected to REF, it is push-pull topology; OUTC & OUTD is disabled. If this pin is connected to GND, it is full-bridge topology.
19	OVPR	This pin is for reference voltage of Over-Voltage Protection (OVP).
20	ENA	This pin is for turning on/off the IC. If enable voltage is lower than 2.1V, DCR mode is disabled. If enable voltage is higher than 2.5V, DCR mode is activated and OLP is disabled.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	IC Supply Voltage	10	28	V
T_A	Operating Temperature Range	-25	+85	°C
T_J	Operating Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-65	+150	°C
θ_{JA}	Thermal Resistance Junction-to-Air[1,2]		90	°C/W
P_D	Power Dissipation		1.4	W

Notes:
1. Thermal resistance test board. Size: 76.2mm x 114.3mm x 1.6mm (1S0P); JEDEC standard: JESD51-2, JESD51-3.
2. Assume no ambient airflow.

Pin Breakdown Voltage

Pin #	Name	Value	Unit	Pin #	Name	Value	Unit
1	RT	7	V	11	OLR	±7	V
2	ENA	7		12	OLP	±7	
3	CMP	7		13	GND	7	
4	ADIM	7		14	OUTA	28	
5	REF	7		15	OUTB	28	
6	MODE	7		16	OUTC	28	
7	BDIM	7		17	OUTD	28	
8	OVPR	7		18	VIN	28	
9	VOLR	7		19	TIMER	7	
10	SENSE	±7		20	RT1	7	

Electrical Characteristics

For typical values, T_A = 25°C, V_{IN} = 15V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to T_A= -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Under-Voltage Lockout Section (UVLO)						
V_{th}	Start Threshold Voltage		8.0	8.7	9.4	V
V_{thhys}	Start Threshold Voltage Hysteresis		0.4	0.8	1.2	V
I_{st}	Startup Current	V_{IN} = 9.0V	40	100	120	µA
I_{op}	Operating Supply Current	V_{IN} = 15V, Not Switching	0.5	2.0	3.5	mA
ON/OFF Section						
V_{on}	On-State Input Voltage		1.4		5.0	V
V_{off}	Off-State Input Voltage				0.7	V
I_{sb}	Standby Current	V_{IN} = 15V, ENA = LOW	100	160	200	µA
R_{ENA}	Pull-Down Resistor		120	200	280	kΩ
Reference Section (Recommend 1µF X7R Capacitor)						
V_5	5V Regulation Voltage	0 ≤ I_5 ≤ 3mA	4.9	5.0	5.1	V
V_{5line}	5V Line Regulation	10 ≤ V_{IN} ≤ 24V		4	50	mV
V_{5load}	5V Load Regulation	I_5 = 3mA		4	50	mV
Oscillator Section (Main)						
f_{osc}	Oscillation Frequency	T_A = 25°C, RT = 50kΩ	48.50	50.0	51.50	kHz
		RT = 50kΩ	48.25	50.00	51.75	
f_{str}	Oscillator Frequency in Striking Mode	T_A = 25°C, RT = 50kΩ, RT1 = 100kΩ	68.90	71.45	74.00	kHz
		RT = 50kΩ, RT1 = 100kΩ	68.60	71.45	74.30	
V_{cth}	CT High Voltage			2		V
V_{ctl}	CT Low Voltage			0.45		V
Burst Dimming Section						
$V_{bdim(ON)}$	Burst Dimming On Voltage		2		5	V
$V_{bdim(Off)}$	Burst Dimming Off Voltage		0		0.8	V

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Electrical Characteristics (Continued)

For typical values, T_A = 25°C, V_{IN} = 15V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to T_A = -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Error Amplifier Section						
A_V	Open-Loop Gain(3)			24		dB
G_m	Error Amplifier Transconductance		20	40	60	μmho
I_{sin}	Output Sink Current	OLP = 2.25V	30	50	70	μA
I_{sur1}	Output Source Current 1	OLP = 0V	20	40	60	μA
I_{sur2}	Output Source Current 2	CMP = 2.7V	1.4	2.0	2.6	μA
I_{bsin}	Burst CMP Sink Current		38	52	66	μA
I_{olpi}	OLP Input Current	OLP = 2V	-1	0	1	μA
I_{olpo}	OLP Output Current	OLP = -2V	10	20	30	μA
V_{olpr}	OLP Input Voltage Range(3)		-4		4	V
V_{alim}	ADIM Limit Voltage	ADIM = 2V		1.5		V
V_{off1}	Error Amplifier Offset	T_A = 25°C, V_{ADIM} = 1V	0.97	1.00	1.03	V
		-25°C ≤ T_A ≤ 85°C, V_{ADIM} = 1V	0.96	1.00	1.04	V
Open-Lamp Regulation Section						
I_{olr1}	Error Amplifier Source Current for Open-Lamp Regulation	Striking, OLR = V_{olr1}+0.05	2.5	3.0	3.5	μA
I_{olr2}		OLR = 3.1V	-1	0	1	μA
V_{olr1}	Open-Lamp Regulation Voltage 1	Striking	1.85	2.00	2.15	V
V_{olr2}	Open-Lamp Regulation Voltage 2	Striking	2.8	3.0	3.2	V
V_{olr3}	Open-Lamp Regulation Voltage 3		3.05	3.25	3.45	V
I_{olrsi}	OLR Error Amplifier Sink Current	Normal, OLR = 3.5V	15.0	42.5	70.0	μA
I_{olri}	OLR Input Current	OLR = 2.5V	-1	0	1	μA
I_{olro}	OLR Output Current	OLR = -2.5V	15	25	35	μA
V_{olrr}	OLR Input Voltage Range(3)		-4		4	V

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Electrical Characteristics (Continued)

For typical values, T_A = 25°C, V_{IN} = 15V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to T_A= -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Protection Section						
V_{olp0}	Open-Lamp Protection Voltage 0	Open Lamp in Striking		V_{OLP}		V
V_{olp1}	Open-Lamp Protection Voltage 1	Normal, Vena = 2V	0.4	0.5	0.6	V
V_{cmpr}	CMP-High Protection Voltage		2.85	3.00	3.15	V
V_{slp}	Short-Lamp Protection Voltage	Normal, Vena = 2V	0.4	0.5	0.6	V
V_{tmr1}	Timer Threshold Voltage 1	Striking: Repeat 4 Times	2.9	3.0	3.1	V
V_{tmr2}	Timer Threshold Voltage 2	Normal	0.9	1.0	1.1	V
I_{tmr1}	Timer Current 1	Open Lamp	1.6	2.0	2.4	µA
I_{tmr2}	Timer Current 2	Short Lamp	40	50	60	µA
TSD	Thermal Shutdown			150		°C
V_{ovp}	Over-Voltage Protection Voltage			V_{OVPR}		V
V_{DCR}	ENA2.3V OLP Disable/Enable Change Voltage		2.1	2.3	2.5	V
Output Section						
V_{ndhv}	NMOS Gate High Voltage	V_{IN} = 12V	V_{IN} -0.5	V_{IN}	V_{IN} +0.5	V
V_{ndlv}	NMOS Gate Low Voltage[3]	V_{IN} = 12V	-0.3	0	0.3	V
V_{nuv}	NMOS Gate Voltage with UVLO Activated	V_{IN} = 4.5V	0		0.3	V
I_{ndsur}	NMOS Gate Drive Source Current	V_{IN} = 12V		200		mA
I_{ndsin}	NMOS Gate Drive Sink Current	V_{IN} = 12V		300		mA
Maximum / Minimum Overlap						
	Minimum Overlap Between Diagonal Switches	f_{osc} = 100kHz, *See Figure 14*		0		%
	Maximum Overlap Between Diagonal Switches	f_{osc} = 100kHz *See Figure 14*	86		90	%
Dead Time						
t_{D_AB}	NDR_A/NDR_B	*See Figure 34*	450	550	650	ns
t_{D_CD}	NDR_C/NDR_D	*See Figure 35*	450	550	650	ns

Note:

3. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

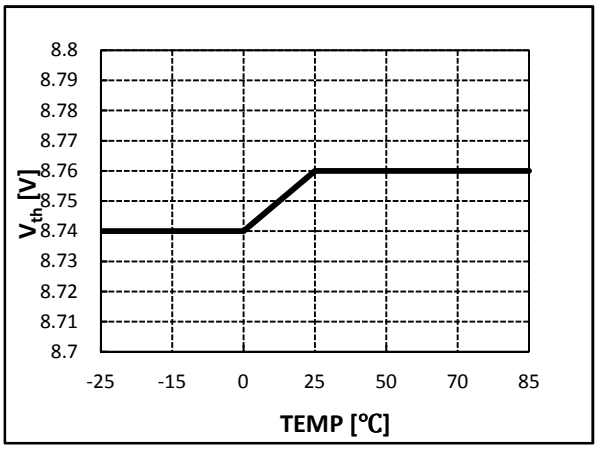

Figure 3. Start Threshold Voltage vs. Temperature

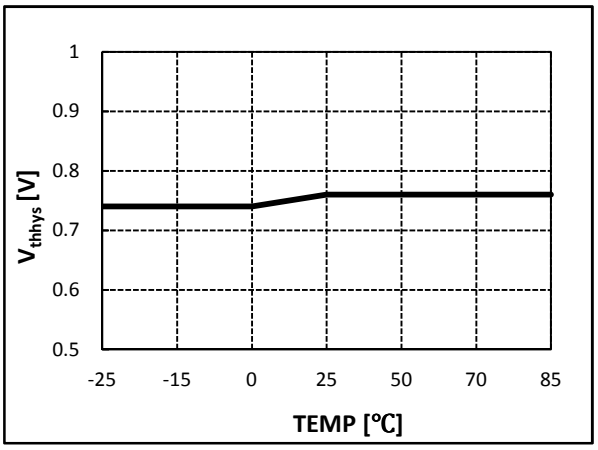

Figure 4. Start Threshold Voltage Hysteresis vs. Temperature

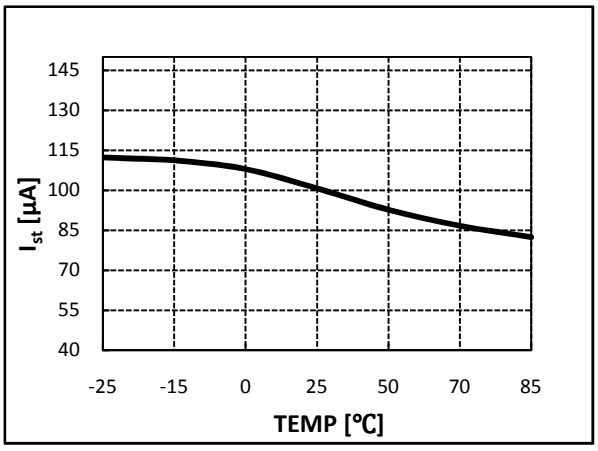

Figure 5. Startup Current vs. Temperature

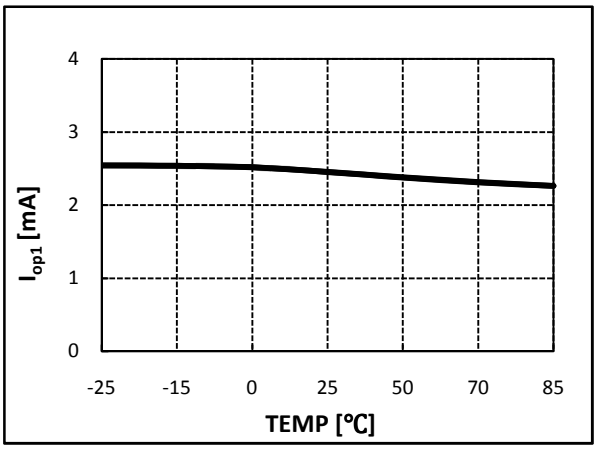

Figure 6. Operating Current vs. Temperature

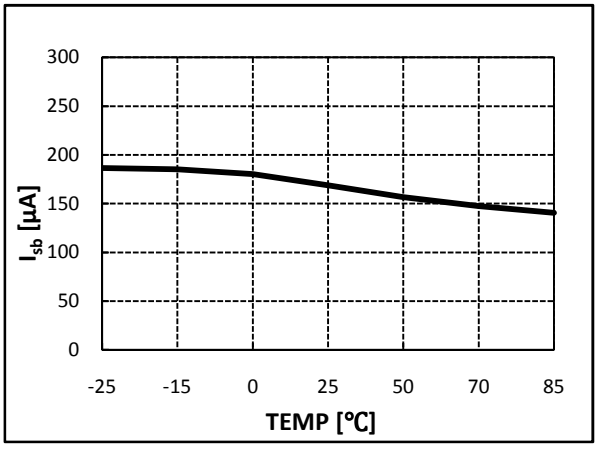

Figure 7. Standby Current vs. Temperature

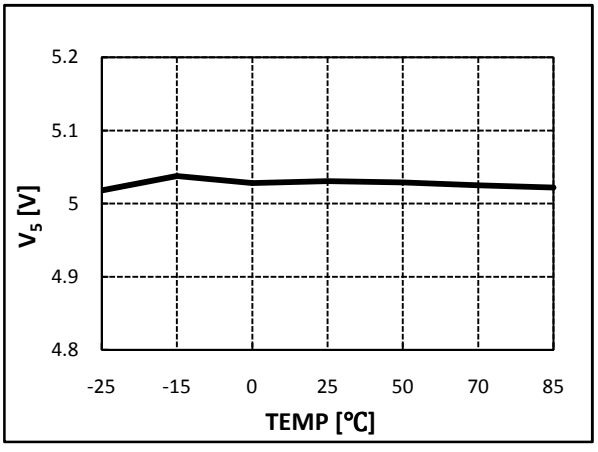

Figure 8. 5V Regulation Voltage vs. Temperature

Typical Performance Characteristics (Continued)

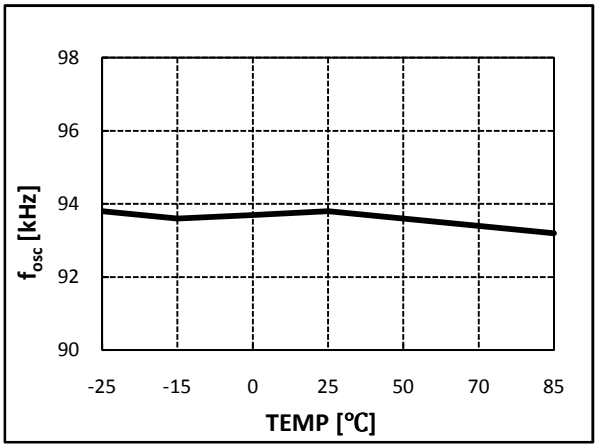

Figure 9. Oscillation Frequency vs. Temperature

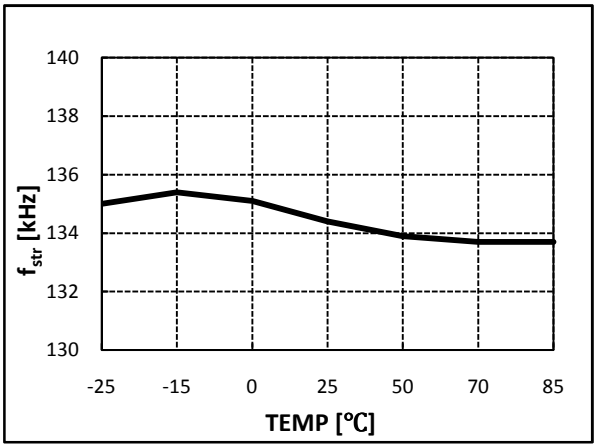

Figure 10. Oscillation Frequency in Striking vs. Temperature

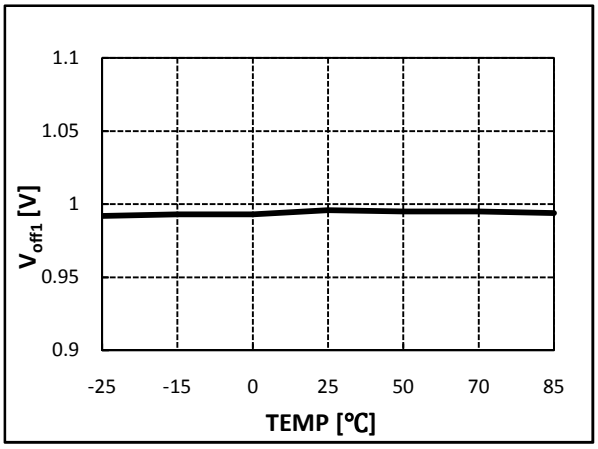

Figure 11. Error Amplifier Offset 1 vs. Temperature

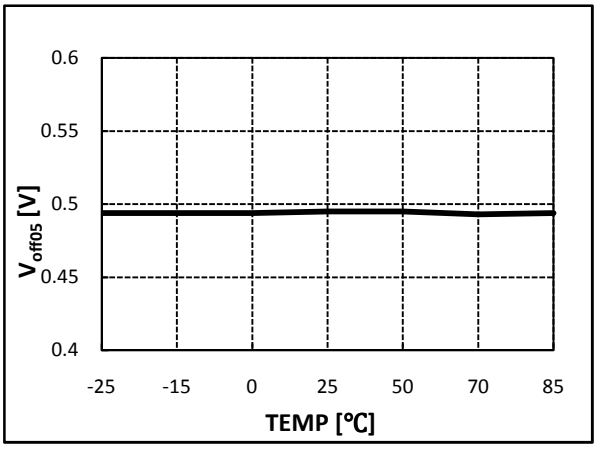

Figure 12. Error Amplifier Offset 05 vs. Temperature

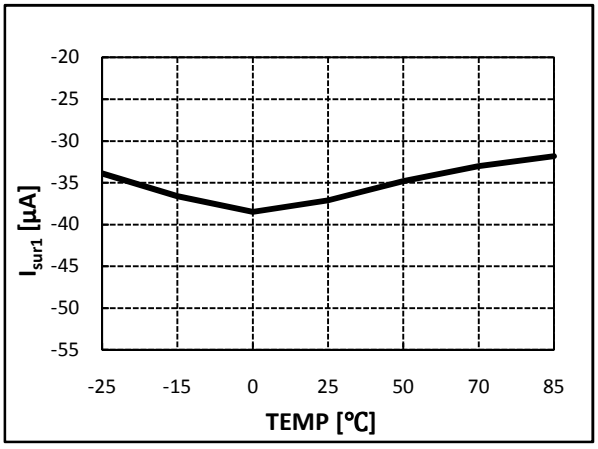

Figure 13. Error Amplifier Source Current 1 vs. Temperature

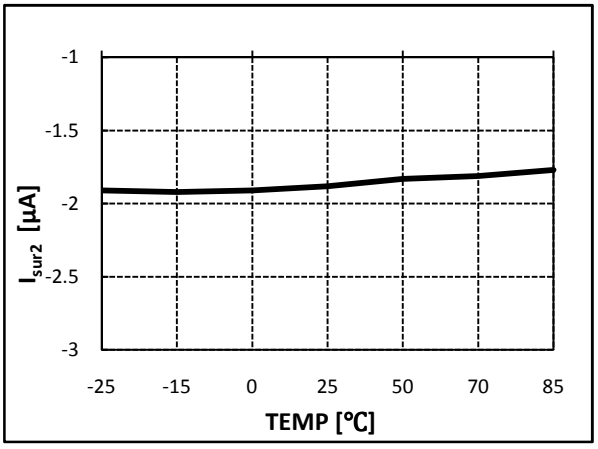

Figure 14. Error Amplifier Source Current 2 vs. Temperature

Typical Performance Characteristics (Continued)

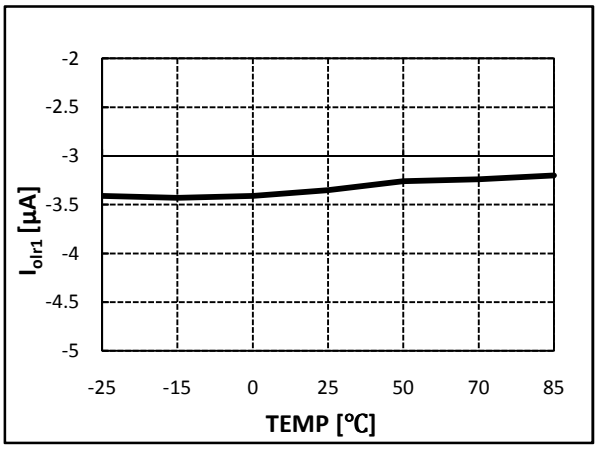

Figure 15. Error Amplifier Source Current for OLR vs. Temperature

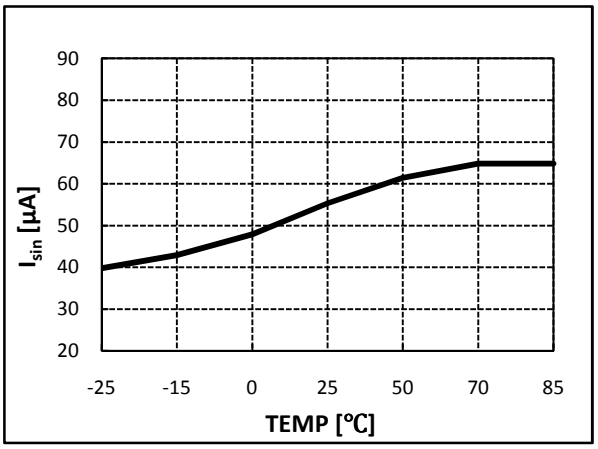

Figure 16. Error Amplifier Sink Current vs. Temperature

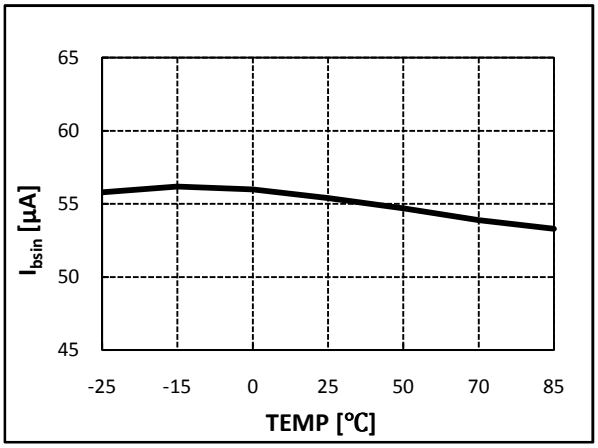

Figure 17. Burst CMP Sink Current vs. Temperature

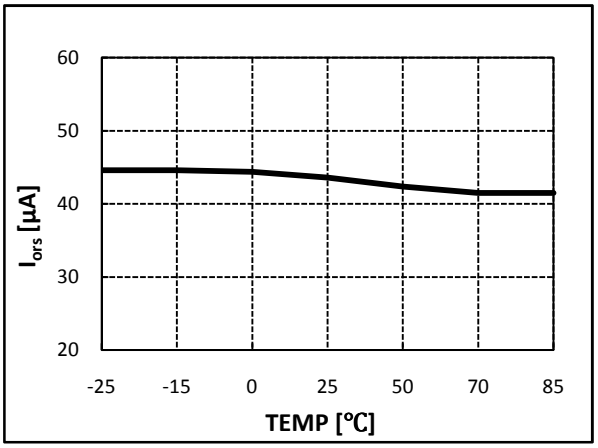

Figure 18. OLR Error Amplifier Sink Current vs. Temperature

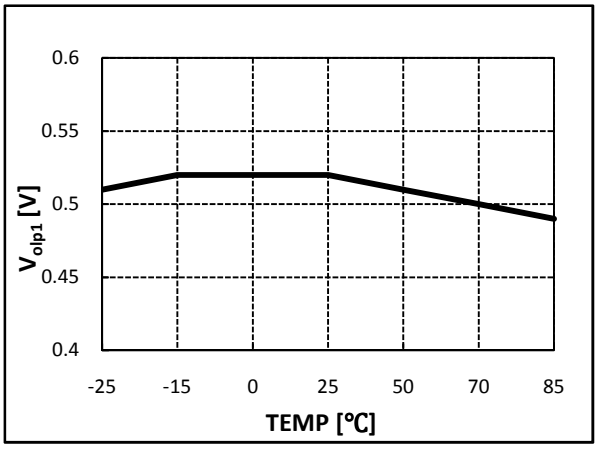

Figure 19. Open-Lamp Protection Voltage 1 vs. Temperature

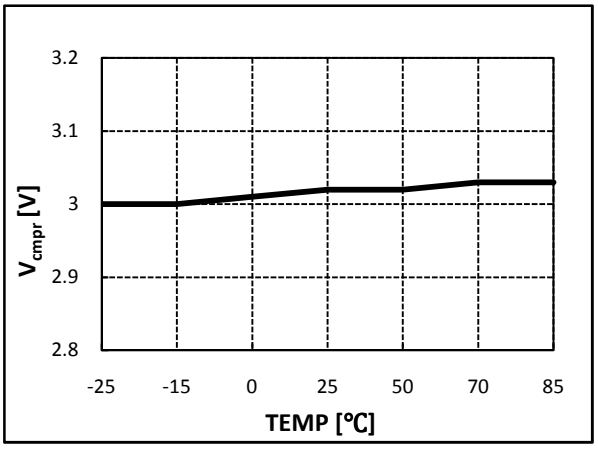

Figure 20. High-CMP Protection Voltage vs. Temperature

Typical Performance Characteristics (Continued)

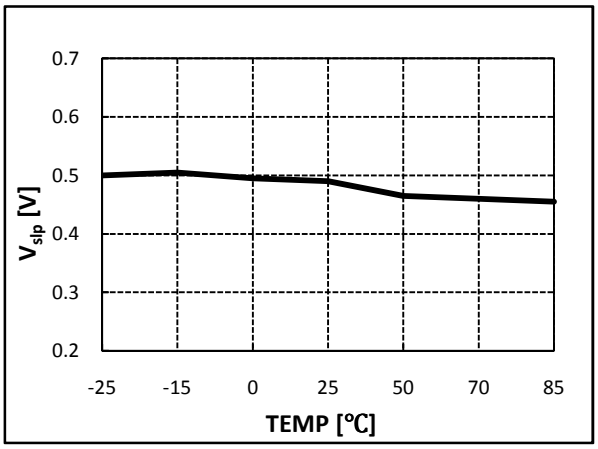

Figure 21. Short-Lamp Protection Voltage vs. Temperature

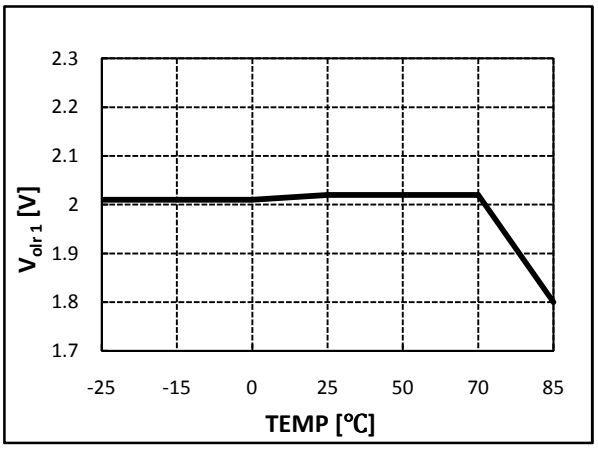

Figure 22. Open-Lamp Regulation Voltage 1 vs. Temperature

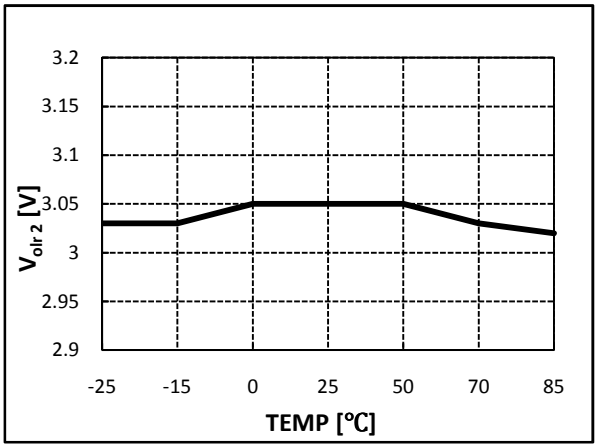

Figure 23. Open-Lamp Regulation Voltage 2 vs. Temperature

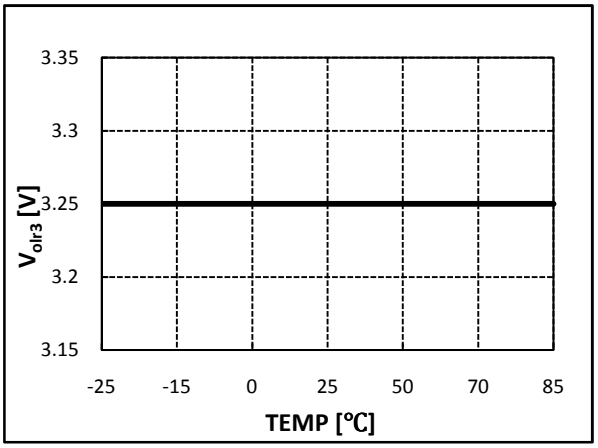

Figure 24. Open-Lamp Regulation Voltage 3 vs. Temperature

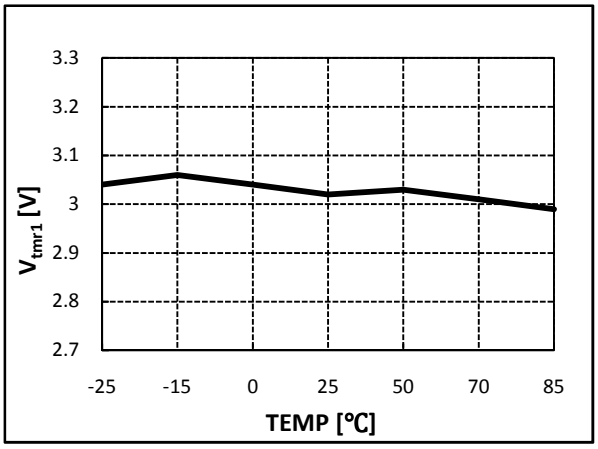

Figure 25. TIMER Threshold Voltage 1 vs. Temperature

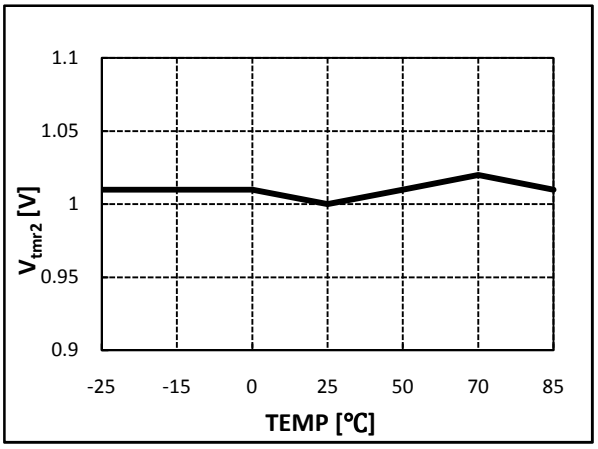

Figure 26. TIMER Threshold Voltage 2 vs. Temperature

Typical Performance Characteristics (Continued)

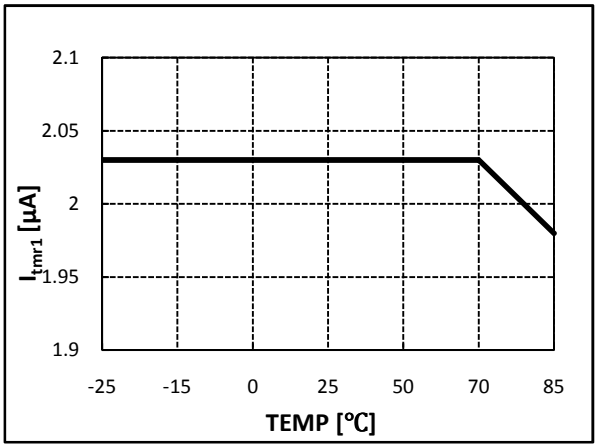

Figure 27. TIMER Current 1 vs. Temperature

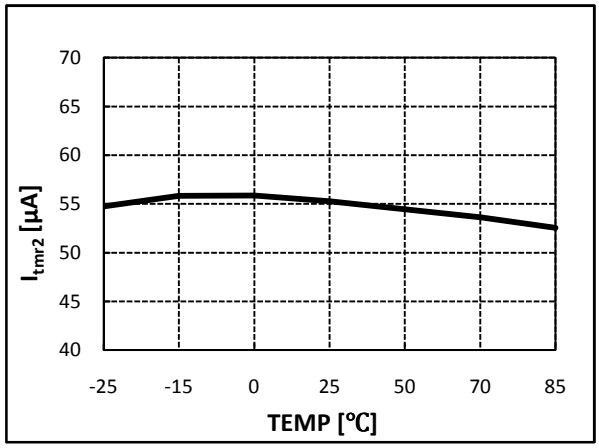

Figure 28. TIMER Current 2 vs. Temperature

Functional Description

UVLO

The under-voltage lockout (UVLO) circuit guarantees stable operation of the IC control circuit by stopping and starting it as a function of V_{IN}. The UVLO circuit turns on the control circuit when V_{IN} exceeds 9V. When V_{IN} is lower than 8V, the IC startup current is less than 120μA.

ENA

Applying voltage higher than 1.4V to the ENA pin enables the IC. If V_{ENA} is higher than 2.5V, the IC enters DCR mode. If V_{ENA} is lower than 2.1V, IC enters normal mode. Applying voltage lower than 0.7V to the ENA pin disables the IC.

Main Oscillator

The internal timing capacitors (CTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 2V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next, the timing capacitors start charging again and a new switching cycle begins. The main frequency can be programmed by adjusting the RT values. The main frequency can be calculated as:

$$f_{OSC} = \frac{500}{0.000189 \bullet RT[k\Omega] + t_{delay}}[kHz] \quad (1)$$

where t_{delay} is:

20 < RT[kΩ] < 30 : 0.00075
30 < RT[kΩ] < 40 : 0.00070
40 < RT[kΩ] < 60 : 0.00055
60 < RT[kΩ] < 70 : 0.00050

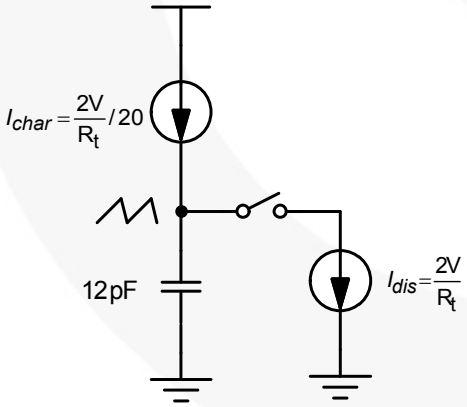

Figure 29. Main Oscillator Circuit

In striking mode, the timing resistor for striking (RT1) is connected to ground internally. The total timing resistor is the parallel connecting value of RT and RT1. The calculation of the striking frequency is similar with Equation (1). RT is only different with normal frequency. RT value for striking frequency is calculated as:

$$RT_{str} = \frac{RT \bullet RT1}{RT + RT1} \quad (2)$$

Analog Dimming

For analog dimming, reference voltage of the internal error amplifier can be controlled by the ADIM pin. Error amplifier control average voltage of OLP input voltage. The ADIM polarity of ADIM is positive.

The peak OLP voltage can be calculated as:

$$V_{OLP}^{max} = V_{ADIM} \frac{\pi}{2}[V] \quad (4)$$

The lamp intensity is proportional to V_{ADIM}. As V_{ADIM} increases, the lamp intensity increases; but ADIM voltage is clamped by 1.5V internally. Even if ADIM voltage is higher than 1.5V, internal error amplifier reference is set to 1.5V. Figure 30 shows an example of the relationship between ADIM voltage and output current.

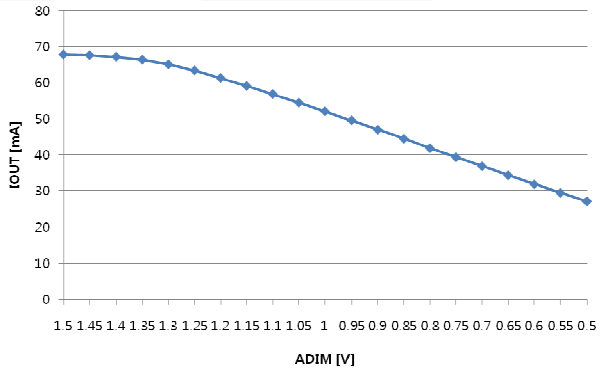

Figure 30. ADIM Voltage vs. Output Current

Figure 31 shows the lamp current waveform vs. V_{ADIM} in analog dimming mode.

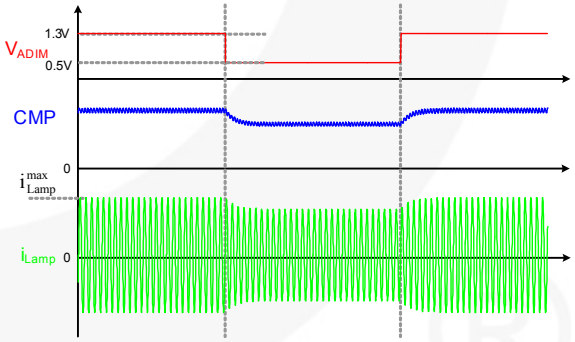

Figure 31. Analog Dimming Waveforms

Burst-Dimming

Lamp intensity is controlled with the BDIM signal over a wide range. When BDIM voltage is higher than 2V, the lamp current is turned on. When BDIM voltage is lower than 0.8V, the lamp current is turned off. The duty cycle of the PWM pulse determines the lamp brightness. The lamp intensity is proportional to BDIM pulse on duty; as BDIM on duty increases, the lamp intensity increases. Figure 32 shows the lamp current waveform vs. V_{BDIM}.

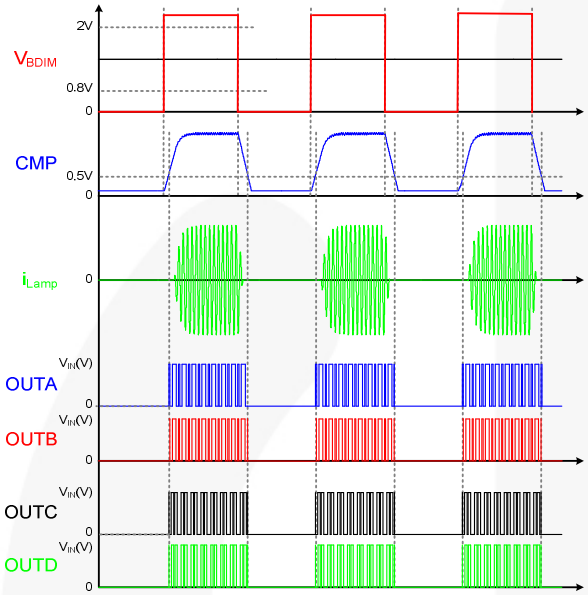

Figure 32. Burst-Dimming Waveforms

During striking mode, burst-dimming operation is disabled to guarantee continuous striking time. Figure 33 shows burst-dimming is disabled during striking mode.

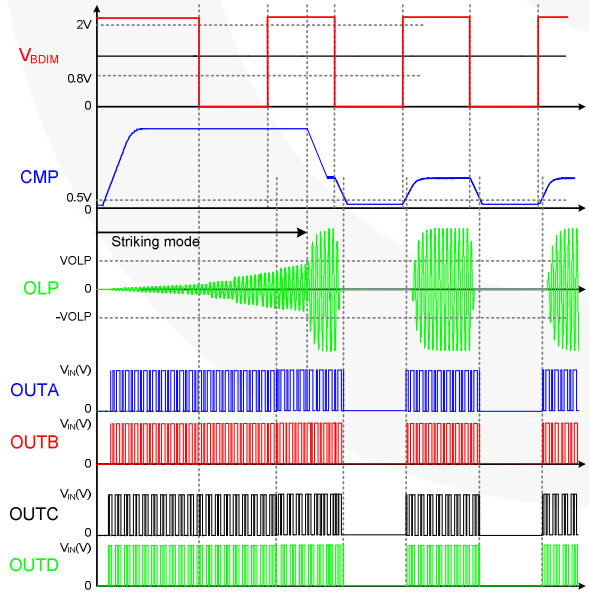

Figure 33. Burst-Dimming During Striking Mode

Output Drives

FAN7319 can drive topologies for half-bridge and full-bridge in Super-IP applications. If the MODE pin is connected to reference voltage, output drive is a push-pull topology. In Super-IP applications, push-pull topology can drive a half-bridge resonant circuit. If the MODE pin is connected to ground, output drive is a full-bridge topology. FAN7319 uses a phase-shift method for full-bridge Cold Cathode Fluorescent Lighting (CCFL) drive. As a result, the temperature difference between the left and right leg is almost zero because ZVS occurs in both of the legs by turns. The detail timing is shown in Figure 34 and Figure 35.

FAN7319 drive voltage is same as V_{IN} supply voltage, so it can drive a pulse transformer without any additional buffer. To prevent over-current in output drive, add a series resistor between the OUT pin and the pulse-transformer (22~47Ω series resistor is enough).

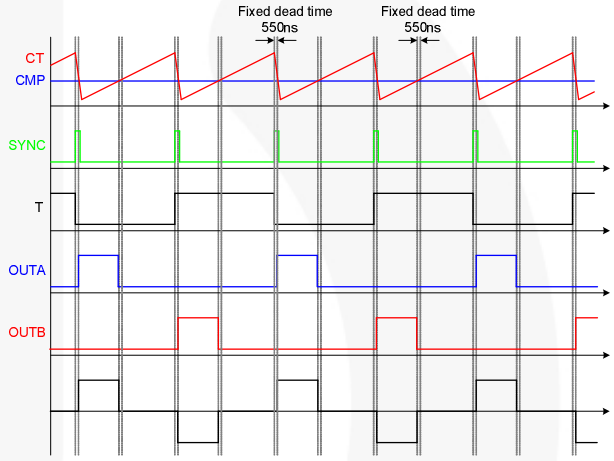

Figure 34. Push-Pull Mode Gate Drive Signal

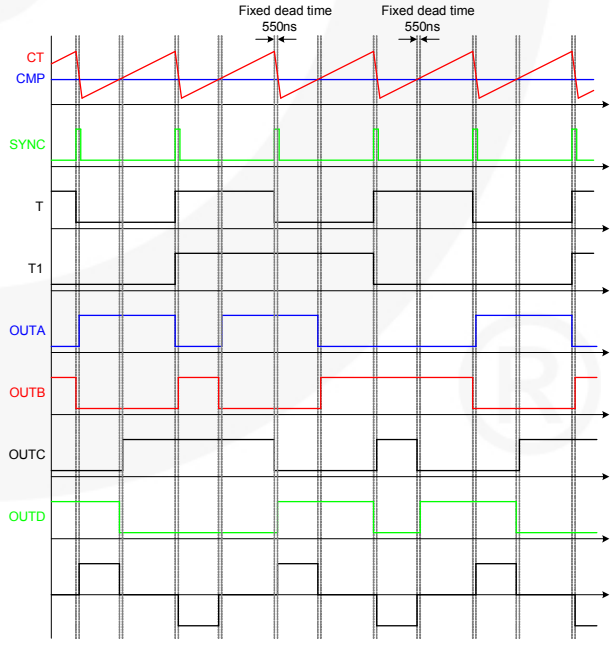

Figure 35. Full-Bridge Mode Gate Drive Signal

Synchronous Drives

FAN7319 can be operated as zero current switching (ZCS) or zero voltage switching (ZVS) mode using the SENSE pin. Internal CT voltage is forced to discharge when the SENSE pin voltage crosses the zero point. If AC signal is applied to the SENSE pin, operating frequency is synchronous with a frequency of input signal. Figure 36 shows the synchronous operation in push-pull topology.

During striking mode, the operating frequency is set to fixed frequency by a resistor, regardless of the SENSE pin zero crossing point.

The SENSE pin zero crossing frequency is faster than set frequency. If zero crossing frequency is slower than set frequency, frequency is abnormal due to irregular discharging of CT voltage.

If SENSE zero crossing frequency is much faster than set frequency, CT discharging voltage could be lower than 1.5V. In this case, CT discharging voltage is held to 1.5V to prevent synchronous frequency being too high.

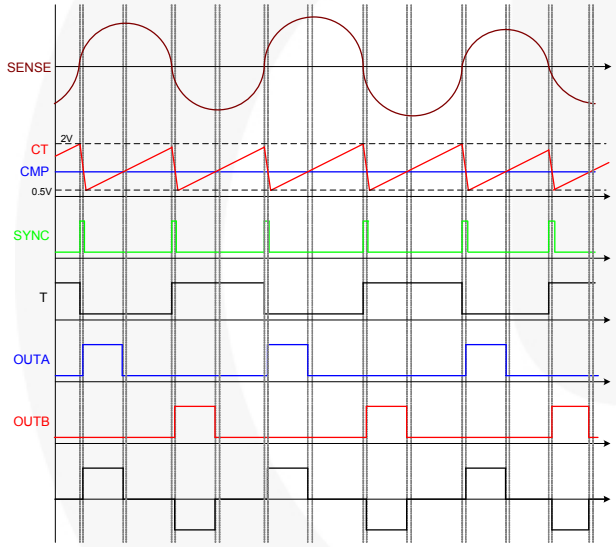

Figure 36. Synchronous Operation in Push-Pull Mode

Protections

The FAN7319 provides the following latch-mode protections: Open-Lamp Regulation (OLR), Open-Lamp Protection (OLP), Short-Lamp Protection (SLP), CMP-HIGH Protection, and Thermal Shutdown (TSD). The latch is reset when V_{IN} falls to the UVLO voltage or ENA is pulled down to GND.

Protection timing can be calculated based on Figure 37.

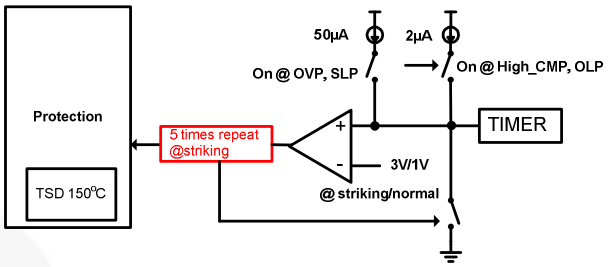

Figure 37. Timer Charging Circuit

Assume that timer capacitor is 1μF.

Striking time is one-time charging from zero to 3V and four-times charging from 0.3V to 3V with 2μA current source. The striking time is calculated as follows:

$$t_{strike} = \frac{C\Delta V_{str}}{I_{sur1}} = \frac{1\mu F \bullet 3V}{2\mu F} + 4 \bullet \frac{1\mu F \bullet 2.7V}{2\mu F} = 6.9s \quad (6)$$

The OVP and SLP delay times are calculated as:

$$t_{OVP\_SLP} = \frac{C\Delta V_{nor}}{I_{sur2}} = \frac{1\mu F \bullet 1V}{50\mu F} = 20ms \quad (7)$$

The CMP-HIGH protection and OLP delay times are calculated as:

$$t_{OLP\_CMPH} = \frac{C\Delta V_{nor}}{I_{sur1}} = \frac{1\mu F \bullet 1V}{2\mu F} = 500ms \quad (8)$$

Open-Lamp Regulation

When the maximum of the rectified OLR input voltages V_{OLR}^{max} is more than 3V, the IC enters regulation mode and controls the CMP voltage. The IC limits the lamp voltage by decreasing the CMP source current. If V_{OLR}^{max} is between 2V and 3V, the CMP source current decreases from 40μA to 3μA. Then, if V_{OLR}^{max} reaches 3V, CMP source current decreases to 0μA, so CMP voltage remains constant and the lamp voltage also remains constant, as shown in Figure 38. Finally, if V_{OLR}^{max} is more than 3.25V, the error amplifier for OLR is operating and CMP sink current increases, so CMP voltage decreases and the lamp voltage maintains the determined value.

At the same time, while V_{OLR}^{max} is more than OVPR, the 50μA current source starts charging TIMER capacitor in normal mode. When TIMER voltage reaches 1V, the IC enters shutdown, as shown in Figure 40. This protection is disabled in striking mode to ignite lamps reliably.

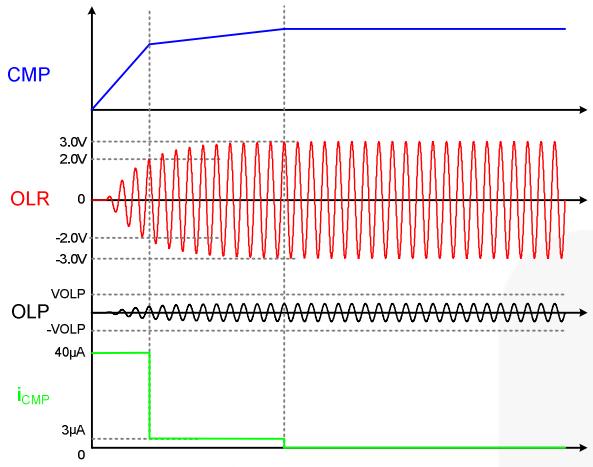

Figure 38. Open-Lamp Regulation in Striking Mode

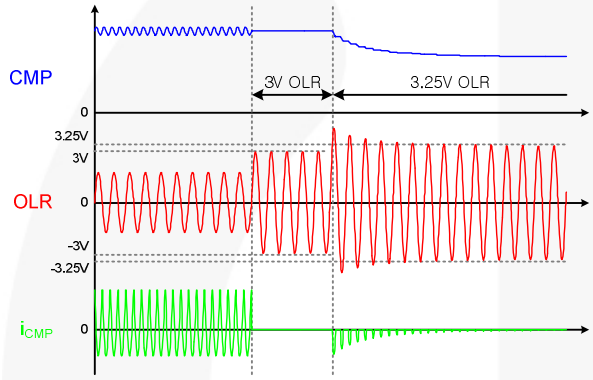

Figure 39. Open-Lamp Regulation in Normal Mode

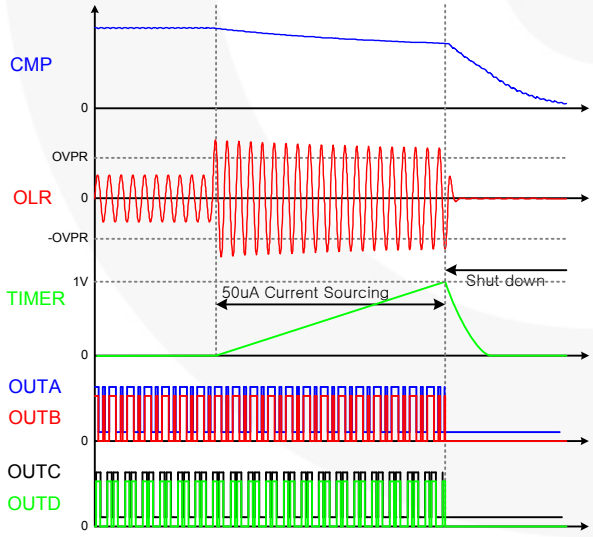

Figure 40. Over-Voltage Protection in Normal Mode

Open-Lamp Protection

If the minimum of the rectified OLP voltage $V_{\frac{min}{OLR}}$ is less than V_{OLP} during initial operation, the IC operates in striking mode only for 6.9s, as shown in Figure 41. After ignition, if $V_{\frac{min}{OLR}}$ is less than 0.5V in normal mode, the IC is shut down after a delay of 500ms, as shown in Figure 42. In DCR mode (V_{ENA}>2.5V), if $V_{\frac{min}{OLR}}$ is less than 0.5V in normal mode; the IC operates normally without shutdown, as shown in Figure 43.

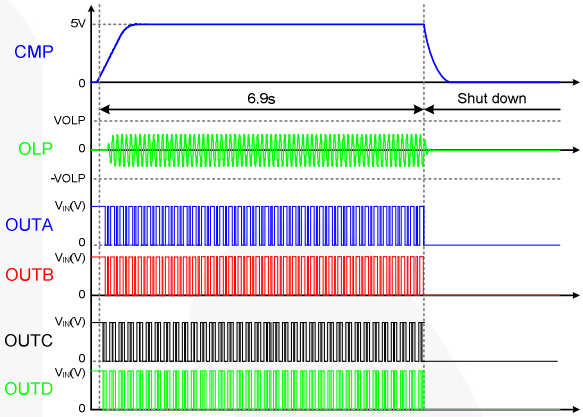

Figure 41. Open-Lamp Protection in Striking Mode

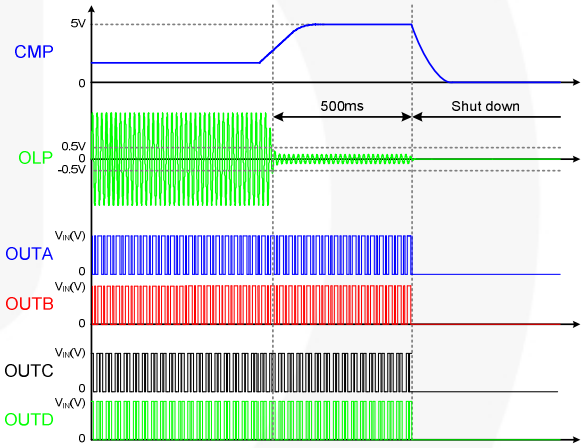

Figure 42. Open-Lamp Protection in Normal Mode

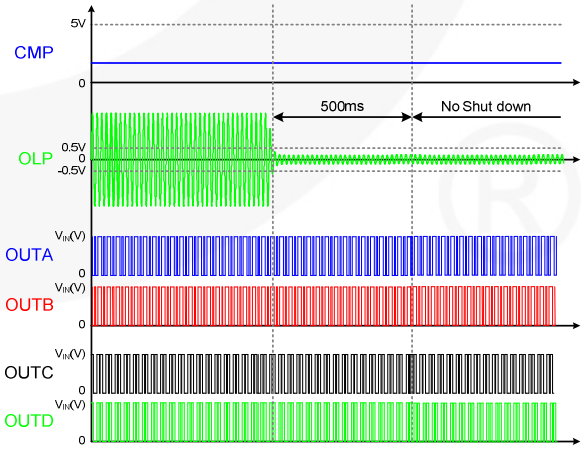

Figure 43. Open-Lamp Protection in DCR Mode

Short-Lamp Protection

If the minimum of the rectified OLR voltages (V_{OLR}^{min}) is less than 0.5V in normal mode, the IC is shut down after a delay of 20ms, as shown in Figure 44. In DCR mode (V_{ENA}>2.5V), if V_{OLR}^{min} is less than 0.5V in normal mode; the IC operates normally without shutdown, as shown in Figure 45. This protection is disabled in striking mode to ignite lamps reliably.

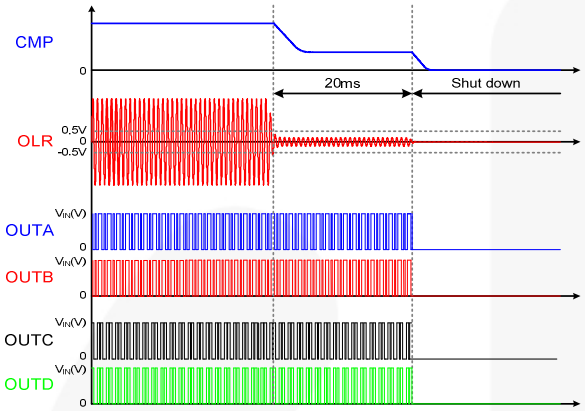

Figure 44. Short-Lamp Protection in Normal Mode

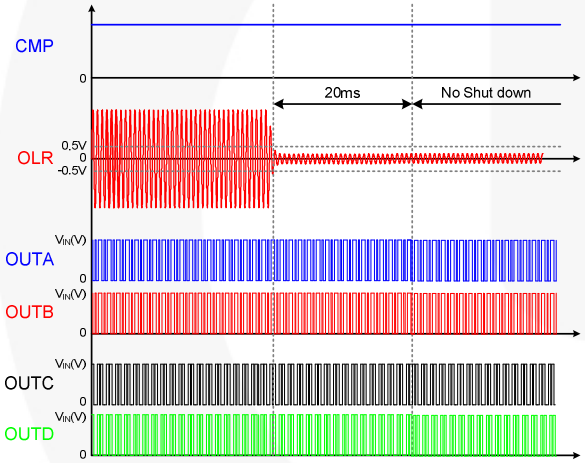

Figure 45. Short-Lamp Protection in DCR Mode

CMP-High Protection

If CMP is 2.5V in normal mode, OLP peak voltage is higher than ADIM voltage and CMP voltage is holding at 2.5V. If CMP is 2.5V in normal mode, OLP peak voltage is lower than ADIM voltage and CMP is charged by 1μA current source. If CMP is higher than 3V, the IC is shut down after a delay of 500ms, as shown in Figure 46. This protection is disabled in striking mode to ignite lamps reliably. To remove CMP-HIGH protection, connect a 1MΩ resistor to CMP capacitor in parallel. Unless 1μA sourcing current flows into the resistor, CMP voltage cannot be charged.

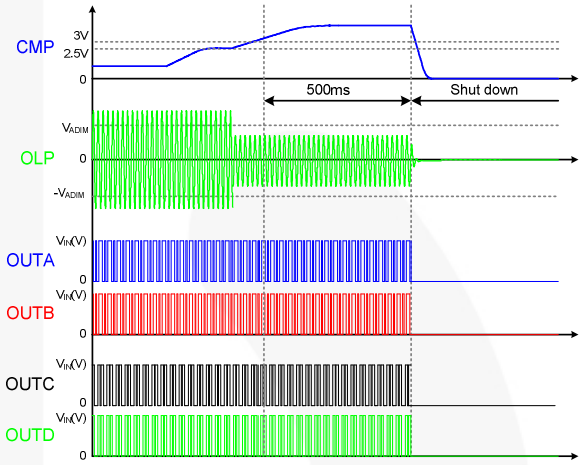

Figure 46. CMP-High Protection in Normal Mode

Thermal Shutdown

The IC provides a function to detect abnormal over-temperature. If the IC temperature exceeds approximately 150°C, the thermal shutdown triggers.

Table 1. Protection Condition Table

Mode	Category	Item	Condition	Operation	DCR Mode VENA > 2.5V	Fault Condition	Changing to Normal Frequency Condition
Striking	Regulation	OLR	$V_{OLR(MAX)}$>2V	CMP Source = 3μA		V_{TIMER}>3V, 5 Times Repeat	$V_{OLP(max)}$>V_{OLP} & $V_{OLR(max)}$<O_{VPR}
			$V_{OLR(MAX)}$>3V	CMP Source = 0μA			
			$V_{OLR(MAX)}$>3.25V	CMP Sink			
		CMP	V_{CMP}>2.5V & V_{ADIM}>$V_{OLP(MAX)}$	CMP Source = 2μA			
	Protection	OLP	$V_{OLP(MAX)}$<V_{OLP}	Timer = 2μA			
		OVP	$V_{OLR(MAX)}$>O_{VPR}	Timer = 2μA			
		SLP	Disabled		Disabled		
		CMP-HIGH	Disabled		Disabled		
Normal	Regulation	OLR	$V_{OLR(MAX)}$>3V	CMP Source = 0μA		VTIMER>1V, 1 Time	
			$V_{OLR(MAX)}$>3.25V	CMP Sink			
		CMP	V_{CMP}>2.5V & V_{ADIM}>$V_{OLP(MAX)}$	CMP Source = 2μA			
	Protection	OLP	$V_{OLP(MAX)}$<0.5V	Timer = 2μA	Disabled		
		OVP	$V_{OLR(MAX)}$>OVPR	Timer = 50μA			
		SLP	$V_{OLR(MAX)}$<0.3V	Timer = 50μA	Disabled		
		CMP-HIGH	$V_{CMP>}$3V	Timer = 2μA			

Typical Full-Bridge Application Circuit (LCD Backlight Inverter)

Application	Input Voltage Range	Number of Lamps
LCD TV (LIPS Type)	13±10%	CCFL/EEFL IP

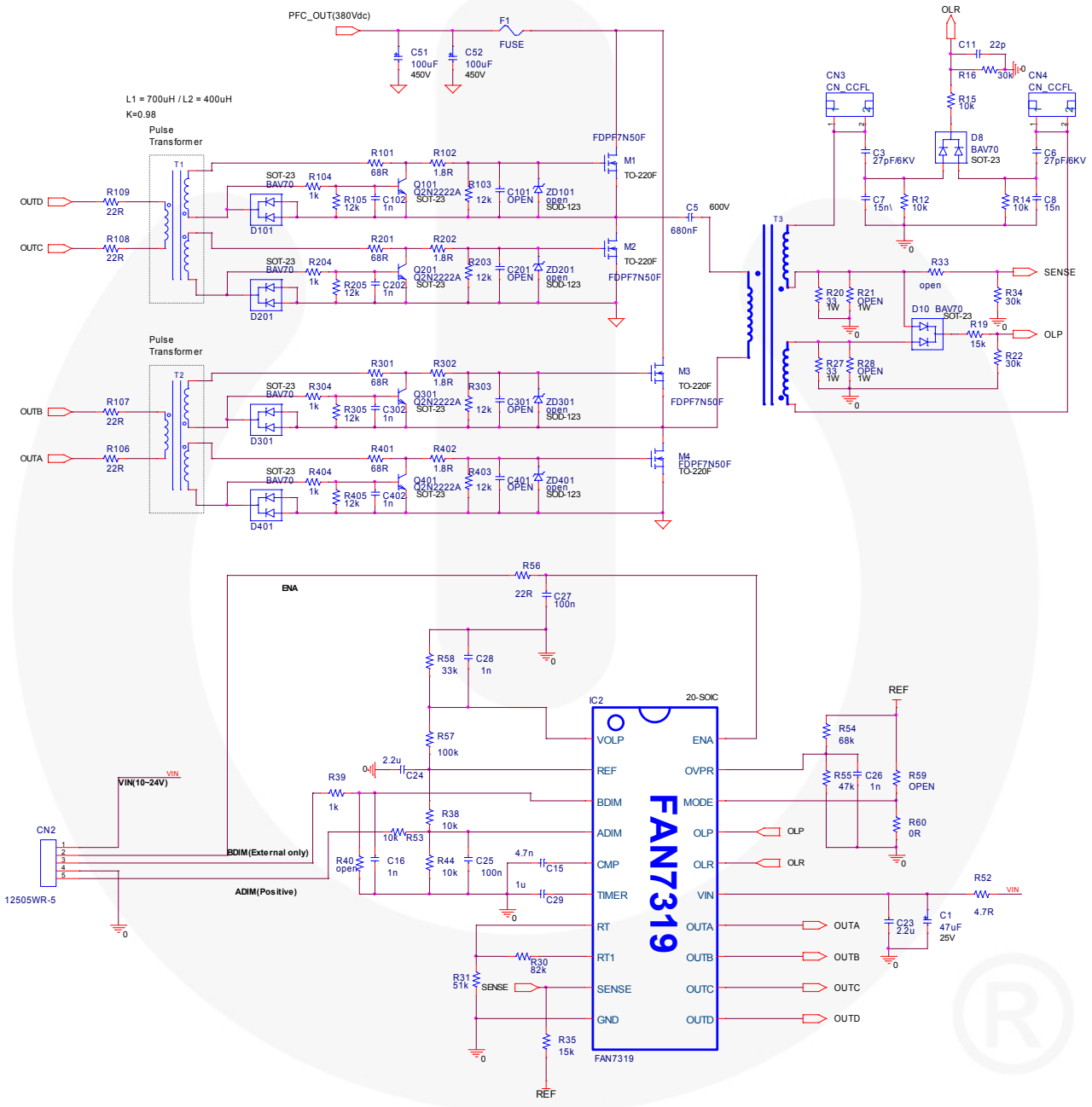

Figure 47. Typical Full-Bridge Application Circuit

Typical Half-Bridge Application Circuit (LCD Backlight Inverter)

Application	Input Voltage Range	Number of Lamps
LCD TV (LIPS Type)	13±10%	CCFL/EEFL IP

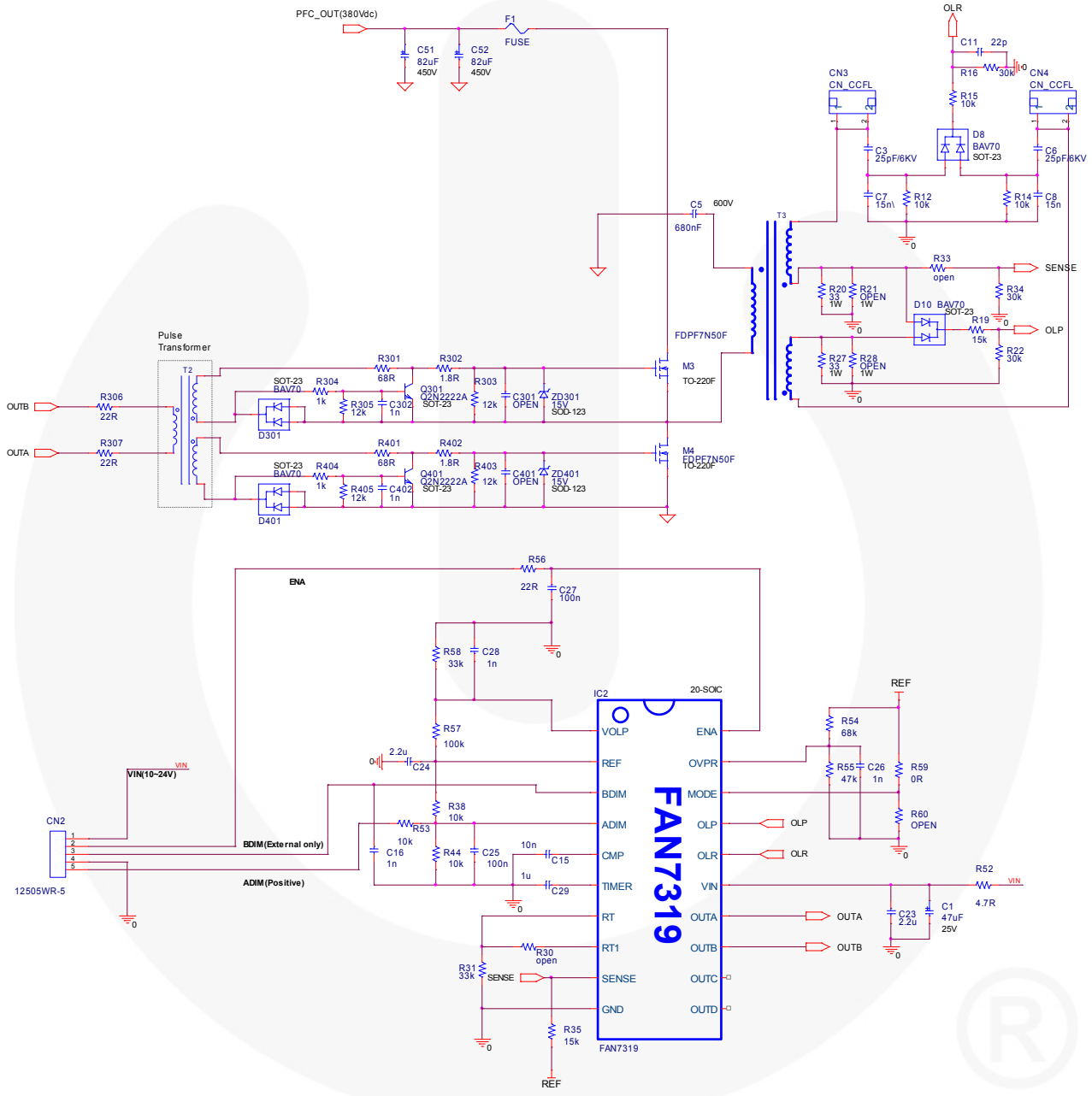

Figure 48. Typical Half-Bridge Application Circuit

Physical Dimensions

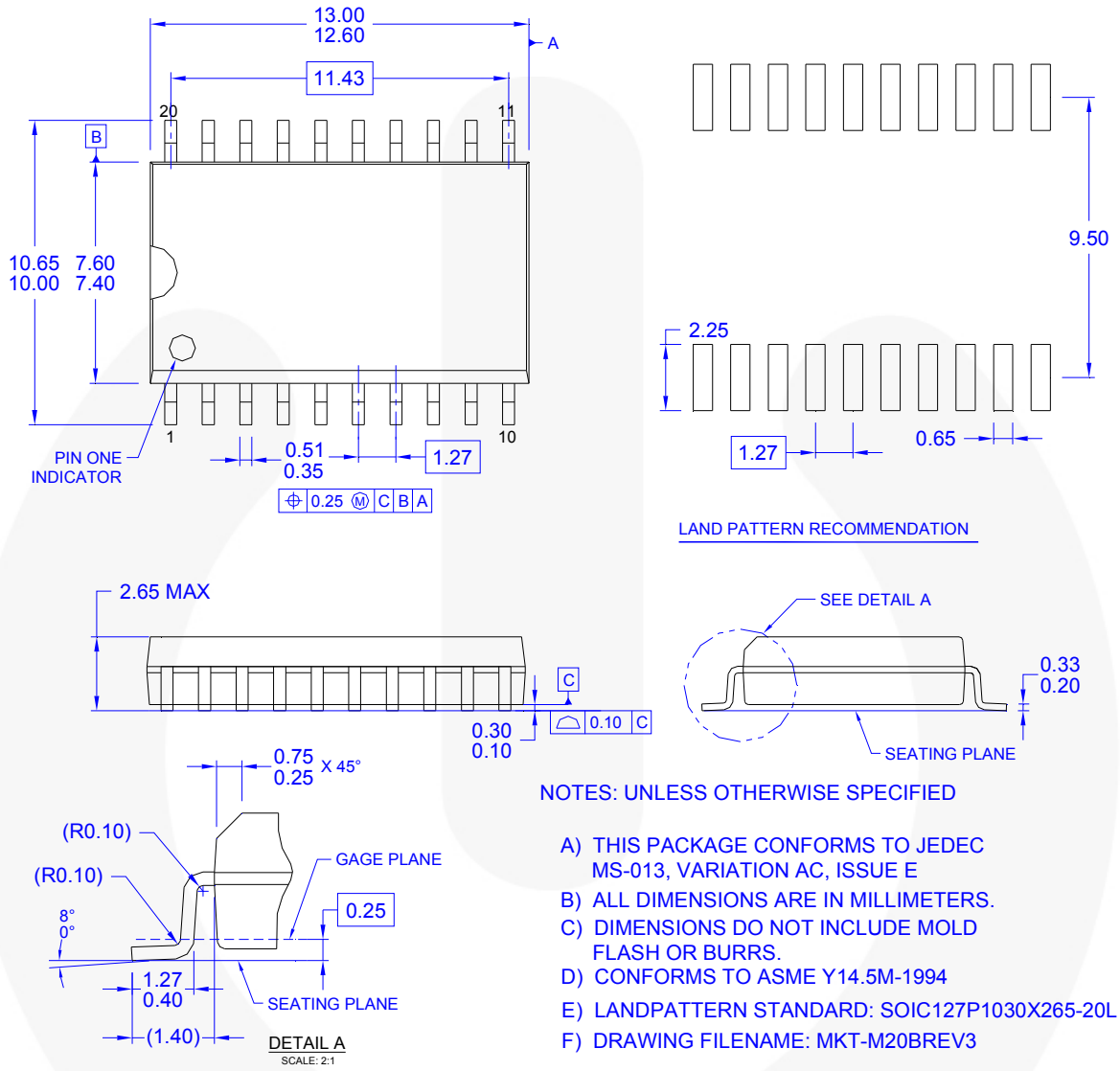

Figure 49. 20-Pin, Small-Outline Integrated Circuit (SOIC) Package

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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