AK7730A

24bit 2ch ADC+ Audio DSP

1. General Description

The AK7730A is a highly integrated audio processing IC, including a stereo 24-bit input A/D and on-chip DSP. High quality analog performance is provided by a stereo A/D with 97dB (48 kHz) dynamic range. This A/D supports sampling frequencies from 8 kHz to 96 kHz. This device includes 72kbit SRAM for delayed audio data that is suitable for simulated surround like a hall simulation. This programmable DSP part supports the sampling frequencies from 8 kHz to 192 kHz. The design allows up to 4608 execution lines per audio sample cycle at 8 kHz, 768 at 48 kHz, 192 lines at 192 kHz with multiple functions per line. The AK7730A can be used to implement complete sound field control, such as echo, 3D, parametric equalization, etc. It is packaged in a 48-lead LQFP package.

2. Features

DSP:

- **Word length:** **24-bit (Data RAM)**
- **Instruction cycle time:** **27ns (768fs, fs=48kHz)**
- **Multiplier:** **24 x 16 → 40-bit**
- **Divider:** **24 / 24 → 16-bit or 24-bit**
- **ALU:** **34-bit arithmetic operation (Overflow margin: 4bit)**
- **24-bit arithmetic and logic operation**
- **Shift+Register:** **1, 2, 3, 4, 6, 8 and 15 bits shifted left**
  1, 2, 3, 4, 8 and 15 bits shifted right
- **Other numbers in parentheses are restricted. Provided with indirect shift function**
- **Program RAM:** **768 x 32-bit**
- **Coefficient RAM:** **1024 x 16-bit**
- **Data RAM:** **256 x 24-bit**
- **Offset RAM:** **48 x 13-bit**
  (6144 x 12-bit / 3072 x 24-bit / 4096 x 12-bit + 1024 x 24-bit)
- **Internal Memory:** **72kbit SRAM**
- **Sampling frequency:** **8kHz to 192kHz**
- **Serial interface port for micro-controller**
- **Master clock:** **768fs@48kHz (generated by PLL from 256fs or 384fs)**
- **Master/Slave operation**
- **Serial signal input port (up to 8 ch):16/20/24-bit : Output port (8 ch): 24-bit**

ADC: 2 channels

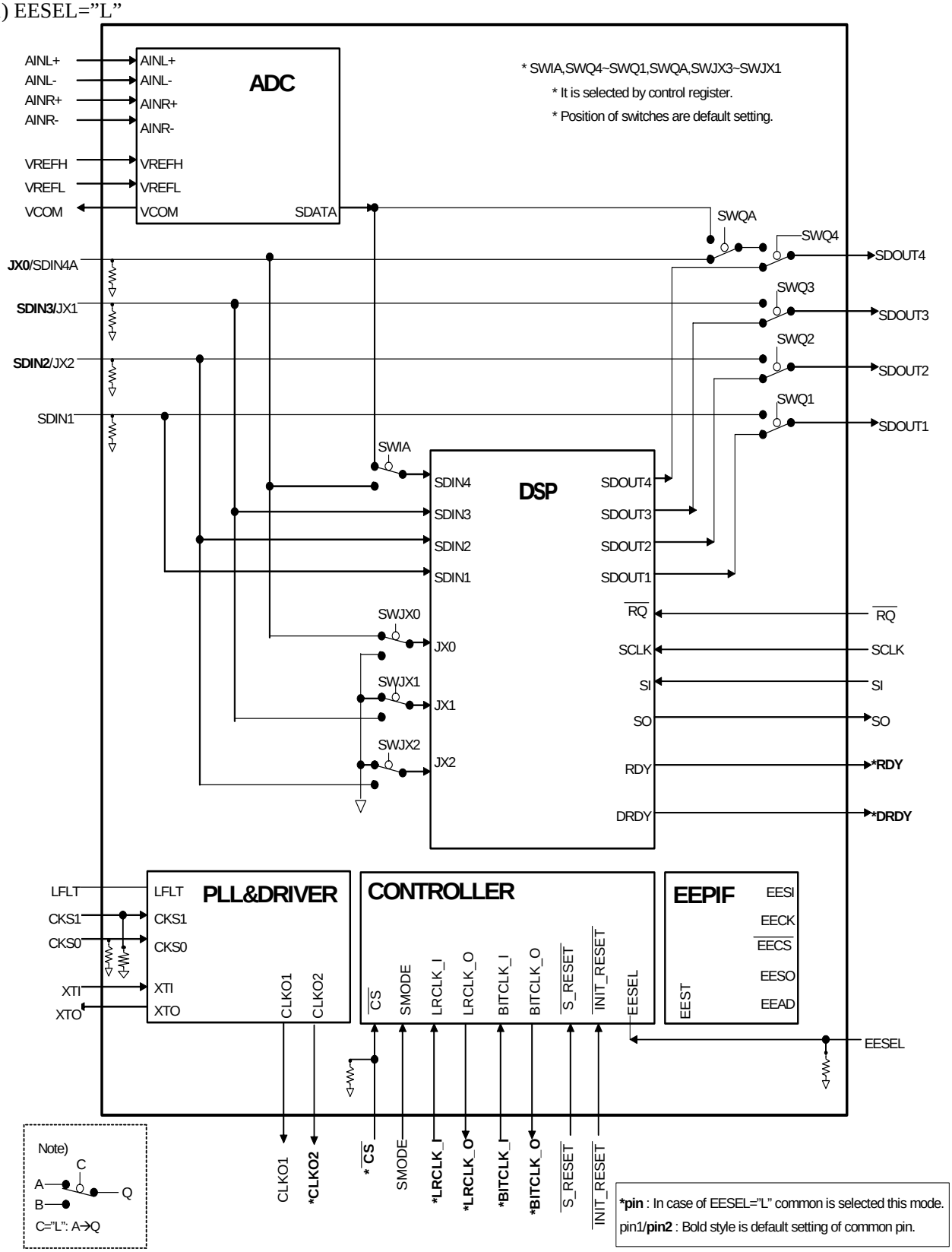
- **24-bit 64x Over-sampling delta sigma**
- **Sampling frequency:** **8kHz to 96kHz**
- **DR:** **97dBA (fs=48 kHz Full-differential Input)**
- **S/N :** **98dBA (fs=48 kHz Full-differential Input)**
- **S/(N+D) :** **92dB (fs= 48 kHz Full-differential Input)**
- **Digital HPF (fc = 1Hz)**
- **Single-ended or Full-differential Input**

Other

- **EEPROM boot**
  (Optional Selectable EEPROM boot between 2 different programs)
- **Up to 3 external Jump pins**
- **CRC error check function**
- **LRCLK and BITCLK input and output for slave mode**
- **Power supply:** **+3.3V±0.3V**
- **Operating temperature range:** **-40°C~85°C**
- **Package:** **48pin LQFP (0.5mm pitch)**

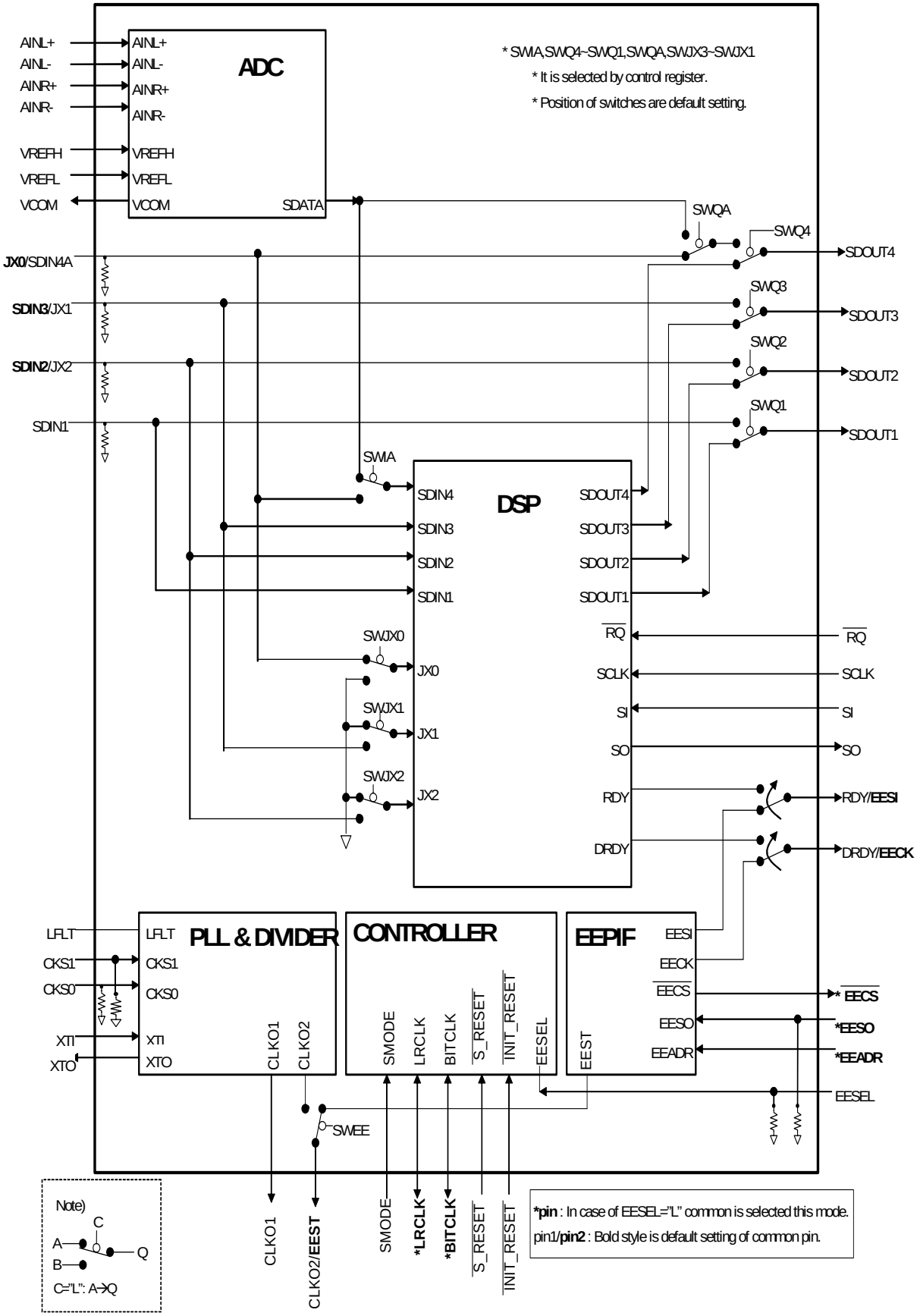
3. Block diagram

1) EESEL="L"



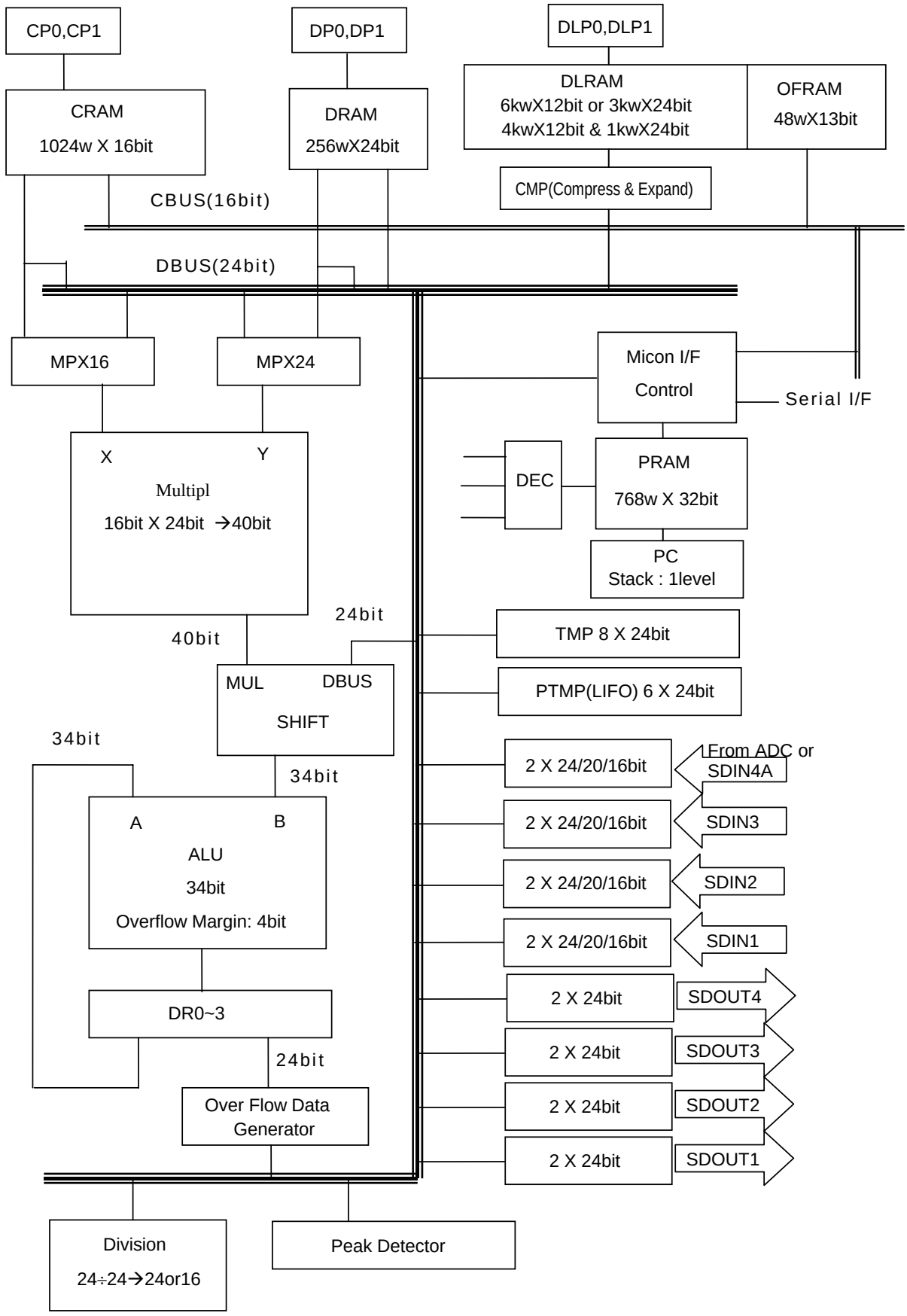
This block diagram is a simplified illustration of the AK7730A; it is not a circuit diagram.

2) EESEL="H"



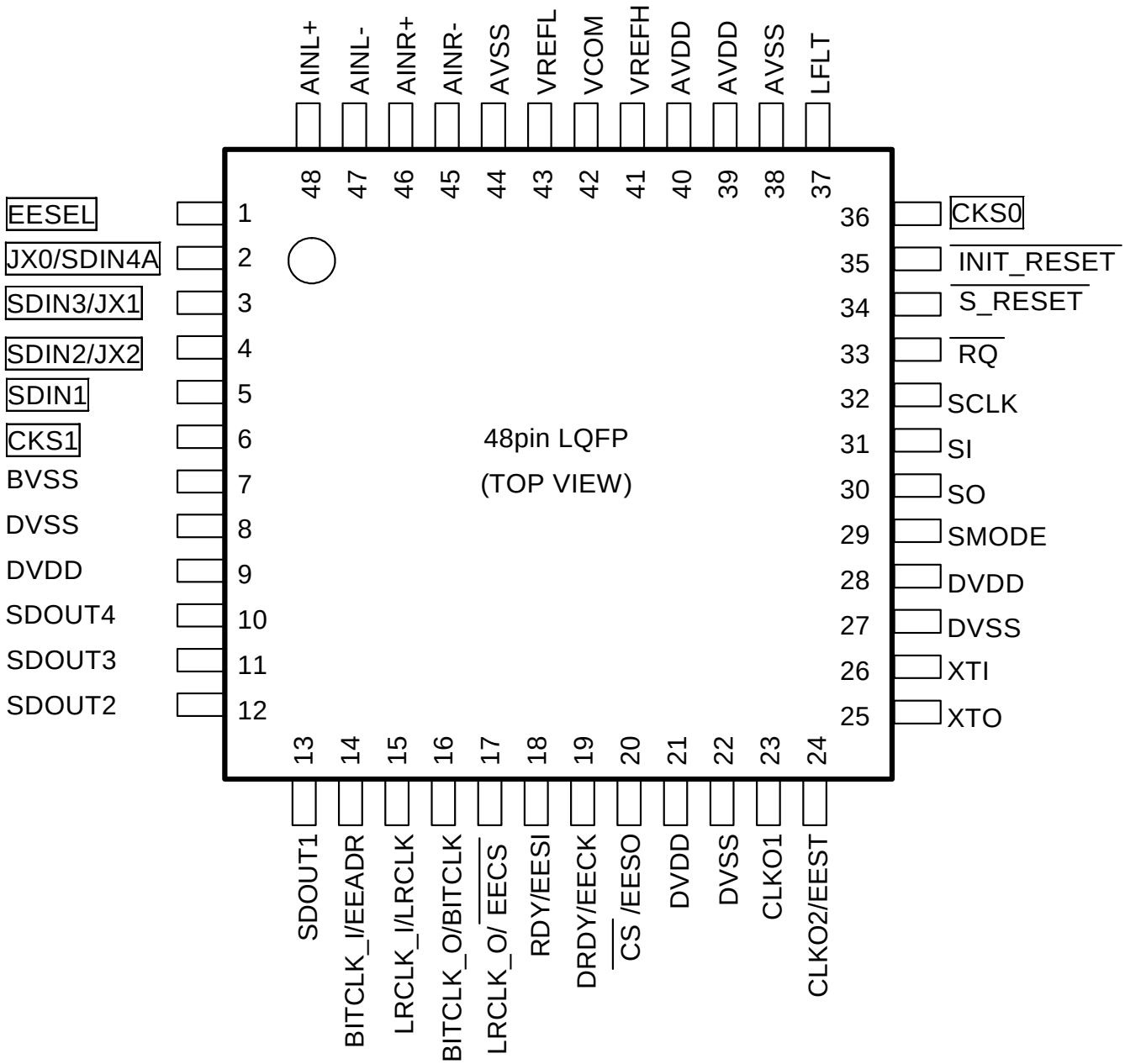
This block diagram is a simplified illustration of the AK7730A; it is not a circuit diagram.

◆ AK7730A DSP Block diagram



4. Description of Input/Output Pins

(1) Pin layout



Note) *** is internal pull-down pin.

(2) Pin function

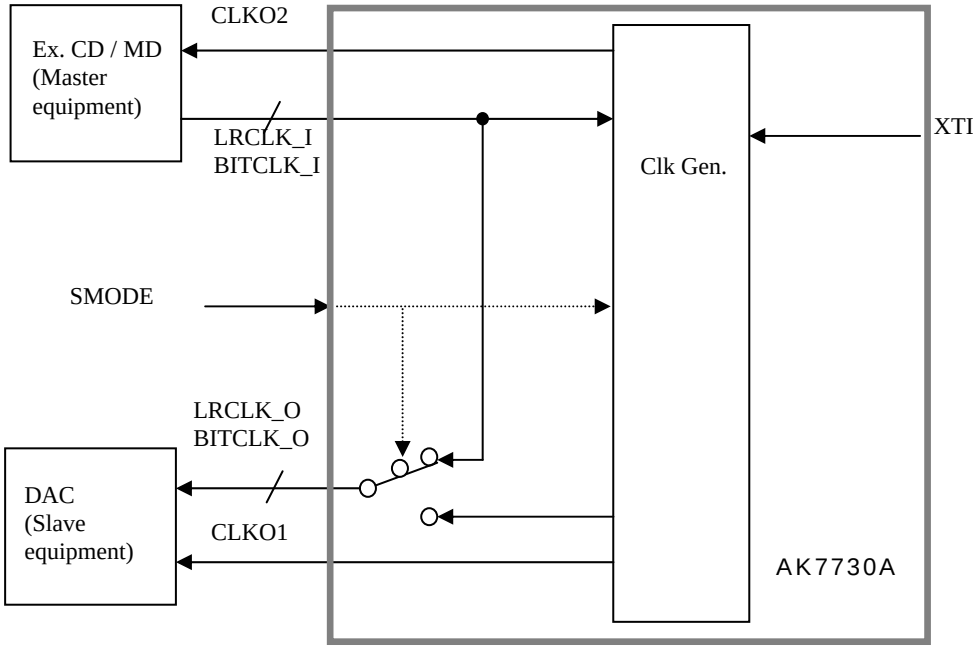
Pin No.	Pin name	I/O	Function	Classification
1	EESEL	I	**Control Mode select pin (Internal pull-down)** EESEL="L" : Normal mode EESEL="H" : In case of self-boot up mode using AKM product EEPROM AK6510C,AK6512C EESEL must be fixed "L" or "H"	Control
2	JX0/SDIN4A	I	**External conditional jump pin / DSP serial data input pin (Internal pull-down)** * Normally use as JX0 pin. * It can change its function as SDIN4 by control register setting (SWA,SWJX0) It can input as serial input port compatible with MSB justified 24 bits / LSB justified 24, 20 and 16 bits. (Normally this port is connected to ADC serial output.)	Digital section Conditional input / Serial input data
3	SDIN3/JX1	I	**DSP serial data input pin / External condition jump pin (Internal pull- down)** * Compatible with MSB justified 24 bits / LSB justified 24, 20 and 16 bits. * It can change its function as a conditional jump pin JX1 by control register setting (SWJX1).	Digital section Serial input data / Conditional input
4	SDIN2/JX2	I	**DSP serial data input pin / External condition jump pin (Internal pull-down)** * Compatible with MSB justified 24 bits / LSB justified 24, 20 and 16 bits. * It can change its function as a conditional jump pin JX2 by control register setting (SWJX2).	
5	SDIN1	I	**DSP serial data input pin (Internal pull-down)** Compatible with MSB justified 24 bits / LSB justified 24, 20 and 16 bits.	Digital section Serial input data
6	CKS1	I	**Master clock (XTI) select pin (Internal pull-down)** Normally, connect to DVSS or open.	Control
7	BVSS	-	**Silicon substrate potential 0V** Connect to AVSS.	Analog power supply
8	DVSS	-	**Ground pin for digital section 0.0V**	Digital power supply
9	DVDD	-	**Power supply pin for digital section 3.3V(typ)**	
10	SDOUT4	O	**DSP Serial data output pin** * Outputs MSB justified 24-bit data. * Allows the selectable output from ADC or SDIN4A by control register setting (SWQA,SWQ4)	Digital section Serial output data
11	SDOUT3	O	**DSP Serial data output pin** * Outputs MSB justified 24-bit data. * Allows the selectable output from SDIN3 by control register setting (SWQ3).	
12	SDOUT2	O	**DSP Serial data output pin** * Outputs MSB justified 24-bit data. * Allows the selectable output from SDIN2 by control register setting (SWQ2).	
13	SDOUT1	O	**DSP Serial data output pin** * Outputs MSB justified 24-bit data. * Allows the selectable output from SDIN1 by control register setting (SWQ1).	

Pin No	Pin name	I/O	Function	Classification
14	BITCLK_I (EESEL="L")	I	**Serial bit clock input pin** Slave mode: Input 64 fs or 48 fs clocks. When it uses only for master mode then connect to DVSS. (SMODE="H")	System clock
	EEADR (EESEL="H")	I	EEPROM address pin. AK6510C: EEADR="L". AK6512C: EEADR="L" Start address is 0000h EEADR="H" Start address is 1000h.	EEP
15	LRCLK_I (EESEL="L")	I	**LR channel select clock input pin.** Slave mode (SMODE="L") : Input the fs clock. Master mode (SMODE="H"): Connect to DVSS.	System clock
	LRCLK (EESEL="H")	I/O	**LR channel select clock pin** Slave mode (SMODE="L") : Input the fs clock. Master mode (SMODE="H") : Output the fs clock.	System clock
16	BITCLK_O (EESEL="L")	O	**Serial bit clock output pin** Master mode (SMODE="H") : Outputs 64fs clock. Slave mode (SMODE="L") : Outputs BITCLK_I clock.	System clock
	BITCLK (EESEL="H")	I/O	**Serial bit clock pin** Slave mode (SMODE="L") : Inputs 64fs or 48fs clock. Master mode (SMODE="H") : Outputs 64fs clock.	System clock
17	LRCLK_O (EESEL="L")	O	**LR channel select clock output pin** Master mode (SMODE="H") : Outputs the fs clock. Slave mode (SMODE="L") : Outputs LRCLK_I clock.	System clock
	$\overline{\text{EECS}}$ (EESEL="H")	O	**EEPROM Chip select pin** Connect with $\overline{\text{CS}}$ pin of AK6510C/12C.	EEP
18	RDY (EESEL="L")	O	**Data write ready output pin for microcomputer interface.** $\overline{\text{CS}}$ ="H" : Hi-Z	Microcomputer Interface
	RDY/EESI (EESEL="H")	O	**Data write ready output pin for microcomputer interface /** **EEPROM serial data output pin.** Connect with SI pin of AK6510C/12C. After finished data transfer from EEPROM (EEST changes from"L" to"H"), this pin automatically changes its function as RDY pin.	EEP/ Microcomputer Interface
19	DRDY (EESEL="L")	O	**Output data ready pin for Microcomputer interface.** $\overline{\text{CS}}$ ="H" : Hi-Z	Microcomputer Interface
	DRDY/EECK (EESEL="H")	O	**Output data ready pin for Microcomputer interface /** **EEPROM serial data output clock pin.** Connect to SCK pin of AK6510C/12C. When EEPROM data transfer finishes (EEST changes from"L" to"H"), this pin automatically changes function as DRDY pin.	EEP/ Microcomputer Interface

Pin No	Pin name	I/O	Function	Classification
20	$\overline{CS}$ (EESEL="L")	I	**Chip select pin for Microcomputer interface. (Internal pull-down)** $\overline{CS}$ ="H" : SI can not input, SO,RDY.DRDY = Hi-Z When EESEL="H", this function does not work.	Microcomputer interface
	EESO (EESEL="H")	I	**EEPROM serial data receive pin (Internal pull-down)** Connect to SO pin of AK6510C/12C.	EEP
21	DVDD	-	**Power supply pin for digital section 3.3V (typ)**	Power supply
22	DVSS	-	**Ground pin for digital section 0V**	
23	CLKO1	O	**Clock output pin** Output frequency can selectable by control register.	System clock
24	CLKO2 (EESEL="L")	O	**Clock output pin** Output frequency can selectable by control register.	System clock
	EEST (EESEL="H")	O	**EEPROM write status pin** The level of this pin changes from "L" to "H" when data transfer finishes from EEPROM. It indicates the interface for the microcomputer is available.	EEP
25	XTO	O	**Crystal oscillator output pin** When crystal oscillator is used, it should be connected between XTI and XTO When the external clock is used, keep this pin open.	System clock
26	XTI	I	**Master clock input pin** Connect a crystal oscillator between this pin and the XTO pin, Or input the external CMOS clock signal to XTI pin.	
27	DVSS	-	**Ground pin for digital section 0V**	Digital Power supply
28	DVDD	-	**Power supply pin for digital section 3.3V (typ)**	
29	SMODE	I	**Slave / Master mode selector pin** SMODE="L": Slave mode. SMODE="H": Master mode.	Control
30	SO	O	**Serial data output pin for Microcomputer interfaces.**	Microcomputer Interface.
31	SI	I	**Microcomputer interface serial data input and serial data output control pin.** When SI does not use, leave SI = "L".	
32	SCLK	I	**Microcomputer interface serial data clock pin.** When SCLK does not use, leave SCLK="H"	
33	$\overline{RQ}$	I	**Microcomputer interface write request pin.** $\overline{RQ}$ ="L": Microcomputer interface enable. However, when run-time data update: $\overline{RQ}$ ="H". When Microcomputer interface does not use, leave $\overline{RQ}$ ="H".	
34	$\overline{S\_RESET}$	I	**System Reset pin**	Reset
35	$\overline{INIT\_RESET}$	I	**Reset pin (for initialization)** Use initialization of the AK7730A. When changing CKS1 or CKS0 and changing XTI input frequency, this pin setting is necessary.	
36	CKS0	I	**Master clock (XTI) select pin (Internal pull-down)**	Control

Pin No	Pin name	I/O	Function	Classification
37	LFLT	-	**Filter connection pin for PLL** When use the PLL function connect with R (5.6kΩ and C (6.8nF) in series and down to the analog ground (AVSS).	Analog section
38	AVSS	-	**Analog ground 0V**	
39	AVDD	-	**Power supply pin for analog section 3.3V (typ)**	
40	AVDD	-	**Power supply pin for analog section 3.3V (typ)**	
41	VREFH	I	**Analog reference voltage input pin**. Normally, connect to AVDD, and connect 0.1μF and 10μF capacitors between this pin and AVSS.	
42	VCOM	O	**Common voltage** Normally, connect to 0.1μF capacitor between this pin and AVSS. Don't connect outside circuits.	
43	VREFL	I	**Analog reference voltage input pin for low-level.** Normally, connect to AVSS.	
44	AVSS	-	**Analog ground 0V**	
45	AINR-	I	**ADC Rch analog inverted input pin.**	
46	AINR+	I	**ADC Rch analog non-inverted input pin.**	
47	AINL-	I	**ADC Lch analog inverted input pin.**	
48	AINL+	I	**ADC Lch analog non-inverted input pin.**	

Note) Do NOT leave open digital input pin except pull-down pins and BITCLK_I, LRCLK_I on master mode.
(If you do not use pull-down pin, leave open or connects to DVSS.)



Fig,1 Connect with others

5. Absolute maximum rating

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Item	Symbol	min	max	Unit
Power supply voltage				
Analog(AVDD)	VA	-0.3	4.6	V
Digital(DVDD)	VD	-0.3	4.6	V
|AVSS(BVSS)-DVSS| Note 1)	ΔGND		0.3	V
Input current (except for power supply pin)	IIN	-	±10	mA
Analog input voltage AINL+,AINL-,AINR+,AINR-,	VINA	-0.3	VA+0.3	V
Digital input voltage	VIND	-0.3	VA+0.3	V
Operating ambient temperature	Ta	-40	85	°C
Storage temperature	Tstg	-65	150	°C

Note 1) AVSS(BVSS) should be same level as DVSS.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operations are not guaranteed under these critical conditions in principle.

6. Recommended operating conditions

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Items	Symbol	min	typ	max	Unit
Power supply voltage					
AVDD	VA	3.0	3.3	3.6	V
DVDD	VD	3.0	3.3	VA	V
Reference voltage (VREF)					
VREFH Note 1)	VRH		VA		V
VREFL Note 2)	VRL		0.0		V

Note 1) VREFH normally connects with AVDD.
Note 2) VREFL normally connects with AVSS

Note: The analog input voltage and output voltage are proportional to the VREFH-VREFL voltages.

7. Electric characteristics

(1) Analog characteristics

(Unless otherwise specified, Ta = 25°C; AVDD, DVDD = 3.3V; VREFH = AVDD, VREFL = AVSS;
BITCLK = 64 fs; Signal frequency 1 kHz;
Measuring frequency = 20 Hz to 20 kHz @48 kHz, 20 Hz~40 kHz @96kHz;
ADC with all differential inputs, CLKO output = 18.432MHz; XTI = 18.432MHz, SMODE = "H")

	Parameter	min	typ	max	Unit
ADC Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (-1dBFS) (Note1)	82	92		dB
	fs = 96kHz (-1dBFS)		88		dB
	Dynamic range fs = 48kHz (A filter) (Note2)	90	97		dB
	fs = 96kHz		93		dB
	S/N fs = 48kHz (A filter)	90	98		dB
	fs = 98kHz		93		dB
	Inter-channel isolation (f=1kHz)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching		0.1	0.3	dB
	Gain drift		50		ppm/°C
	Analog input				
	Input voltage (Note3)	±1.22	±1.32	±1.42	Vp-p
	Input impedance (fs=48kHz) (Note 4)		95		kΩ

Note 1) In case of using single-ended input, this value is not guarantee.
Note 2) Indicates S/(N+D) when -60 dBFS signal is applied.
Note 3) The full-scale (ΔAIN = (AIN+) - (AIN-)) can be represented by (±FS = ± (VREFH-VREFL) ×0.4).

(2) DC characteristics

(VDD=AVDD=DVDD=3.0~3.6V, Ta=25°C)

Parameter	Symbol	min	typ	max	Unit
High level input voltage	VIH	80%VDD			V
Low level input voltage	VIL			20%VDD	V
High level output voltage Iout=-100μA	VOH	VDD-0.5			V
Low level output voltage Iout=100μA	VOL			0.5	V
Input leak current Note 1)	Iin			±10	μA
Input leak current (pull-down) Note 2)	Iid		30		μA
Input leak current (XTI pin)	Iix		50		μA

Note 1) The pull-down pins and XTI pin are not included.
Note 2) The pull-down pins are 1, 2,3,4,5,6,20 and 36 pin.

Note:

Regarding the input/output levels in the text, the low level will be represented as "L" or 0, and the high level as "H" or 1. In principle, "0" and "1" will be used to represent the bus (serial/parallel) such as registers.

(3) Current consumption

(AVDD=DVDD=3.0V~3.6V, Ta=25°C; master clock (XTI)=18.432MHz=384fs[fs=48kHz];
PLL is in active mode.)

Power supply				
Parameter	min	typ	max	Unit
Power supply current Note 1)				
1)Normal Speed				
a) AVDD		15		mA
b) DVDD		50		mA
c) total(a+b)		65		mA
2)Double Speed				
a) AVDD		16		mA
b) DVDD		55		mA
c) total(a+b)		71		mA
3)Quadruple Speed				
a) AVDD		4		mA
b) DVDD		55		mA
c) total(a+b)		59		mA
4) 1)2)3) max Note 2)				
a) AVDD			23	mA
b) DVDD			77	mA
c) total(a+b)			100	mA
5) $\overline{\text{INIT\_RESET}}$ ="L" (reference) Note 3)		4		mA
Power consumption				
1)Normal Speed				
a) AVDD		50		mW
b) DVDD		165		mW
c) total(a+b)		215		mW
2)Double Speed				
a) AVDD		53		mW
b) DVDD		182		mW
c) total(a+b)		235		mW
3)Quadruple Speed				
a) AVDD		13		mW
b) DVDD		182		mW
c) total(a+b)		195		mW
4) 1)2)3) max Note 2)				
a) AVDD			83	mW
b) DVDD			277	mW
c) total(a+b)			360	mW
5) $\overline{\text{INIT\_RESET}}$ ="L" (reference) Note 3)		13		mW

Note 1) Varies slightly different according to the system frequency and contents of the DSP program.

Note 2) Max value is “Double Speed” mode.

Note 3) This is a reference value in case of using the crystal oscillator. Because most of the power current at the initial reset state is the oscillator section, the value may vary slightly according to the types of crystal oscillators and external circuits. This is “reference value” only.

(4) Digital filter characteristics

Values described below are design values cited as references.

1) ADC Section:

(Ta=25°C; AVDD, DVDD =3.0V~3.6V; fs=48 kHz; HPF=off Note1))

parameter	Symbol	min	typ	max	Unit
Pass band±0.005dB Note 2)	PB	0		21.5	kHz
(-0.02dB)		-	21.768	-	kHz
(-6.0dB)		-	24.00	-	kHz
Stop band	SB	26.5			kHz
Pass band ripple Note 2)	PR			±0.005	dB
Stop band attenuation Note3,4)	SA	80			dB
Group delay distortion	ΔGD			0	us
Group delay (Ts=1/fs)	GD		29.3		Ts

Note 1) HPF response is not including.
Note 2) The pass band is from DC to 21.5 kHz when fs = 48 kHz.
Note 3) The stop band is from 26.5 kHz to 3.0455MHz when fs = 48 kHz.
Note 4) When fs = 48 kHz, the analog modulator samples analog input at 3.072MHz. The input signal is not attenuated by the digital filter in the multiple bands (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3...) of the sampling frequency.

(5) Switching characteristics

5-1) System clock

(AVDD=DVDD=3.0V~3.6V,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Master clock (XTI)					
a) With a crystal oscillator: Note.1)					
CKS[1:0]=0h	fMCLK	-	16.9344 18.432	-	MHz
CKS[1:0]=1h	fMCLK	-	11.2896 12.288	-	MHz
CKS[1:0]=2h	fMCLK	-	22.5792 24.576	-	MHz
b) With an external clock: Note. 1)					
Duty factor (≤18.5MHz) (>18.5MHz)		40 45	50 50	60 55	% %
CKS[1:0]=0h	fMCLK	16.0		18.6	MHz
CKS[1:0]=1h	fMCLK	11.0		12.4	MHz
CKS[1:0]=2h	fMCLK	22.0		24.8	
CKS[1:0]=3h	fMCLK	24.0		37.0	MHz
Clock rise time Clock fall time	tCR tCF			6 6	ns ns
LRCLK Sampling frequency	fs	8	48	192	kHz
Slave mode :clock rise time Slave mode :clock fall time	tLR tLF			6 6	ns ns
BITCLK Note 2)	fBCLK	48	64		fs
Slave mode: High level width Slave mode: Low level width	tBCLKH tBCLKL	36 36			ns ns
Slave mode :clock rise time Slave mode :clock fall time	tBR tBF			6 6	ns ns

Note 1) Only CKS[1:0]=3h is not use PLL.

Note 2) 48fs mode can be use only at slave mode.

5-2) Reset

(AVDD=DVDD=3.0V~3.6V,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
$\overline{\text{INIT\_RESET}}$ Note 1)	tRST	400			ns
$\overline{\text{S\_RESET}}$	tRST	400			ns

Note 1) "L" is acceptable when power is turned on, but "H" needs stable master clock input.

5-3) Audio interface

(AVDD=DVDD=3.0~3.6V,Ta=-40°C ~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BITCLK frequency	fBCLK	48	64		fs
BITCLK low level width	tBCLKL	36			ns
BITCLK high level width	tBCLKH	36			ns
Delay time from BITCLK"↑" to LRCLK	tBLRD	20			ns
Delay time from LRCLK to BITCLK "↑"	tLRBD	20			ns
Delay time from LRCLK to serial data output	tLRD			25	ns
Delay time from BITCLK to serial data output	tBSOD			25	ns
Serial data input latch hold time	tBSIDS	25			ns
Serial data input latch setup time	tBSIDH	25			ns
Master mode					
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		%
Delay time from BITCLK"↑" to LRCLK Note 1)	tBLRD	20			ns
Delay time from LRCLK to BITCLK"↑" Note 1)	tLRBD	20			ns
Delay time from LRCLK to serial data output	tLRD			25	ns
Delay time from BITCLK to serial data output	tBSOD			25	ns
Serial data input latch hold time	tBSIDS	25			ns
Serial data input latch setup time	tBSIDH	25			ns

Note 1) This feature is to avoid LRCLK edge and BITCLK "↑"edge.

5-4) Microcomputer interface

(AVDD=DVDD=3.0V~3.6V, Ta=-40~85°C, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcomputer interface signal					
$\overline{RQ}$ Fall time	tWRF			8	ns
$\overline{RQ}$ Rise time	tWRR			8	ns
SCLK fall time	tSF			8	ns
SCLKrise time	tSR			8	ns
SCLK low level width	tSCLKL	50			ns
SCLK high level width	tSCLKH	50			ns
Microcomputer to AK7730A					
Time from $\overline{RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	200			ns
Time from $\overline{RQ}$ "↑" to $\overline{RESET}$ "↑" Note 1)	tWRE	200			ns
$\overline{RQ}$ high level width	tWRQH	200			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	200			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	6×tMCLK			ns
SI latch setup time	tSIS	100			ns
SI latch hold time	tSIH	100			ns
AK7730A to microcomputer					
Time from SCLK"↑" to DRDY"↓"	tSDR			3×tMCLK	ns
Time from SI"↑"to DRDY"↓"	tSIDR			3×tMCLK	ns
SI high level width	tSIH	3×tMCLK			ns
Delay time from SCLK"↓" to SO output	tSOS			100	ns
Hold time from SCLK"↑" to SO output	tSOH	150			ns
AK7730A to microcomputer (RAM DATA read-out)					
SI latch setup time (SI="H")	tRSISH	30			ns
SI latch setup time (SI="L")	tRSISL	30			ns
SI latch hold time	tRSIH	30			ns
Time from SCLK"↓" to SO output	tSOD			100	ns
AK7730A to microcomputer (CRC result out) Note 2)					
Delay time from $\overline{RQ}$ "↑" to SO output	tRSOC			150	ns
Delay time from $\overline{RQ}$ "↓" to SO output Note 3)	tFSOC	50			ns
$\overline{CS}$ (EESEL="L" or open)					
$\overline{CS}$ Fall time	tCSF			8	ns
$\overline{CS}$ Rise time	tCSR			8	ns
Time from $\overline{S\_RESET}$ "↓" to $\overline{CS}$ "↓"	tWRCS	400			ns
Time from $\overline{CS}$ "↑" to $\overline{S\_RESET}$ "↑"	tWCSR	400			ns
$\overline{CS}$ high level width	tWCSH	800			ns
Time from $\overline{CS}$ "↓" to $\overline{RQ}$ "↓"	tWCSRQ	400			ns
Time from $\overline{RQ}$ "↑" to $\overline{CS}$ "↑"	tWRQCS	400			ns
$\overline{CS}$ "↓" to SO,RDY,DRDY Hi-Z release (RL=10kΩ)	tCSHR			600	ns
$\overline{CS}$ "↑" to SO,RDY,DRDY Hi-Z (RL=10kΩ)	tCSHS			600	ns
EEPROM to AK7730A(EESEL="H")					
EESO latch setup time	tEESOS	100			ns
EESO latch hold time	tEESOH	100			ns

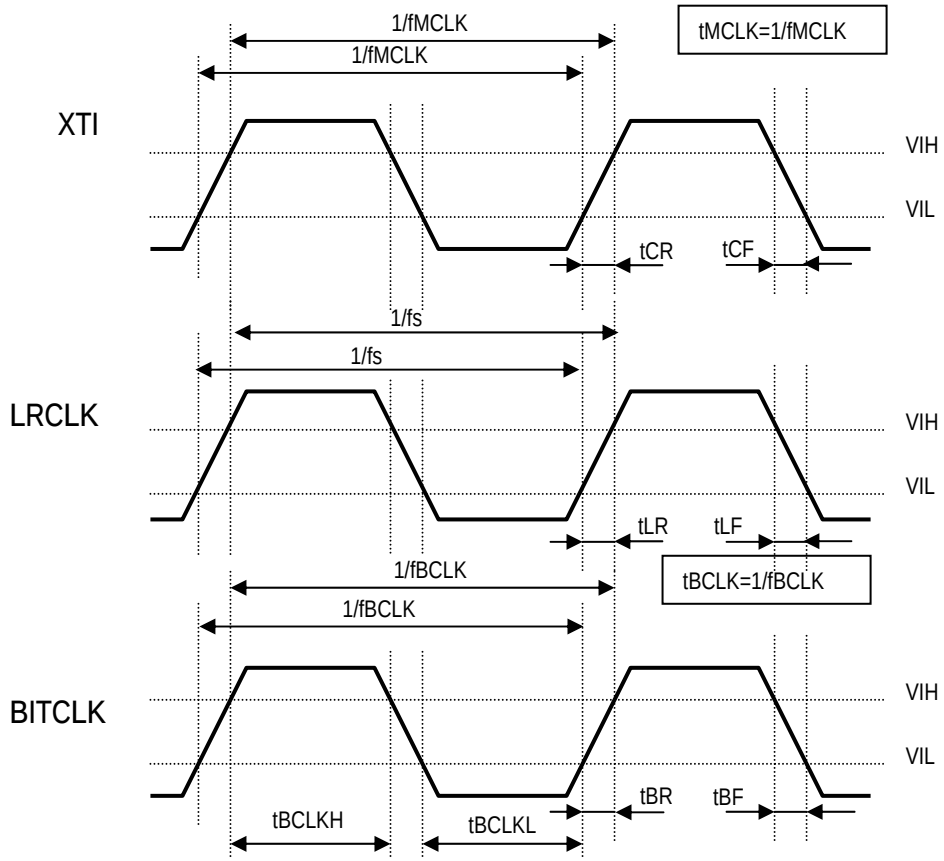
Note 1) Except for external jump code set at reset state.

Note 2) In the case of the data of the surplus of serial data D(x) divided by G(x) is equal to R(x), then SO = "H".

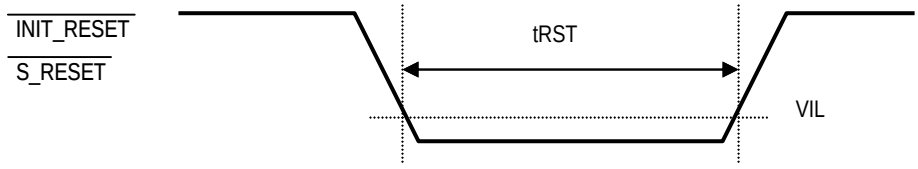
Note 3) This means that it must read more than 50ns before $\overline{RQ}$ falling .

(6) Timing waveform

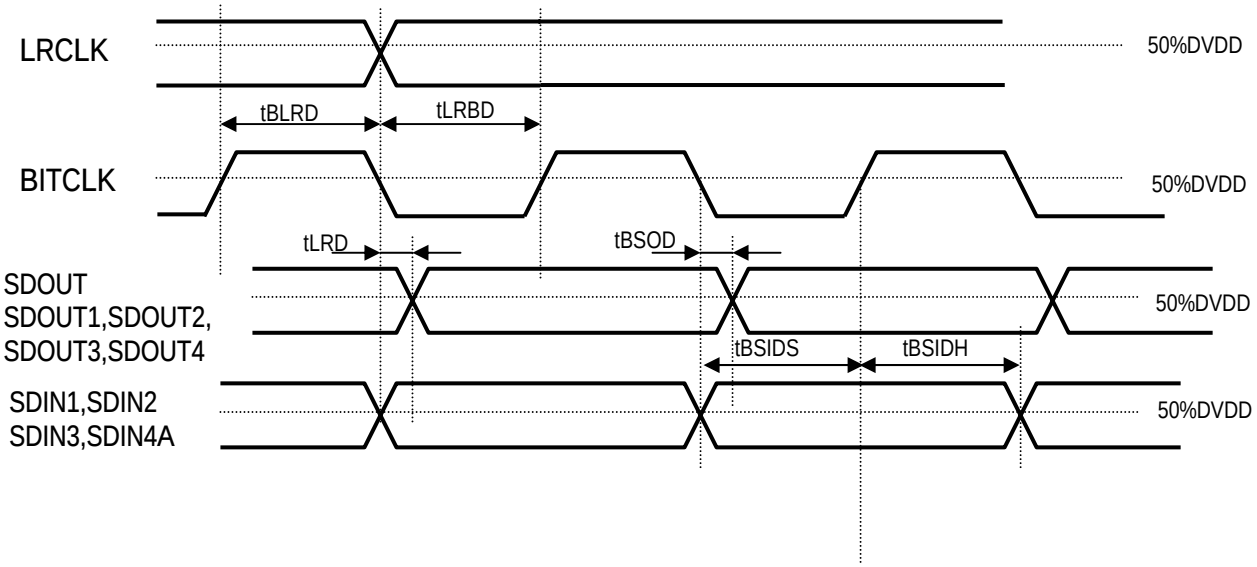
6-1) System clock



6-2) RESET

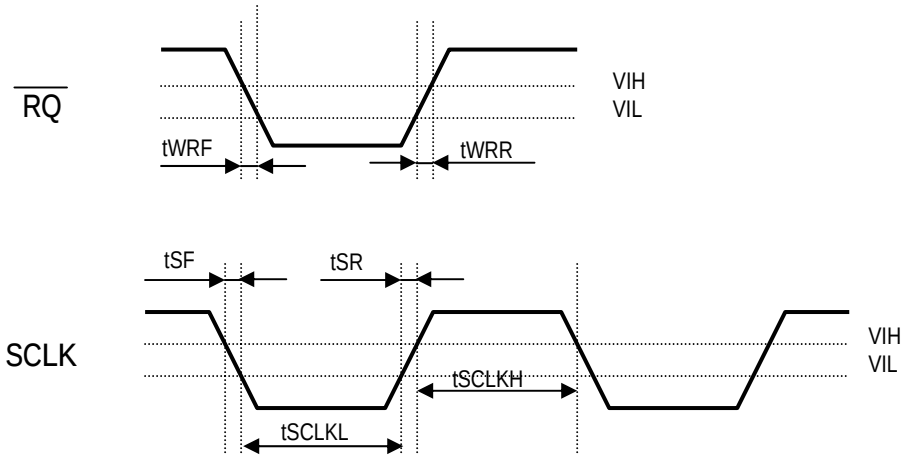


6-3) Audio interface

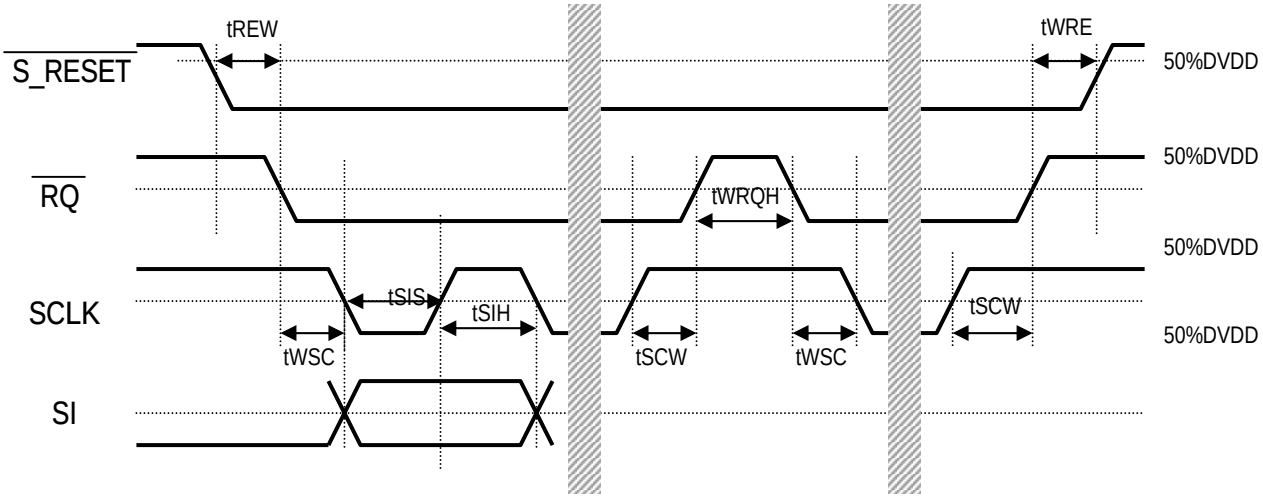


6-4) Microcomputer interface

■ Microcomputer interface



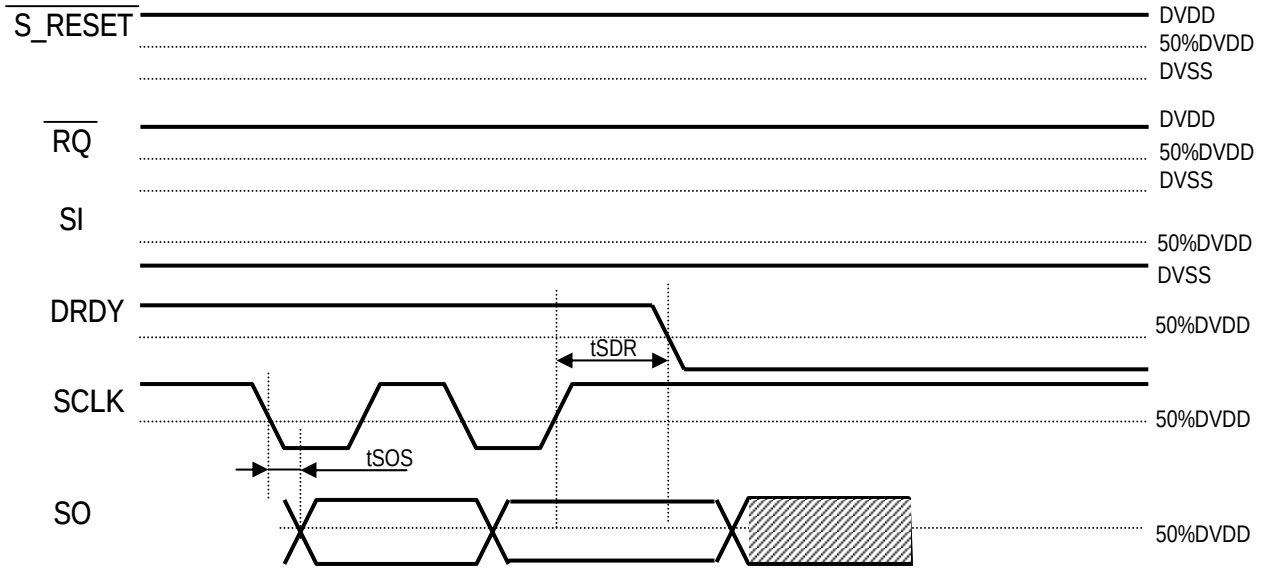
■ AK7730A → Microcomputer



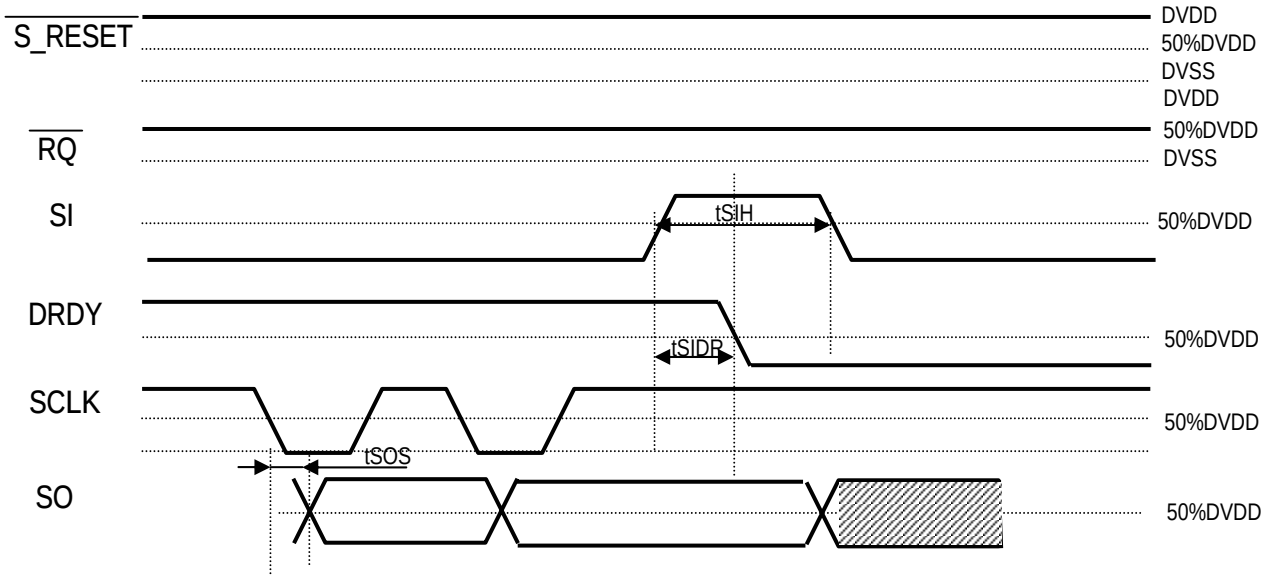
Note: The timing of the RUN state is the same except $\overline{\text{S\_RESET}}$ is "H".

■ AK7730A → Microcomputer (DBUS Output)

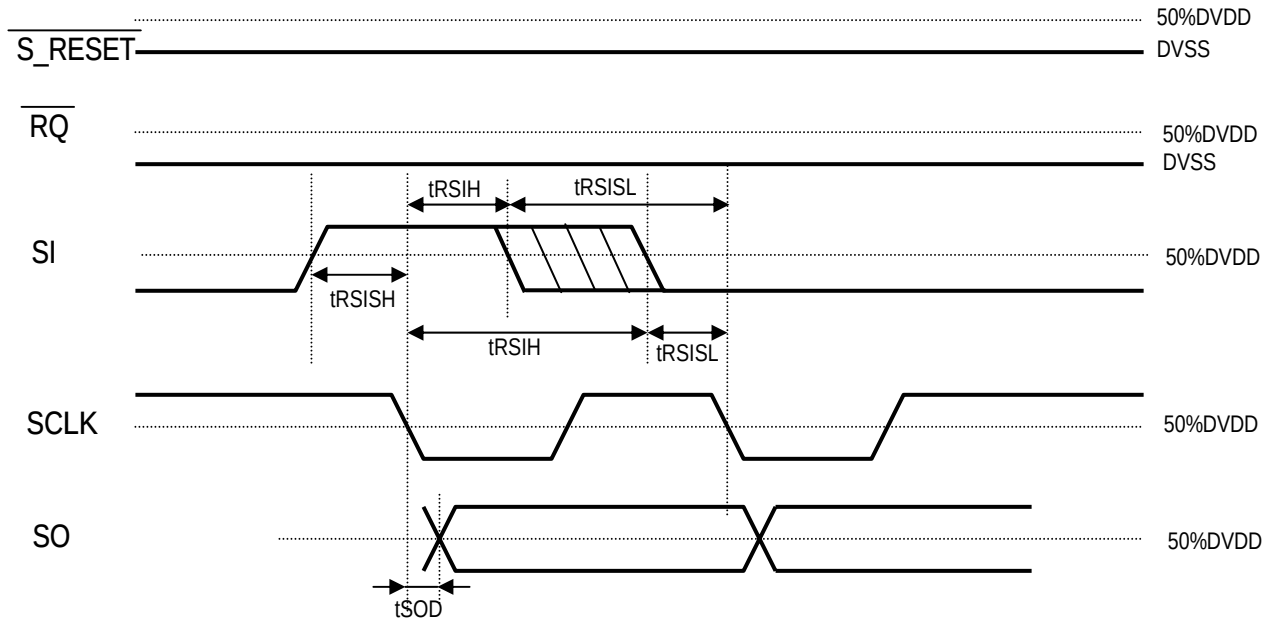
1) DBUS 24-bit output



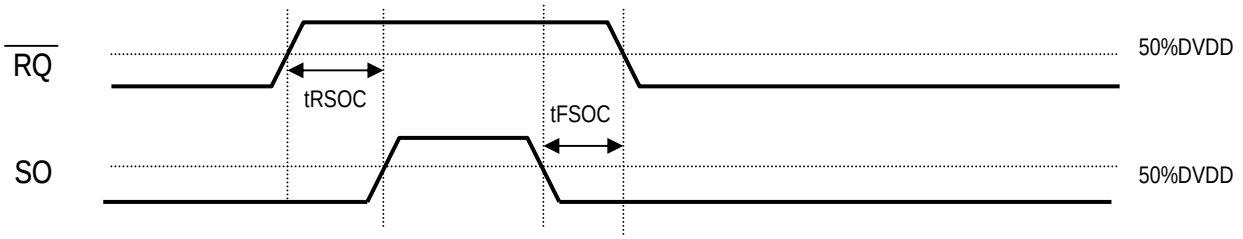
2) DBUS less than 24-bit (In case of using SI control)



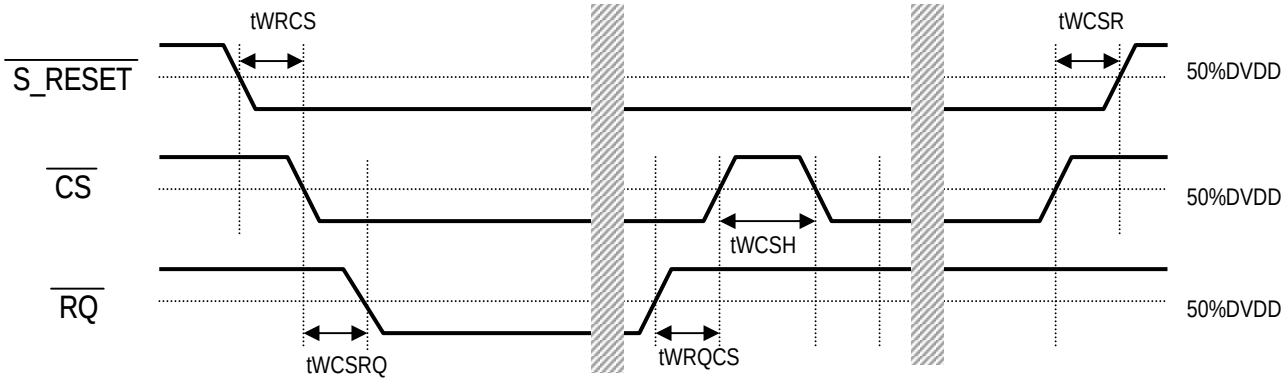
■ AK7730A → Microcomputer (Read out RAM DATA)

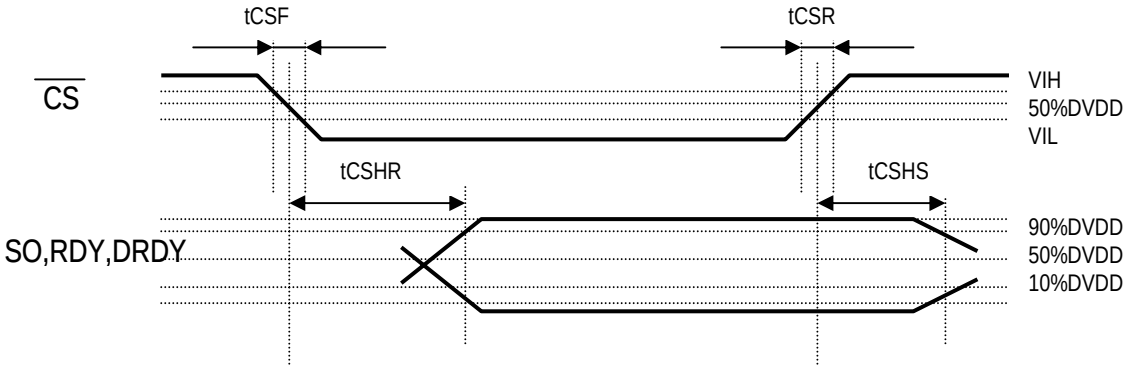


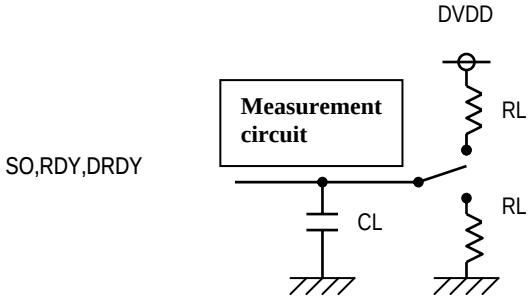
■ AK7730A → Microcomputer (CRC Check: {the surplus of D(x)/G(x)}=R(x))



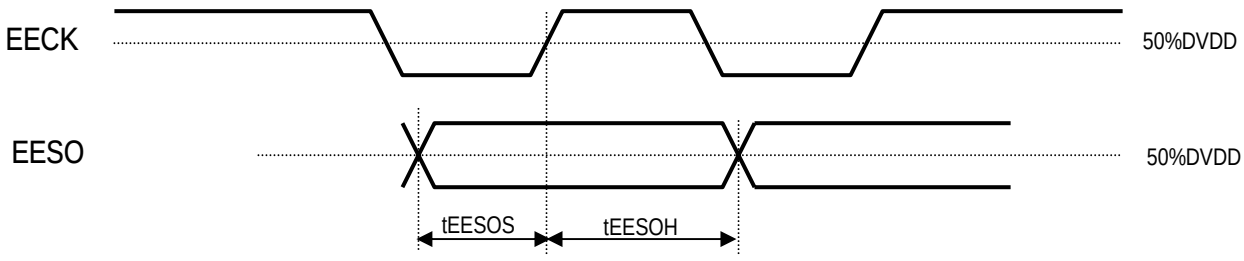
■ $\overline{CS}$ (EESEL="L" or OPEN)







■ EEPROM→ AK7730A



8. Function Description

(1) Various setting

1-1) SMODE: slave and master mode selector pin

This pin setting decides LRCLK and BITCLK to either inputs or outputs.

a) Slave mode: SMODE="L" LRCLK (1fs) and BITCLK (64fs or 48fs) become inputs.

b) Master mode: SMODE="H" LRCLK (1fs) and BITCLK (64fs) become outputs.

Note) SMODE pin designed as fixed “L” or “H”. Therefore, after release the initial reset($\overline{\text{INIT\_RESET}}$ =”L”→”H”) this pin must change during the system reset state ($\overline{\text{S\_RESET}}$ ="L") . Especially , at the slave mode, it begins phase matching between internal and external clock by the release of sysytem reset (See (8.(4)) Resetting). DO NOT CHANGE SMODE at runtime, It will cause an error.

1-2) CKS1,CKS0 : Master clock (XTI) select pin

Mode	CKS[1:0]	Clock Series	XTI input frequency (MHz)	XTI available input Frequency range (MHz)	Internal PLL	Maximum number of DSP steps (fs=48kHz)
0	0h	384fs series	18.432, 16.9344	16.0~18.6	Use	768
1	1h	256fs series	12.288, 11.2896	11.0~12.4	Use	768
2	2h	512fs series	24.576, 22.5792	22.0~24.8	Use	768
3	3h	768fs series	36.864, 33.8688	24.0~37.0	Not Use	768 (XTI=36.864MHz)

Note) CKS1=CKS[1],CKS0=CKS[0], Mode 3 can not use crystal oscillator.
Mode 3 can not use the crystal oscillator.
The maximum frequency of the master clock (MCLK) is 36.864MHz.

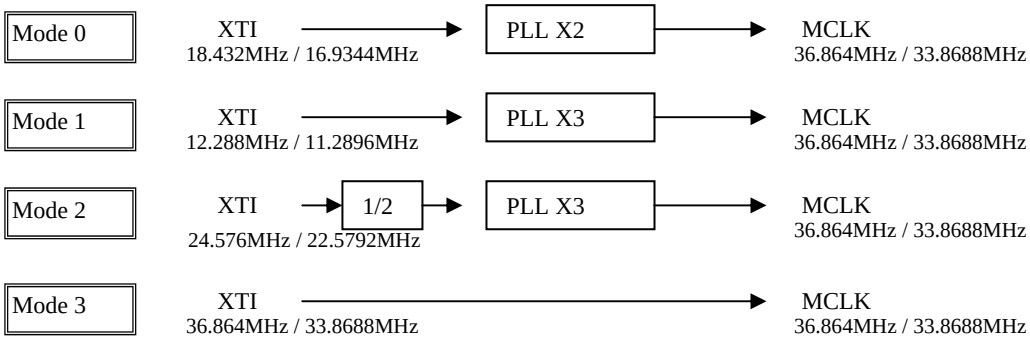


Fig. Relationship of XTI and MCLK (internal master clock)

Normally it will use mode 0 or 1.(When CKS1 and CKS0 leave open, it is selected mode 0.)
Mode 2 is used when 512fs master clock must be supplied. Mode 3 is used when internal PLL is not used.

After power up, it should change the setting of CKS1 and CKS0 during the initial reset($\overline{\text{INIT\_RESET}}$ =”L”, $\overline{\text{S\_RESET}}$ =”L”). Because of CKS1 and CKS0 pins control internal PLL circuit clock, the AK7730A may no operate correctly if these pins change in runtime. XTI frequency changes should also be done during the initial reset.

The sampling rate changing can be done by the control register setting.

(2) Control registers

The control registers can be set via the microcomputer interface in addition to the control pins. These 6 registers consist of 7-bit data however; SCLK always needs 16bit clock (Command Code 8bit, Data 8bit). Each register is set after the last D0 data is written. For the value to be written in the control registers see the description of the interface with microcomputer. The following describes the control register map.

These control registers are initialized by $\overline{\text{INIT\_RESET}}$ ="L", but these are NOT initialized by $\overline{\text{S\_RESET}}$ ="L".

TEST: for TEST (input 0,X: it ignores input data, but should input 0).

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	
W	R										
60h	70h	CONT0	DFS2	DFS1	DFS0	DIFS	DIF1	DIF0	SETCK	X	00h
62h	72h	CONT1	DARARAM	RM	BANK1	BANK0	CMP_N	SS1	SS0	X	00h
64h	74h	CONT2	PSAD	SWA	SWQA	SSDIN3	TEST	TEST	TEST	X	00h
66h	76h	CONT3	SWJX2	SWJX1	SWJX0	SWQ4	SWQ3	SWQ2	SWQ1	X	00h
68h	78h	CONT4	$\overline{\text{CLK1E}}$	CLK1S1	CLK1S0	$\overline{\text{CLK2E}}$	CLK2S1	CLK2S0	TEST	X	00h
6Ah	7Ah	CONT5	SWEE	SETC1	SETC2	TEST	TEST	TEST	TEST	X	00h

1. CONT0 and CONT5 can be set only at system reset ($\overline{\text{S\_RESET}}$ ="L").
2. CONT1~4 should be set at system reset ($\overline{\text{S\_RESET}}$ ="L"), otherwise an unwanted noise could be sent to the outputs.
3. TEST bit is used for test therefore set 0.
4. Default setting is the same value that is initialized by initial reset ($\overline{\text{INIT\_RESET}}$ ="L").

2-1) CONT0: Sampling rate and initerface selection

This register is enable only at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	DFS2	DFS1	DFS0	DIFS	DIF1	DIF0	SETCK	X	00h

① D7,D6,D5:DFS2,DFS1,DFS0 Sampling rate setting.

fs:Sampling frequency

Mode	DFS2	DFS1	DFS0	CKS[1:0] (Input frequency of XTI)				fs(kHz)	DSP Number of Steps
				0h	1h	2h	3h		
0	0	0	0	384fs	256fs	512fs	768fs	48,44.1	768
1	0	0	1	192fs	128fs	256fs	384fs	96(,88.2)	384
2	0	1	0	96fs	64fs	128fs	192fs	192(,176.4)	192
3	0	1	1	576fs	384fs	768fs	1152fs	32(,29.4)	1152
4	1	0	0	1536fs	1024fs	2048fs	3072fs	12(,11.025)	3072
5	1	0	1	768fs	512fs	1024fs	1536fs	24(,22.05)	1536
6	1	1	0	1152fs	768fs	1536fs	2304fs	16(,14.7)	2304
7	1	1	1	2304fs	1536fs	3072fs	4608fs	8	4608

Note 1) Except Mode 0~5 setting and sampling rate is prohibited.
Note 2) In case of select Mode 2, it must set "1" on CONT2 PSAD(D7).

② D4:DIFS Audio interface selection

0: AKM method
1: I^2S compatible (In this case, all input / output pins are I^2S compatible.)

③ D3,D2:DIF1,DIF0 SDIN1,SDIN2,SDIN3,SDIN4A Input mode selector

Mode	DIF1	DIF0	
0	0	0	MSB justified (24bit)
1	0	1	LSB justified (24bit)
2	1	0	LSB justified (20bit)
3	1	1	LSB justified (16bit)

Note) When D4= 1, the state is I^2S compatible independently of mode setting, however set to Mode 0.

④ D1: SETCK

Select output clock when the condition of CONT5 SETC1=1 or SETC2=1

CONT0			DFS2	DFS1	DFS0			
DFS Mode	0	1	2	3	4	5	6	7
SETCK=0	256fs	N/A	N/A	256fs	1024fs	1024fs	512fs	1024fs
SETCK=1	64fs	64fs	64fs	64fs	256fs	256fs	128fs	256fs

⑤ D0: Always 0

When inputs D0, CONT0 setting is fixed.

Note) Underline of the settings with "_" mean default setting.

2-2) CONT1: RAM control

Recommend this register changing at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
62h	72h	CONT1	DATARAM	RM	BANK1	BANK0	CMP_N	SS1	SS0	X	00h

Note) In case of not using DLRAM, it should select mode 2 or 3 on D4,D5.

① D7:DATARAM DATARAM addressing mode selector

0: Ring addressing mode

1: Linear addressing mode

DATARAM has 256-word x 24-bit and has 2 addressing pointer (DP0, DP1).

The Ring addressing mode: It's starting address increments by 1 every sample period.

The Linear addressing mode: Its starting address is always same, DP0 = 00h and DP1 = 80h.

② D6:RM: Decompress bit mode

0: SIGN bit

1: Random data

When it selects Compress & Decompress mode (D3:CMP_N = 0), this bit decides decompressed LSB bits.

③ D5,D4:BANK[1:0] DLRAM Setting

Mode	BANK1:D5	BANK0:D4	Memory
0	0	0	24bit 3kword(RAM A)
1	0	1	12bit 6kword(RAM A)
2	1	0	12bit 4kword(RAM A),24bit 1kword(RAM B)
3	1	1	24bit 1kword(RAM A),12bit 4kword(RAM B)

Note) When the mode 0 or 1 is selected, the pointer 0 and 1 are available for both RAM area.
When the mode 2 or 3 is selected, the pointer 0 is available for the RAM A and the pointer is available for the RAM B.
In case of not using DLRAM, it should select mode 2 or 3.

④ D3:CMP_N 12bitDLRAM Compress & Decompress selector

When mode 1,2 or 3 is selected, this register can set up ON or OFF of its compress/decompress function.

0: Compress & Decompress function ON

When it writes to DLRAM the DBUS data is compressed to 12-bit and when it read from DLRAM, the data is depressed to 24-bit.

1: Compress & Decompress function OFF

It always writes to DLRAM MSB 12-bit of DBUS data and it read from MSB 12-bit of DLRAM and add to 000h for LSB bits.

⑤ D2,D1:SS[1:0] DLRAM setting of sampling timing (only for RAM A)

Mode	SS1:D2	SS0:D1	RAM A mode selected by BANK[1:0]
0	0	0	Update every sampling time
1	0	1	Update every 2 sampling time
2	1	0	Update every 4 sampling time
3	1	1	Update every 8 sampling time

Note) When the mode 1,2 or 3 is selected, it comes out aliasing.

⑥ D0: Input always 0

When inputs D0, CONT1 setting is fixed.

Note) Underlines of the setting of "_" mean default setting.

2-3) CONT2: ADC control and others (see 3.Block diagram)

Recommend this register changing at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
64h	74h	CONT2	PSAD	SWA	SWQA	SSDIN3	TEST	TEST	TEST	X	00h

① **D7:PSAD**

0:Normal operation
1:ADC power save

In the case of not using ADC, set this value to "1" and ADC will be in RESET.
This can be useful for saving power consumption.
The digital output signals of ADC will be 00000h.
When changing to normal operation, set this value to "0" at system reset.

② **D6:SWA** (See 3. Block diagram.)

0: Normal operation (ADC SDATA connected to DSP SDIN4)
1: JX0/SDIN4A pin connected to DSP SDIN4.

③ **D5:SWQA** (See 3. Block diagram.)

0: In the case of SWQ4=1, JX0/SDIN4A pin connected to SDOUT4
1: In the case of SWQ4=1, ADC SDATA connected to SDOUT4.

④ **D4: SSDIN3 load source selector for DBUS**

0:DR2,DR3 through output
1:SDIN3 Digital input (Lch,Rch)

⑤ **D3:TEST**

0:Normal operation
1:Test mode (Do NOT use this mode)

⑥ **D2:TEST**

0:Normal operation
1:Test mode (Do NOT use this mode)

⑦ **D1:TEST**

0:Normal operation
1:Test mode (Do NOT use this mode)

⑧ **D0: Always input 0**

When inputs D0, CONT2 setting is fixed.

Note): Underlines of the setting of "_" mean default setting.

2-4) CONT3 : Internal path setting (see. 3.block diagram)

Recommend this register changing at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
66h	76h	CONT3	SWJX2	SWJX1	SWJX0	SWQ4	SWQ3	SWQ2	SWQ1	X	00h

① **D7:SWJX2**
0:SDIN2/JX2 pin uses as SDIN2 pin (JX2=0)
1:SDIN2/JX2 pin uses as JX2 pin.

② **D6:SWJX1**
0:SDIN3/JX1 pin uses as SDIN3 pin (JX1=0)
1:SDIN3/JX1 pin uses as JX1 pin.

③ **D5:SWJX0**
0:JX0/SDIN4A pin uses as JX0 pin
1:JX0/SDIN4A pin uses as SDIN4A (JX0=0)

④ **D4:SWQ4**
0: Output DSP SDOUT4
1:SWQA=0; Output JX0/SDIN4A.
SWQA=1; Output ADC SDATA.

⑤ **D3:SWQ3**
0:Output DSP SDOUT3.
1:Output SDIN3/JX1.

⑥ **D2:SWQ2**
0:Output DSP SDOUT2.
1:Output SDIN2/JX2

⑦ **D1:SWQ1**
0:Output DSP SDOUT1.
1:Output SDIN1

⑧ **D0: Always input 0**
When inputs D0, CONT3 setting is fixed.

Note) Underlines of the setting of "_" mean default setting.

2-5) CONT4:CLKO1,CLKO2 setting 1

Recommend this register changing at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
68h	78h	CONT4	$\overline{\text{CLK1E}}$	CLK1S1	CLK1S0	$\overline{\text{CLK2E}}$	CLK2S1	CLK2S0	TEST	X	00h

Noise may comes out when it changes CLKO1 or CLKO2.

Once CLKO1 or CLKO2 outputs, it can not stop without $\overline{\text{CLK1E}}$ =1, $\overline{\text{CLK2E}}$ =1 setting or initial reset.

① D7: $\overline{\text{CLK1E}}$ CLKO1 output control

0: CLKO1 outputs clock selected by CLK1S1 and CLK1S0
1: CLKO1 outputs "L".

② D6,D5:CLK1S1,CLKS0 CLKO1 output clock select.

Mode	CLK1S1	CLK1S0	CLKO1
0	0	0	MCLK/2
1	0	1	MCLK/3
2	1	0	MCLKx2/9
3	1	1	TEST

Note1) MCLK is an internal clock. MCLK is changed by the input frequency of the XTI.
Normaly MCLK=36.864MHz or 33.8688MHz. see (5) System Clock 1) Master clock select table.

Note2) It is time from $\overline{\text{INIT\_RESET}}$ release to clock begins to output.
CKS[1:0]=0h(XTI=18.432MHz) : 15ms(max)
CKS[1:0]=1h(XTI=12.288MHz) : 22ms(max)
CKS[1:0]=2h(XTI=24.576MHz) : 22ms(max)

③ D4: $\overline{\text{CLK2E}}$ CLKO2 output control

0: CLKO2 outputs clock selectected by CLK2S1 and CLK2S0.
1: CLKO2 outputs "L".

④ D3,D2:CLK2S1,CL2S0 CLKO2 output clock select

Mode	CLK2S1	CLK2S0	CLKO2
0	0	0	MCLK/2
1	0	1	MCLK/3
2	1	0	MCLKx2/9
3	1	1	TEST

Note : same as Note1) and Note2) of ②.

⑤ D1:TEST
0:Normal operation
1:TESTmode (Do NOT use this mode)

⑥ D0: Always input 0
When inputs D0, CONT4 setting is fixed.

Note) Underlines of the setting of "_" mean default setting.

2-6) CONT5: CLKO1,CLKO2 setting 2

This register is enabled only at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
6Ah	7Ah	CONT5	SWEE	SETC1	SETC2	TEST	TEST	TEST	TEST	X	00h

Note) Set this register after setting CONT0.

① **D7: SWEE Select CLKO2 output**
0: CLKO2(@EESEL="L"),EEST(@EESEL="H")
1: CLKO2(@EESEL="L" or "H")

② **D6: SETC1**
0: Output CLKO1 clock that selected by CONT4 CLK1S1 and CLK1S0
1: Output CLKO1 clock that selected by CONT0 SETCK

Note) When SETC1 selected "1", CLKO1 outputs clock that SETCK setting by the system reset release.
When changing this register, it comes out click noise at CLKO1.
When CLKO1 outputs, it can not stop until $\overline{\text{CLK1E}}$ =1 or initial reset. (Clock is requied.)

③ **D5: SETC2**
0: Output CLKO2 clock that selected by CONT4 CLK2S1 and CLK2S0
1: Output CLKO2 clock that selected by CONT0 SETCK

Note) When SETC2 selected "1", CLKO2 outputs clock that SETCK setting by the system reset release.
When changing this register, it comes out click noise at CLKO2.
When CLKO2 outputs, it can not stop until $\overline{\text{CLK2E}}$ =1 or initial reset. (Clock is requied.)
Even in EESEL="H" condition, if SETC2=1 then SETC2 setting is valid.

④ **D4:TEST**
0:Normal operation
1:TESTmode (Do NOT use this mode)

⑤ **D3:TEST**
0:Normal operation
1:TESTmode (Do NOT use this mode)

⑥ **D2:TEST**
0:Normal operation
1:TESTmode (Do NOT use this mode)

⑦ **D1:TEST**
0:Normal operation
1:TESTmode (Do NOT use this mode)

⑧ **D0: Always input 0**
When inputs D0, CONT5 setting is fixed.

Note) Underlines of the setting of "_" mean default setting.

(3) Power supply startup sequence

At the rising of AVDD and DVDD, $\overline{\text{INIT\_RESET}}$ and $\overline{\text{S\_RESET}}$ should be set to “L”.

$\overline{\text{INIT\_RESET}}$ = “L” makes all control registers initialize. Note 1), Note 2). Then the VREF (Analog reference level) of the AK7730A is set up and it begins to generate internal master clock by setting to $\overline{\text{INIT\_RESET}}$ = “H”. The interface of the AK7730A cannot accept before PLL locks. So, it must wait at least 22ms from $\overline{\text{INIT\_RESET}}$ = “H”. Note 3)

Normally, $\overline{\text{INIT\_RESET}}$ setting is only done at turn on power.

Note 1): To confirm initialization it requires power up and master clock (XTI) supplied.

Note 2): Set to $\overline{\text{INIT\_RESET}}$ = “H” after setting the oscillation when a crystal oscillator is used.
This setting time may differ depending on the crystal oscillator and its external circuit.

Note 3): In case of CKS[1:0] = 0h then waiting time is 15ms. CKS[1:0] = 1h or 2h then waiting time is 22ms.

NOTE: Do not stop the system clock (slave mode: XTI, LRCLK, BITCLK, master mode: XTI) except when $\overline{\text{S\_RESET}}$ = "L". If these clock signals are not supplied, excess current will flow due to dynamic logic that is used internally, and an operation failure may result.

Don’t set $\overline{\text{S\_RESET}}$ ="H" during $\overline{\text{INIT\_RESET}}$ ="L", unless its crystal oscillator will stop or be in unstable.

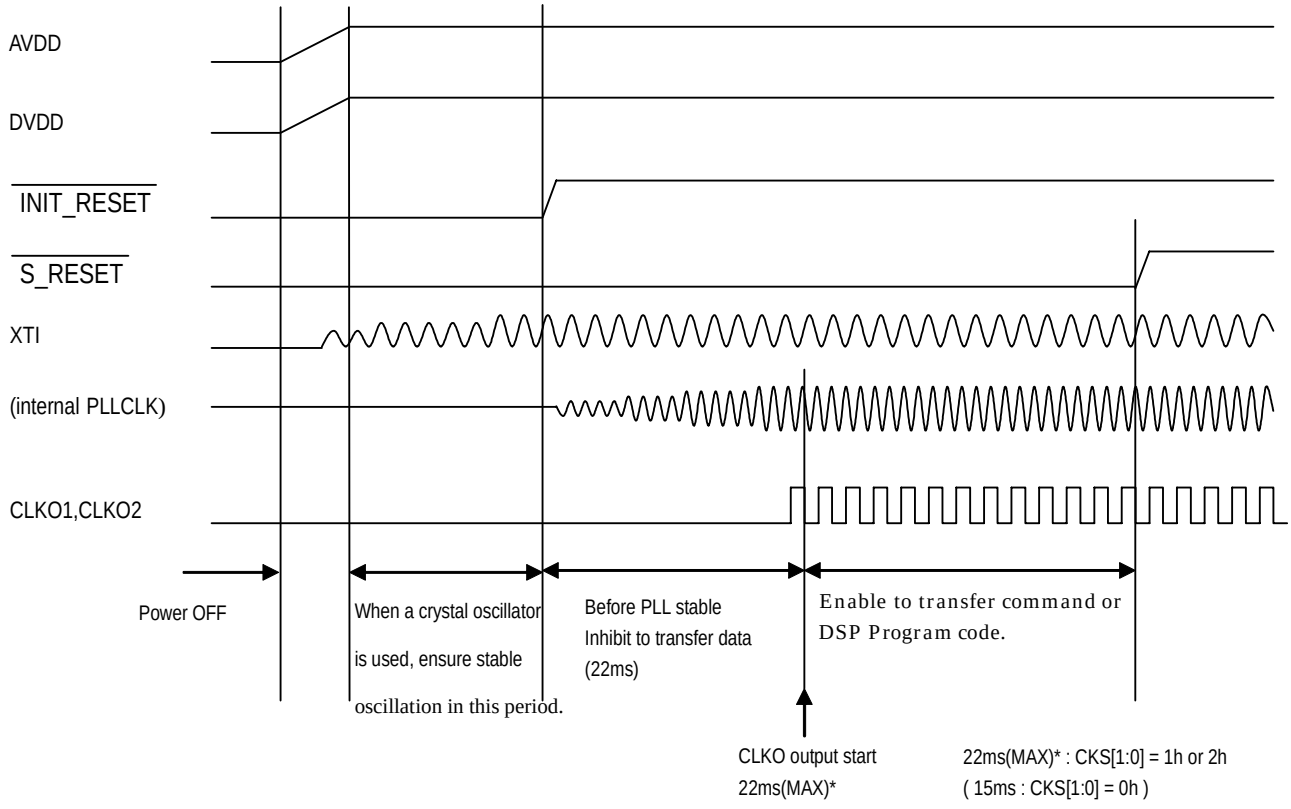


Fig. Power supply startup sequence

(4) Resetting

The AK7730A has two reset pins: $\overline{\text{INIT\_RESET}}$ and $\overline{\text{S\_RESET}}$.

The $\overline{\text{INIT\_RESET}}$ pin is used to set up VREF and initialize the AK7730A, as shown in "Power supply startup sequence section (3)."

The system is reset when $\overline{\text{S\_RESET}}$ ="L". (Description of "reset" is for "system reset".)

During a system reset, a program write operation is normally performed (except for write operation during running).

During the system reset phase, the ADC sections are also reset. (The digital section of ADC output is MSB first 00000h). However, VREF will be active; LRCLK and BITCLK in the master mode will be inactive**.**

The system reset is released by setting $\overline{\text{S\_RESET}}$ to "H", which activates the internal counter.

This counter generates LRCLK and BITCLK in the master mode: however, a problem may occur when a clock signal is generated.

When the system reset is released in slave mode, internal timing will be actuated in synchronization with rising edge "↑" of LRCLK (when the standard input format is used). Timing between the external and internal clocks is adjusted at this time. Therefore make sure to avoid phase difference between LRCLK and internal timing. If the phase difference in LRCLK and internal timing is within about -1/16 to 1/16 of the input sampling cycle (1/fs) during the operation, the operation is performed with internal timing remaining unchanged. If the phase difference exceeds the above range, the phase is adjusted by synchronizing the "↑" of LRCLK (when the standard input format is used). This prevents synchronization failure with the external circuit.

The ADC section can output 516-LRCLK after its internal counter has started. (The internal counter starts at the first rising edge of LRCLK in master mode. In slave mode, it starts 2 LRCLKs after the release of system reset.)

The AK7730A performs normal operation when $\overline{\text{S\_RESET}}$ is set to "H".

(5) System clock

1) master clock select table.

(A) Sampling frequency 48kHz series (Normal :48kHz, Double:96kHz, Quadruple:192kHz)

XTI	INPUT PIN CKS1	INPUT PIN CKS0	CONT0 DFS2	CONT0 DFS1	CONT0 DFS0	FS [KHz]	DSP STEP	MCLK [MHz]	PLL active	AD active	X'tal active
18.432	0	0	0	0	0	48	768	36.864	○	○	○
↑	↑	↑	0	0	1	96	384	↑	○	○	○
↑	↑	↑	0	1	0	192	192	↑	○	×	○
↑	↑	↑	0	1	1	32	1152	↑	○	○	○
↑	↑	↑	1	0	0	12	3072	↑	○	○	○
↑	↑	↑	1	1	1	8	4608	↑	○	○	○
12.288	0	1	0	0	0	48	768	36.864	○	○	○
↑	↑	↑	0	0	1	96	384	↑	○	○	○
↑	↑	↑	0	1	0	192	192	↑	○	×	○
↑	↑	↑	0	1	1	32	1152	↑	○	○	○
↑	↑	↑	1	0	0	12	3072	↑	○	○	○
↑	↑	↑	1	1	1	8	4608	↑	○	○	○
24.576	1	0	0	0	0	48	768	36.864	○	○	○
↑	↑	↑	0	0	1	96	384	↑	○	○	○
↑	↑	↑	0	1	0	192	192	↑	○	×	○
↑	↑	↑	0	1	1	32	1152	↑	○	○	○
↑	↑	↑	1	0	0	12	3072	↑	○	○	○
↑	↑	↑	1	1	1	8	4608	↑	○	○	○
36.864	1	1	0	0	0	48	768	36.864	×	○	×
↑	↑	↑	0	0	1	96	384	↑	×	○	×
↑	↑	↑	0	1	0	192	192	↑	×	×	×
↑	↑	↑	0	1	1	32	1152	↑	×	○	×
↑	↑	↑	1	0	0	12	3072	↑	×	○	×
↑	↑	↑	1	1	1	8	4608	↑	×	○	×

(B) Sampling frequency 44.1kHz series (Normal: 44.1kHz, Double: 88.2kHz, Quadruple:176.4kHz)

XTI	INPUT PIN CKS1	INPUT PIN CKS0	CONT0 DFS2	CONT0 DFS1	CONT0 DFS0	FS [KHz]	DSP STEP	MCLK [MHz]	PLL Active	AD Active	X'tal Active
16.9344	0	0	0	0	0	44.1	768	33.8688	○	○	○
↑	↑	↑	0	0	1	88.2	384	↑	○	○	○
↑	↑	↑	0	1	0	176.4	192	↑	○	×	○
↑	↑	↑	0	1	1	29.4	1152	↑	○	○	○
↑	↑	↑	1	0	0	11.025	3072	↑	○	○	○
↑	↑	↑	1	1	1	7.35	4608	↑	○	○	○
11.2896	0	1	0	0	0	44.1	768	33.8688	○	○	○
↑	↑	↑	0	0	1	88.2	384	↑	○	○	○
↑	↑	↑	0	1	0	176.4	192	↑	○	×	○
↑	↑	↑	0	1	1	29.4	1152	↑	○	○	○
↑	↑	↑	1	0	0	11.025	3072	↑	○	○	○
↑	↑	↑	1	1	1	7.35	4608	↑	○	○	○
22.5792	1	0	0	0	0	44.1	768	33.8688	○	○	○
↑	↑	↑	0	0	1	88.2	384	↑	○	○	○
↑	↑	↑	0	1	0	176.4	192	↑	○	×	○
↑	↑	↑	0	1	1	29.4	1152	↑	○	○	○
↑	↑	↑	1	0	0	11.025	3072	↑	○	○	○
↑	↑	↑	1	1	1	7.35	4608	↑	○	○	○
33.8688	1	1	0	0	0	44.1	768	33.8688	×	○	×
↑	↑	↑	0	0	1	88.2	384	↑	×	○	×
↑	↑	↑	0	1	0	176.4	192	↑	×	×	×
↑	↑	↑	0	1	1	29.4	1152	↑	×	○	×
↑	↑	↑	1	0	0	11.025	3072	↑	×	○	×
↑	↑	↑	1	1	1	7.35	4608	↑	×	○	×

(C) CLKO1,2 Output select information

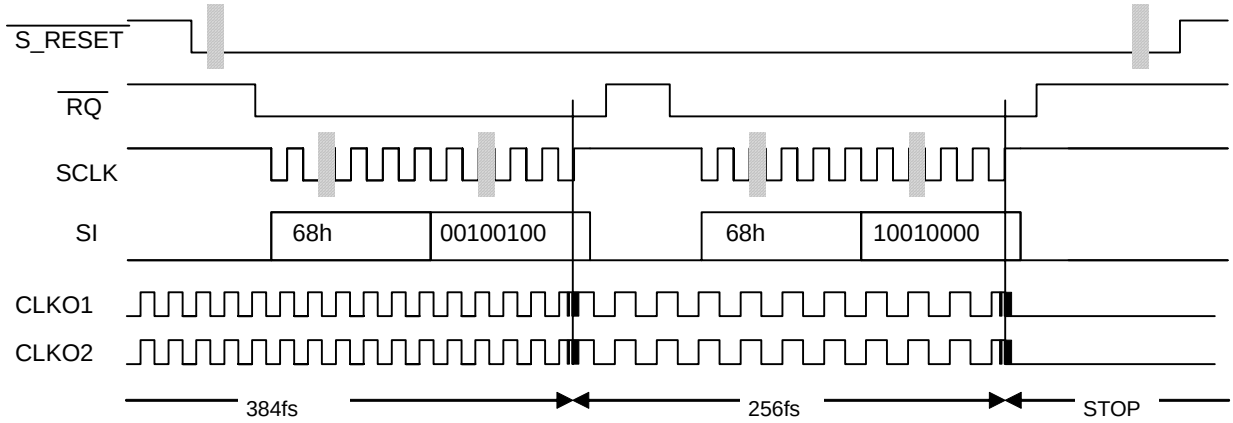
XTI	INPUT PIN CKS1	INPUT PIN CKS0	CONT5 SETC1/ SETC2	CONT4 CLK1S1/ CLK2S1	CONT4 CLK1S0/ CLK2S0	OUTPUT CLKO1 CLKO2[MHz]
18.432	0	0	0	0	0	18.432
			0	0	1	12.288
			0	1	0	8.192
			1	X	X	(256fs)
12.288	0	1	0	0	0	18.432
			0	0	1	12.288
			0	1	0	8.192
			1	X	X	(256fs)
24.576	1	0	0	0	0	18.432
			0	0	1	12.288
			0	1	0	8.192
			1	X	X	(256fs)
36.864	1	1	0	0	0	18.432
			0	0	1	12.288
			0	1	0	8.192
			1	X	X	(256fs)

(D) CLKO1,2 Output information

$\overline{\text{INIT\_RESET}}$	$\overline{\text{S\_RESET}}$	CLKO1/CLKO2	
		$\overline{\text{CLK1E}}$ / $\overline{\text{CLK2E}}$ = 0	$\overline{\text{CLK1E}}$ / $\overline{\text{CLK2E}}$ = 1
L	L	Stop	-
H	L	Active	Stop
H	H	Active	Stop

(E) Output timing image

The following figure indicates the timing of changing of CLKO1 and CLKO2.
(The phase of the clock is not always same as following figure.)



Example. Setting of CONT4 from 00h(Default) to other.

fs=48kHz,44.1kHz

2) Master clock (XTI pin)

The master clock is obtained by connecting a crystal oscillator between the XTI pin and XTO pin or by inputting an external clock into the XTI pin while the XTO pin is left open.

3) Slave mode

The required system clock is XTI, LRCLK (1 fs) and BITCLK (48/64 fs).
The master clock (XTI) and LRCLK must be synchronized, but the phase is not critical.

4) Master mode

The required system clock is XTI. When the master clock (XTI) is input, LRCLK (1 fs) and BITCLK (64 fs) will be outputted from the internal counter synchronized with the XTI. LRCLK and BITCLK will not be active during initial reset ($\overline{\text{INIT\_RESET}}$ ="L") and system reset ($\overline{\text{S\_RESET}}$ ="L").

(6) Audio data interface (internal connection mode)

The serial audio data pins SDIN1,SDIN2,SDIN3,SDIN4A,SDOUT1,SDOUT2,SDOUT3 and SDOUT4 are interfaced with the external system, using LRCLK and BITCLK. The ports SDINA1, SDINA2, SDOUTA1, SDOUTA2, SDOUTD1 and SDOUTD2 are not normally used. These ports are controlled via registers. (See the block diagram on page.2 and the control register setting section at page 28.)

The data format is MSB-first 2's complement. Normally, the input/output format, in addition to the standard format used by AKM, can be changed to I^2S compatible mode by setting the control register "CONT0 DIF (D5) to 1". (In this case, all input/output audio data pin interface are in the I^2S compatible mode.)

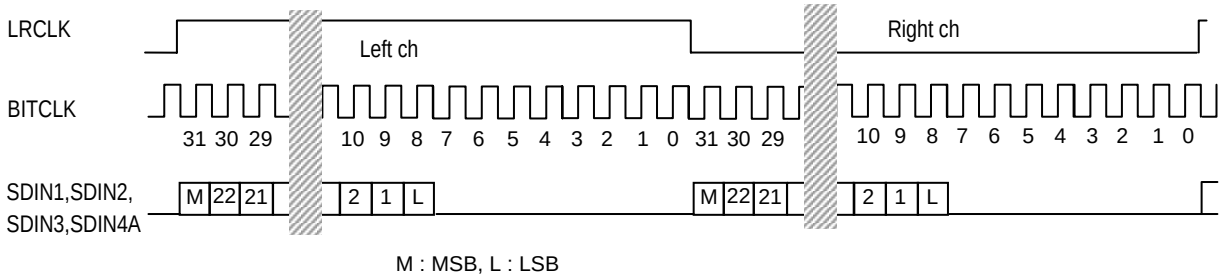
The input SDIN1, SDIN2, SDIN3 and SDIN4A formats are MSB justified 24-bit at initialization. Setting the control registers CONT0: DIF1 (D3), DIF0 (D2) will cause these ports to be compatible with LSB justified 24-bit, 20-bit and 16-bit.

However, individual setting of SDIN1, SDIN2, SDIN3 and SDIN4A is not allowed. The output SDOUT1, SDOUT2, SDOUT3 and SDOUT4 are fixed at 24-bit MSB justified only.

In slave mode BITCLK corresponds to not only 64fs but also 48fs. 64fs is the recommended mode. Following formats describe 64fs examples.

1) Standard input format (DIF = 0: default set value)

a) Mode 1 (DIF1, DIF0 = 0, 0: default set value)

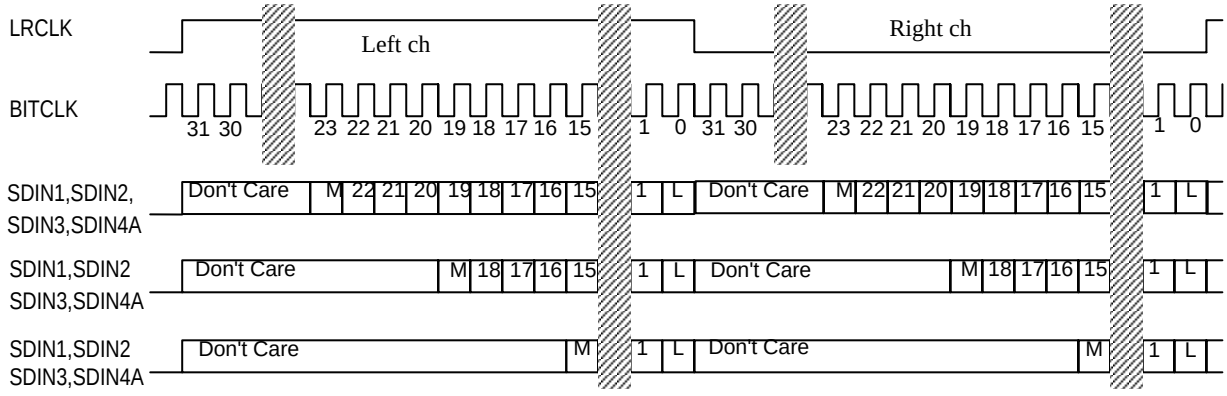


M : MSB, L : LSB

* When you want to input the MSB-justified 20-bit data into SDIN, SDINA input four "0" following the LSB.

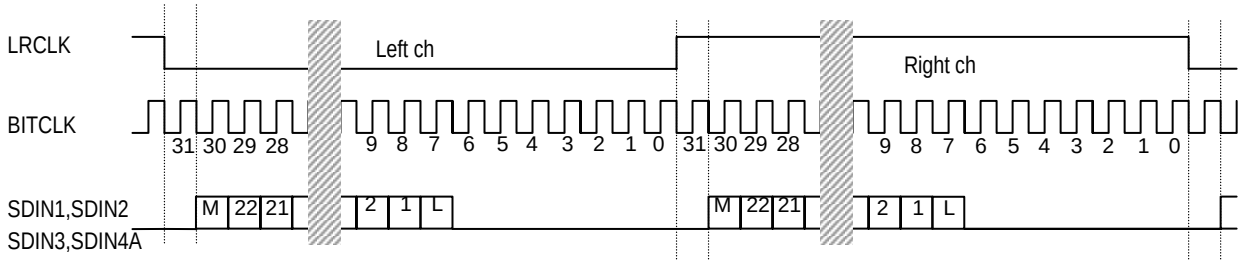
b) Mode 2, Mode 3, Mode 4

SDIN1,SDIN2,SDIN3,SDIN4A	Mode2 : (DIF1,DIF0)=(0,1)	LSB justified 24-bit
SDIN1,SDIN2,SDIN3,SDIN4A	Mode3 : (DIF1,DIF0)=(1,0)	LSB justified 20-bit
SDIN1,SDIN2,SDIN3,SDIN4A	Mode4 : (DIF1,DIF0)=(1,1)	LSB justified 16-bit



M : MSB, L : LSB

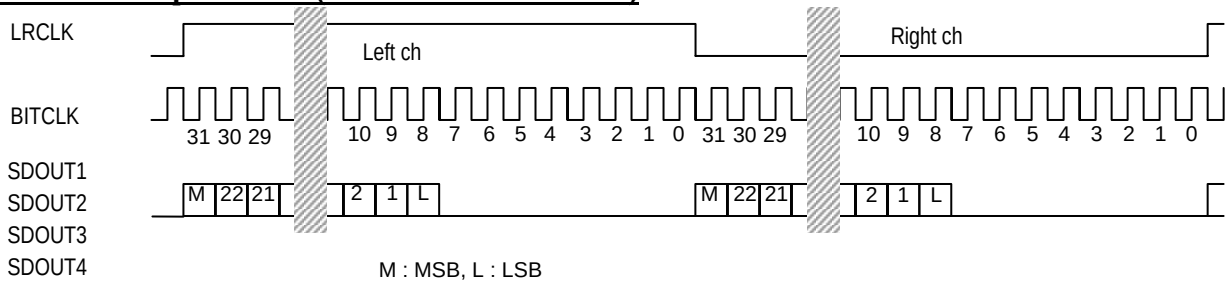
2) I²S compatible input format (DIF=1)



M : MSB, L : LSB

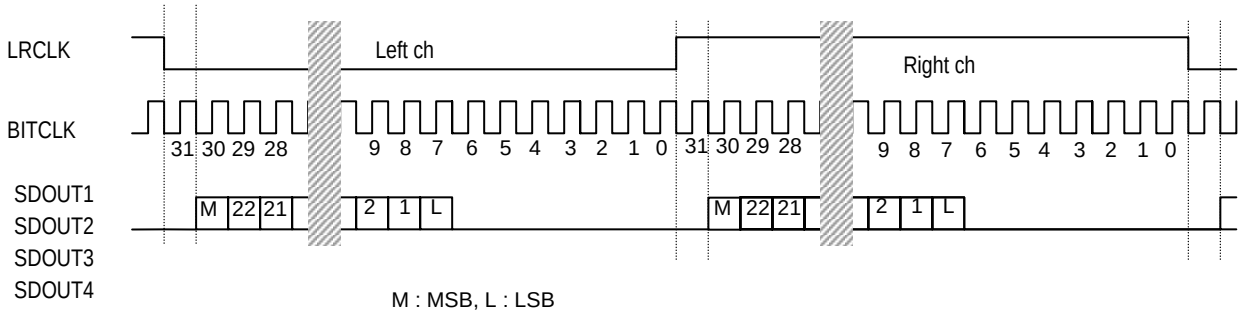
Mode 1: (DIF1(D4),DIF0(D3))=(0,0) must be set.

3) Standard output format (DIF=0: default set value)



M : MSB, L : LSB

4) I²S compatible output format (DIF=1)



M : MSB, L : LSB

(7) Interface with microcomputer

The microcomputer interface uses 6 control pins; $\overline{RQ}$ (ReQuest Bar), SCLK (Serial data input Clock), SI (Serial data Input), SO (Serial data Output), RDY (ReaDY) and DRDY (Data ReaDY).

In the AK7730A, two types of operations are provided; writing and reading during the reset phase (namely, system reset) and R/W during the run phase.

During the reset phase, writing of the control register, program RAM, coefficient RAM, offset RAM, external conditional jump code, and reading of the program RAM, coefficient RAM and offset RAM, are enabled.

During the run phase, writing of coefficient RAM, offset RAM and external conditional jump code, and reading of data on the DBUS (data bus) from the SO, is enabled. Its data is MSB first serial I/O.

When the AK7730A needs to transfer data to the microcomputer, it starts by $\overline{RQ}$ going "L" expects reading of data on the DBUS. The AK7730A reads SI data at the rising point of SCLK, and outputs to SO at the falling point of SCLK.
The AK7730A accepts first data as command then address data or some kinds of data input / output starts.
When $\overline{RQ}$ changes to "H", one command has finished. New command requests must set $\overline{RQ}$ to "L" again. For DBUS data reads, leave $\overline{RQ}$ ="H". (It does not need command code input.)

When it needs to clear the output buffer (MICR), the SI pin uses for control. (In this case, it is necessary to protect against a noise as SCLK.)
Command code table is as follow.

Command code list

Conditions for use	Code name	Command code		Remark:
		WRITE	READ	
RESET phase	CONT0	60h	70h	For the function of each bit, See the description of Control Registers.
	CONT1	62h	72h	
	CONT2	64h	74h	
	CONT3	66h	76h	
	CONT4	68h	78h	
	CONT5	6Ah	7Ah	
	PRAM	C0h	C1h	
	CRAM	A0h	A1h	
	OFRAM	90h	91h	
	External condition jump	C4h	-	
	CRC check (R(x))	B6h	D6h	
RUN phase	CONT0~CONT5	X	70h	Read available, same as RESET code.
	CRAM rewrite preparation	A8h	-	It needs to do before CRAM rewrite
	CRAM rewrite	A4h	-	
	OFRAM rewrite preparation	98h	-	It needs to do before OFRAM rewrite
	OFRAM rewrite	94h	-	
	External condition jump	C4h	-	Same code as RESET
	CRC check (R(x))	B6h	D6h	Same code as RESET

NOTE: Do not send other than the above command codes. Otherwise an operation error may occur.
If there is no communication with the microcomputer, set the SCLK to "H" and the SI to "L" for use.

1) Write during reset phase

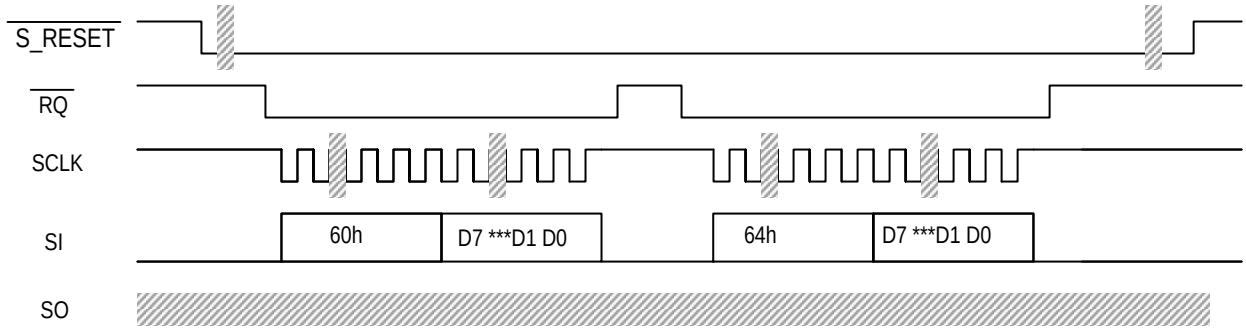
a) Control register write (during reset phase)

The data comprises a set of 2 bytes used to perform control register write operations (during reset phase). When all data has been entered, the new data is sent at the rising edge of the 16th count of SCLK.

Data transfer procedure

① Command code	60h,62h,64h,66h,68h,6Ah
② Control data	(D7 D6 D5 D4 D3 D2 D1 D0)

For the function of each bit, see the description of Control registers, (section 2).



Note) It must be set always 0 to D0.

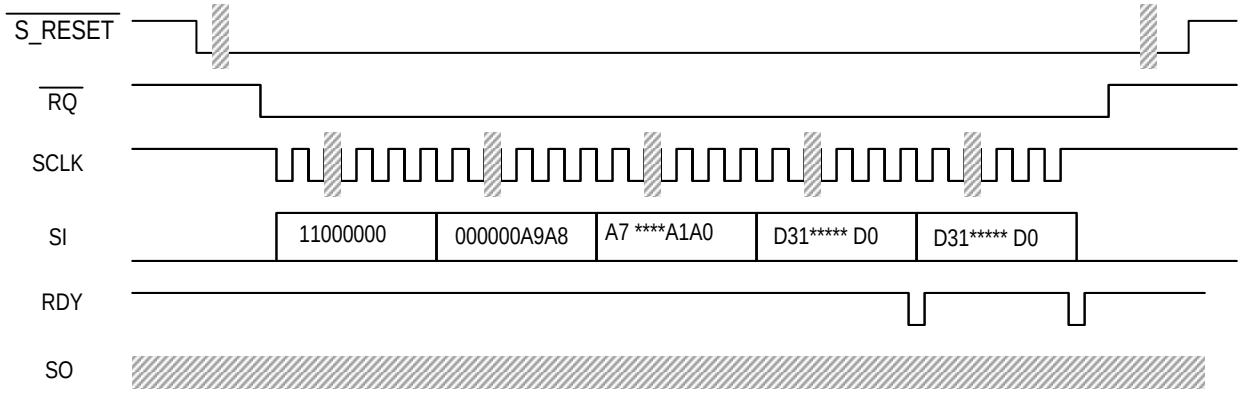
Control Registers write operation

b) Program RAM writes (during reset phase)

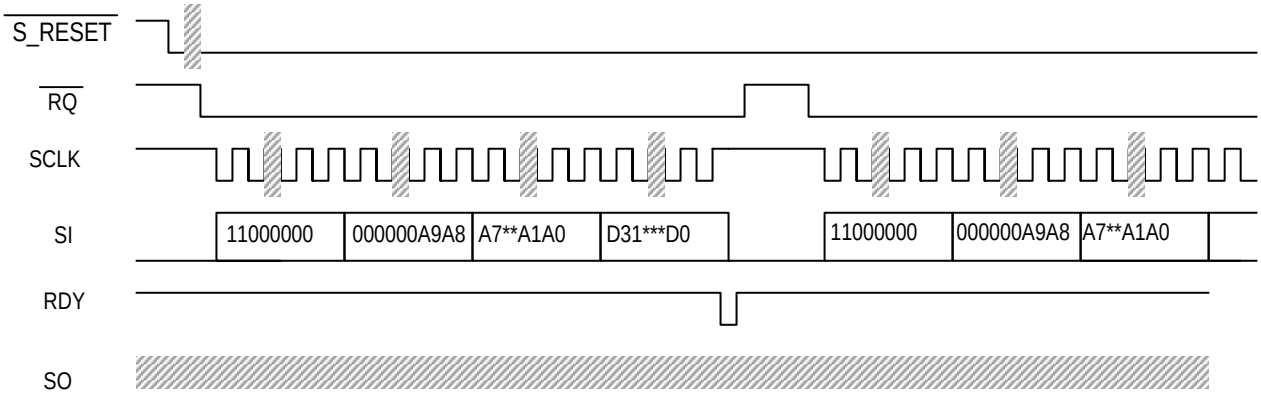
Program RAM write operations are performed during the reset phase using 7-bytes of data. When all data have been transferred, the RDY terminal is set to "L". Upon completion of writing into the PRAM, RDY returns “H” to allow the next data bit input. When writing to sequential addresses, input the data without a command code or address. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" again and then input the command code, address and data in that order.

Data transfer procedure

① Command code	C0h (1 1 0 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 A9 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D31 . . . . . D24)
⑤ Data	(D23 . . . . . D16)
⑥ Data	(D15 . . . . . D8)
⑦ Data	(D7 . . . . . D0)



Input of continuous address data into PRAM



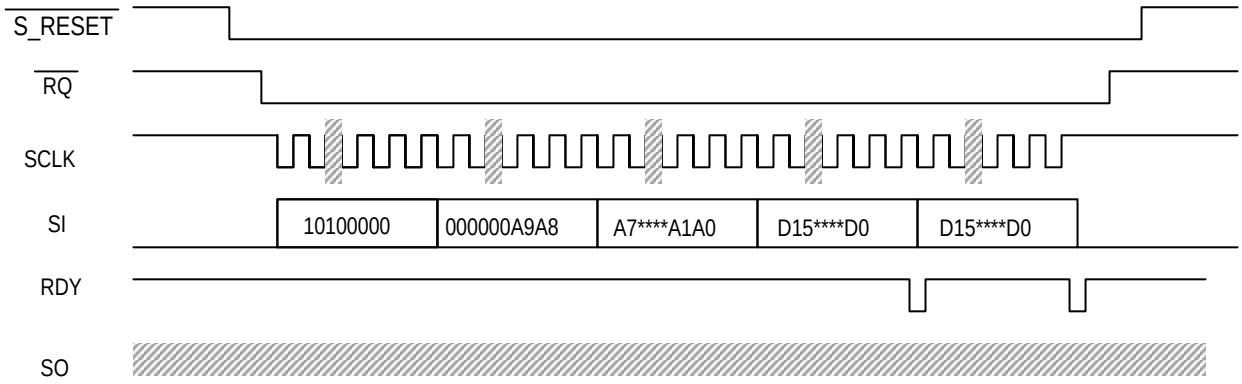
Input of discontinuous address data into PRAM

c) Coefficient RAM writes (during reset phase)

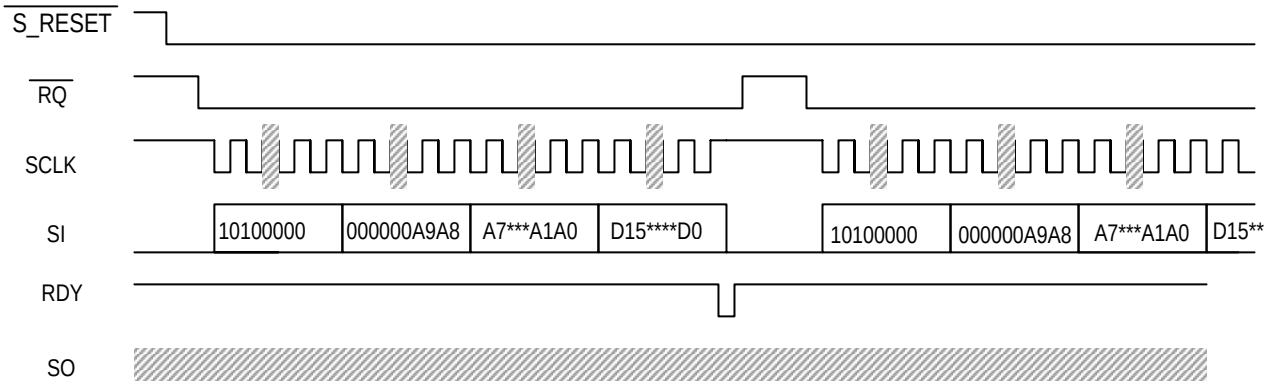
5 bytes of data are used to perform coefficient RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the CRAM, it goes to "H" to allow the next data to be input. When writing to sequential addresses, input the data as shown below. To write discontinuous data, transition the $\overline{RQ}$ terminal from "H" to "L" and then input the command code, address and data.

Data transfer procedure

① Command code	A0h (1 0 1 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 A9 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D15 . . . . . D8)
⑤ Data	(D7 . . . . . D0)



Input of continuous address data into CRAM

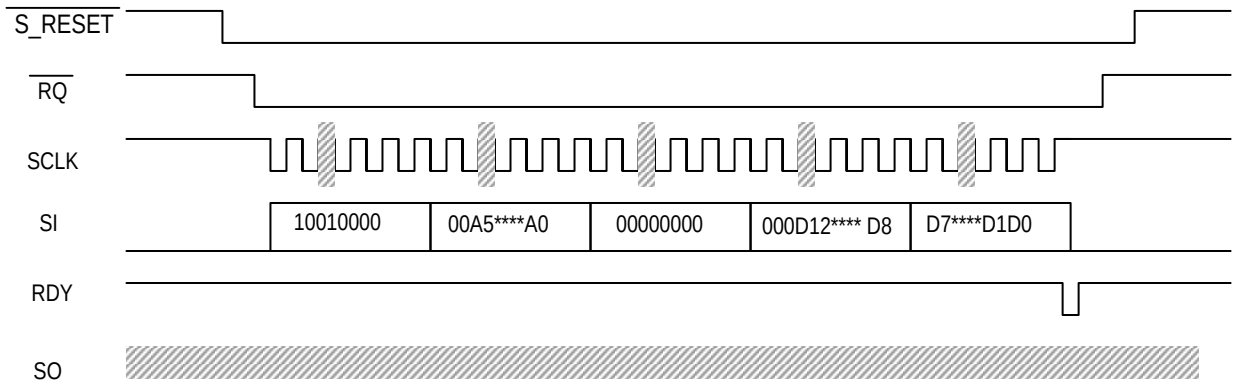


d) Offset RAM writes (during reset phase)

5 bytes of data are used to perform offset RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the OFRAM, it goes to "H" to allow the next data to be input. When writing to sequential addresses, input the data without a command code or address. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" and then input the command code, address and data in that order.

Data transfer procedure

① Command code	90h (1 0 0 1 0 0 0 0)
② Address	(0 0 A5 A4 .. . . A0)
③ Data	(0 0 0 0 0 0 0 0)
④ Data	(0 0 0 D12 D11 * * . D8)
⑤ Data	(D7 . . . . . D0)

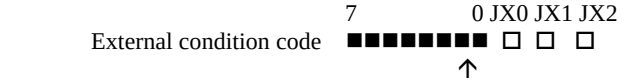


Input of data into OFRAM

e) External conditional jump code writes (during reset phase)

Two bytes of data are used to perform external conditional jump operations. The data can be entered during both the reset and operation phases, and the input data are set to the specified register at the leading edge of the LRCLK. When all data bits have been transferred, the RDY terminal goes to "L". Upon write completion, it goes to "H". A jump command will be executed if there is any one agreement between "1" of each bit of external condition code 8 bits (soft set) plus 3 bits (hard set) at the external input terminal JX0, JX1,JX2 and "1" of each bit of the IFCON field. The data during the reset phase can be written only before release of the reset, after all data has been transferred. $\overline{RQ}$ Transition from "L" to "H" in the write operation during the reset phase must be executed after three LRCLK in the slave mode or one LRCLK in master mode, respectively, from the trailing edge of the LRCLK after release of the reset. Then the RDY goes to "H" after capturing the rise of the next LRCLK. A write operation from the microcomputer is disabled until the RDY goes to "H". The IFCON field provides external conditions written on the program. It resets to 00h by $\overline{INIT\_RESET}$ ="L", however, it remains previous condition even $\overline{S\_RESET}$ ="L".

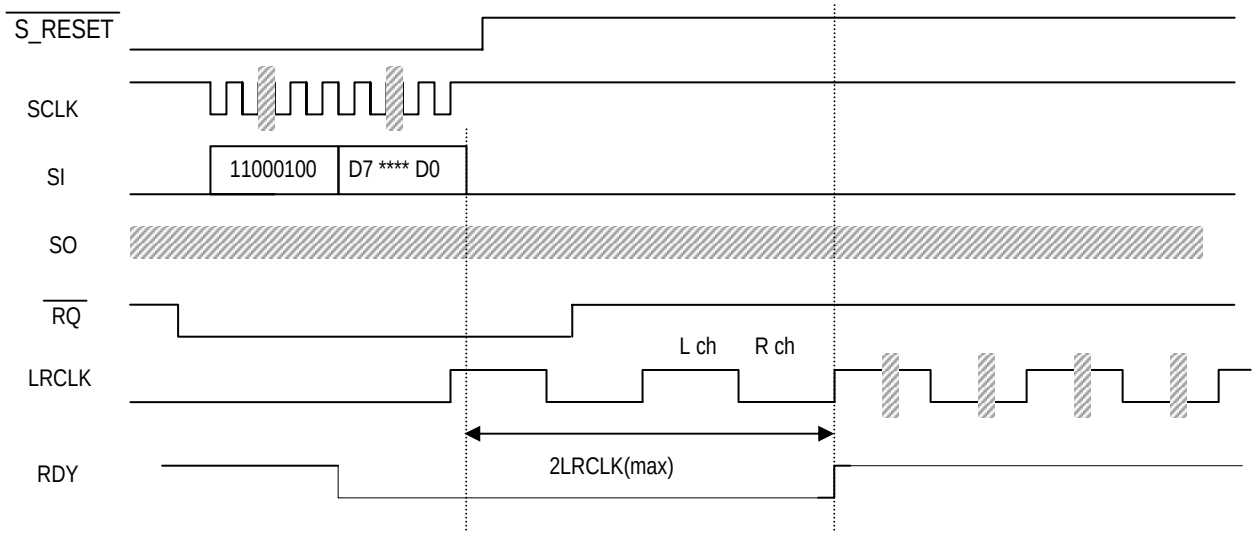
Note: It should be noted that the LRCLK phase is inverted in the I^2S-compatible state.



Check if there is any one agreement between the bit specified in IFCON and "1" in the external condition code

Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



Timing for external conditional jump write operation (during reset phase)

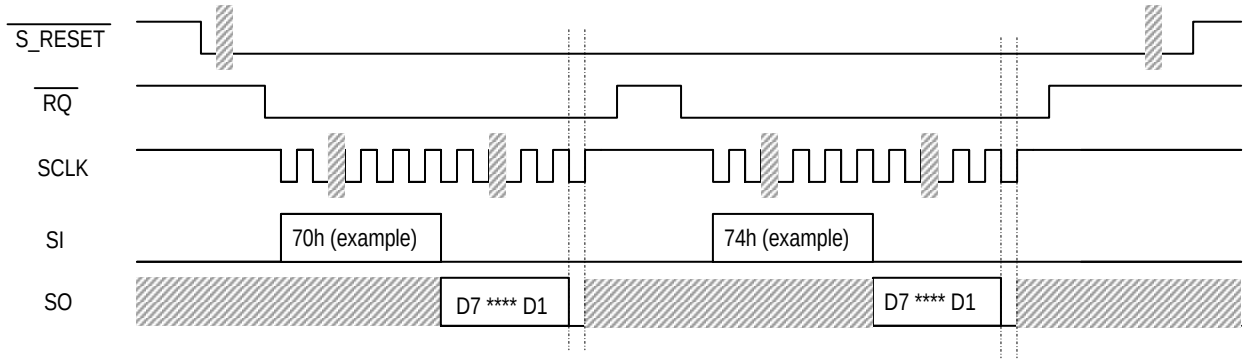
2) Read during reset phase

a) Control register data read (during reset phase)

To read data written into the control registers, input the command code and 16 bits of SCLK. After the input command code, the data of D7 to D1 outputs from SO is synchronized with the falling edge of SCLK. D0 is invalid, so please ignore this bit.

Data transfer procedure

① Command code	70h,72h,74h,76h,78h,7Ah



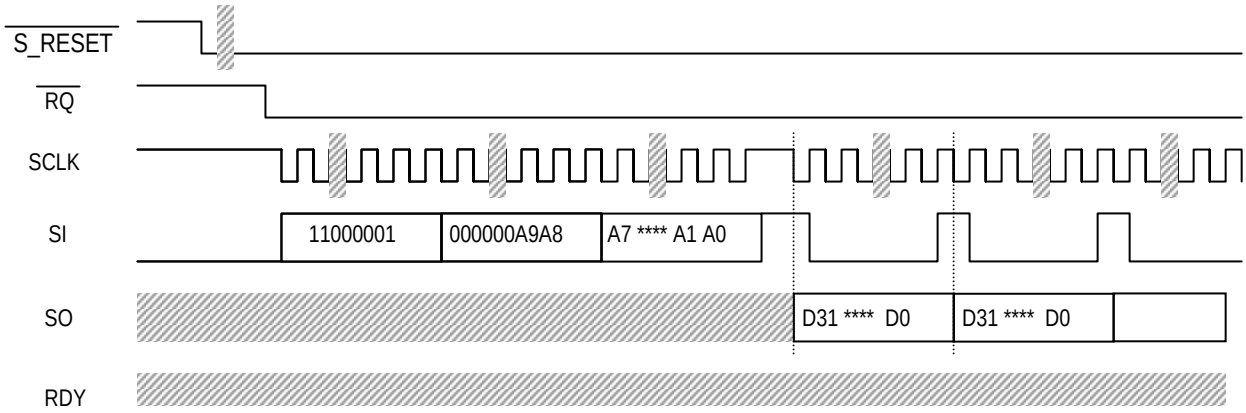
Reading of Control Register data

b) Program RAM read (during reset phase)

To read data written into PRAM, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". The data is then clocked out from SO in synchronization with the falling edge of SCLK. (Ignore the RDY operation that will occur in this case.)
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

①Command code input C1h (1 1 0 0 0 0 0 1)
②Read address input MSB (0 0 0 0 0 0 A9 A8)
③Read address input LSB (A7 . . . . A0)



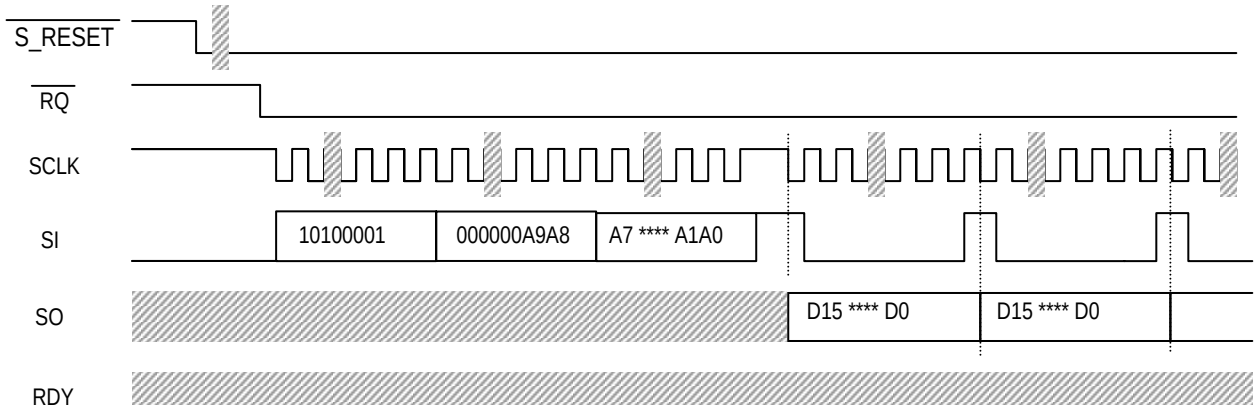
Reading of PRAM data

c) CRAM data read (during reset phase)

To read out the written coefficient data, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". The data is clocked out from SO in synchronization with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

① Command code	A1h (1 0 1 0 0 0 0 1)
② Address upper	(0 0 0 0 0 0 A9 A8)
③ Address lower	(A7 . . . . . A0)



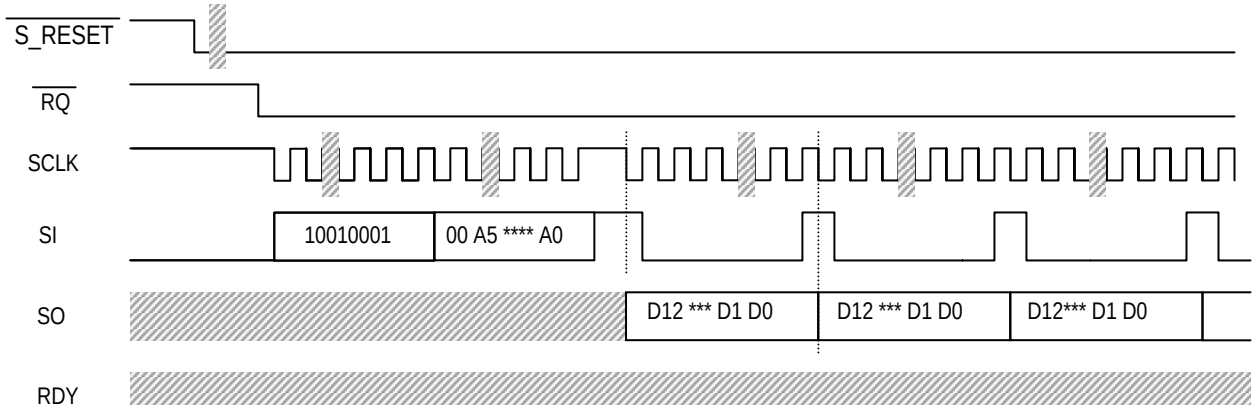
Reading of CRAM data

d) OFRAM data read (during reset phase)

The written offset data can be read out during the reset phase. To read it, input the command code and the address you want to read. After that, set SI to "H" and SCLK to "L". This completes preparation for outputting the data. Then set SI to "L", and the data is clocked out in synchronization with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to “H”.

Data transfer procedure

① Command code	91h (1 0 0 1 0 0 0 1)
② Address	(0 0 A5 . . . . A0)



Reading of OFRAM data

3) Write during RUN phase

a) CRAM rewrites preparation and writes (during RUN phase)

This function is used to rewrite CRAM (coefficient RAM) during program execution. After inputting the command code, you can input a maximum of 16 data (2 bytes 1set) of a continuous address you want to rewrite, then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

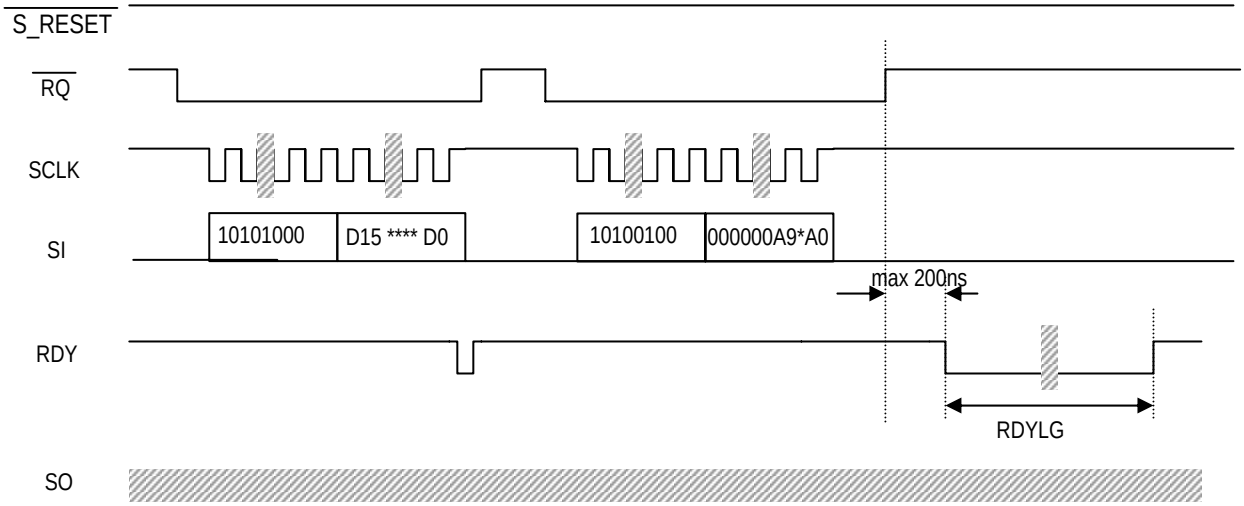
Coefficient RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ○ ○ ↑ ○ ○ ○

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	A8h	(1 0 1 0 1 0 0 0)
	② Data		(D15 . . . . D8)
	③ Data		(D7 . . . . . D0)
* Rewrite	① Command code	A4h	(1 0 1 0 0 1 0 0)
	② Address upper		(0 0 0 0 0 0 A9 A8)
	③ Address lower		(A7 . . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

CRAM rewriting preparation and writing

b) OFRAM rewrites preparation and writes (during RUN phase)

This function is used to rewrite OFRAM (offset RAM) during program execution. After inputting the command code, you can input a maximum of 16 data (3 bytes 1 set) of a continuous address you want to rewrite.
Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the offset RAM are rewritten:

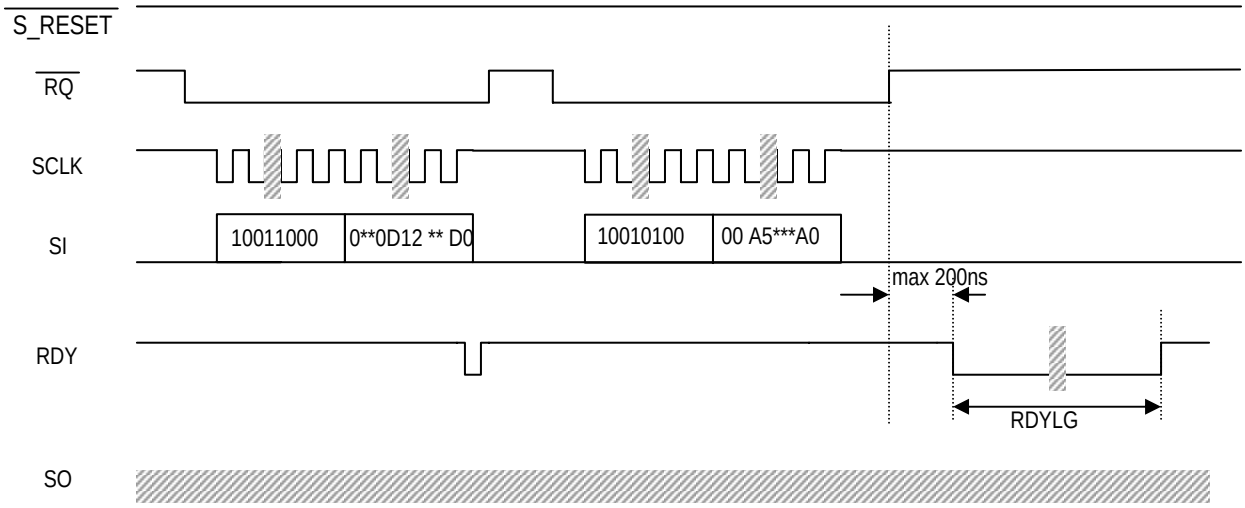
Offset RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↑ ↓ ↓ ↓

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code 98h	(1 0 0 1 1 0 0 0)
	② Data	(0 0 0 0 0 0 0 0)
	③ Data	(0 0 0 D12 . . . D8)
	④ Data	(D7 . . . . . D0)
* Rewrite	① Command code 94h	(1 0 0 1 0 1 0 0)
	② Address	(0 0 A5A4 . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

OFRAM rewriting preparation and writing

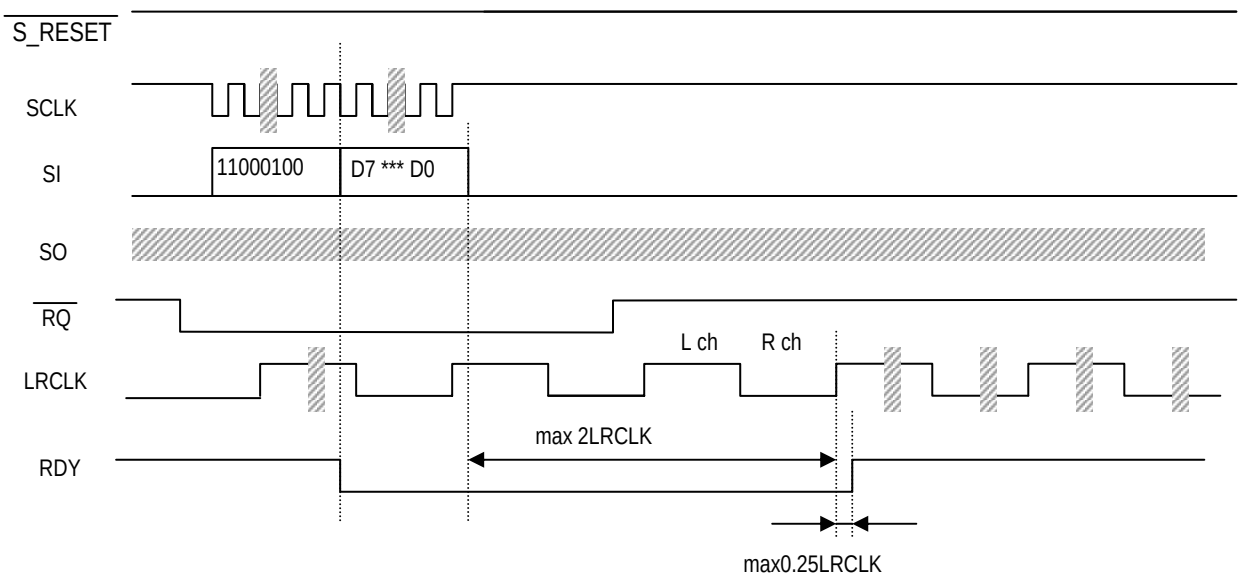
c) External conditional jump code rewrite (during RUN phase)

Two data bytes are used to write an external conditional jump code. Data can be input during both the reset and operation phases, and input data is set to the specified register at the rising edge of LRCLK. When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between each bit of the 8-bit external condition code and "1"of each bit of the IFCON field. A write operation from the microcomputer is disabled until RDY goes to "H".

Note: The LRCLK phase is inverted in the I^2S-compatible state.

Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



External condition jump write timing (during RUN phase)

4) Read-out during RUN phase (SO output)

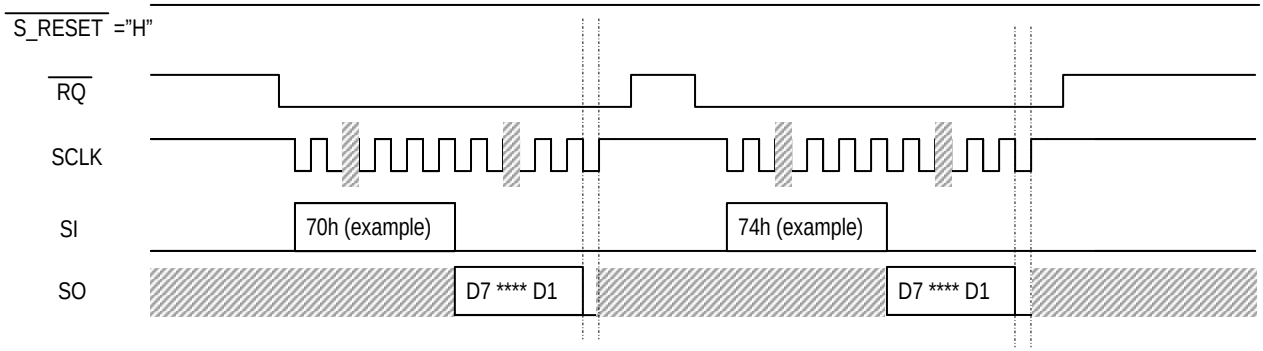
a) Control register data read (during run phase)

The control register can read during run time. To read data written into the control registers, input the command code and 16 bits of SCLK. After the input command code, the data of D7 to D1 outputs from SO is synchronized with the falling edge of SCLK. D0 is invalid, so please ignore this bit.

Data transfer procedure

① Command code 70h,72h,74h,76h,78h,7Ah

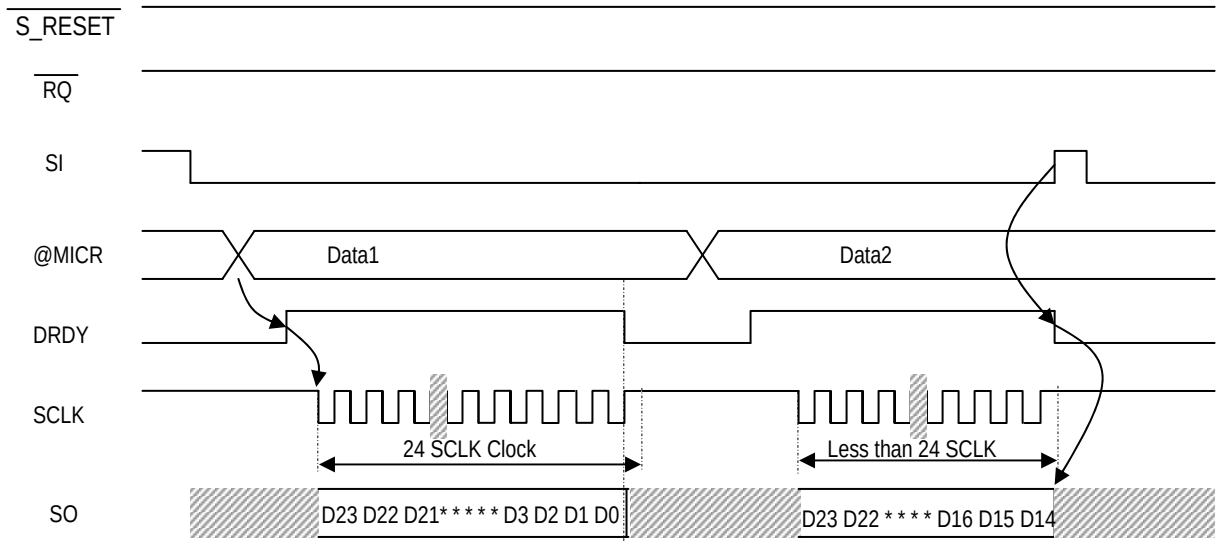
In order to know the each bit function, see 8. Function description (2) Control registers.



b) SO data read (during run phase)

SO outputs data on DBUS (data bus) of the DSP section. Data is set when @MICR the DST field specifies. Setting of data allows DRDY to go to "H", and data is output synchronized with the falling edge of SCLK. When SI goes to "H", DRDY goes to "L" to wait for the next command. Once DRDY goes to "H", the data of the last @MICR command immediately before DRDY goes to "H" will be held until SI goes to "H" or read out 24-bit data with SCLK, and subsequent commands will be rejected. A maximum of 24 bits are output from SO.

Note) In the case of read out 24-bit data, DRDY falls down when 24th SCLK rising edge and SO output bit is not stable. So, if the microcontroller cannot read out at SCLK rising edge, it should ignore the last 1bit (D0).



SO read (during RUN phase)

5) Simple error check for communication

The AK7730A has a simple CRC error check function.

(Note: Its main purpose is checking against the noise effects during writes from microprocessor to the AK7730A. **This check CANNOT guarantee 100% error detection** on the AK7730A, because this CRC (cyclic redundancy check) is before writing internal AK7730A's RAM or its register.

Explanation:

* Serial data(X): Input SI data from $\overline{RQ}$ fall to rise up.
* Generator polynomial G(x) =$x^{16}+x^{12}+x^5+1$ (X.25 of CCITT standard order of hexadecimal is 11021h).
* The rest of D(x) divides by G(x) is R(x).
  This division is using exclusive-or instead of subtraction during this calculation.
  It makes good 16-bit zero data after translated serial data D(X) and the rest R(X) of this division comes out 16bit data.

In order to do simple error check is as following:

1) Use the command code B6h and write the R(x) (the rest result of serial data D(x) divided by G(x)).
2) Then use the command code D6h and read out R(x) to check whether the R(x) is correct or not. (Unless this read out, CRC check itself works.)
3) If the result of D(x) divided by G(x) is equal to R(x), SO outputs "H" from the next rising edge of $\overline{RQ}$ to falling edge of $\overline{RQ}$. (However, SO read out from micro-controller is prior to this signal. Refrain from a runtime read out while doing CRC check.) If R(x) is not equal to the result, it outputs "L".
4) If you want to check other serial data, then repeat action form 1) to 3).

Note) In the case of detecting CRC error in runtime "CRAM rewrite" (A4h) or "OFRAM rewrite"(94h), the possibility of writing data to the wrong address exists.

* Specific order of data translates.

1) Write the register

The rest R(x) data writing is using 3-byte/unit (24bit)

Data translate order.

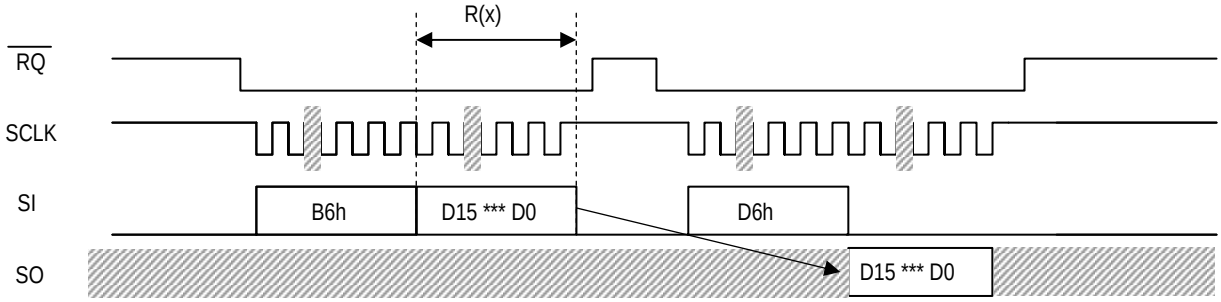
①Command code B6h
②Upper 8bit of R(x) (D15 * * * * * * D8)
③Lower 8bit of R(x) (D7 * * * * * * D0)

2) Read out the register

The rest R(x) data reading out is 3-byte/unit (24bit)

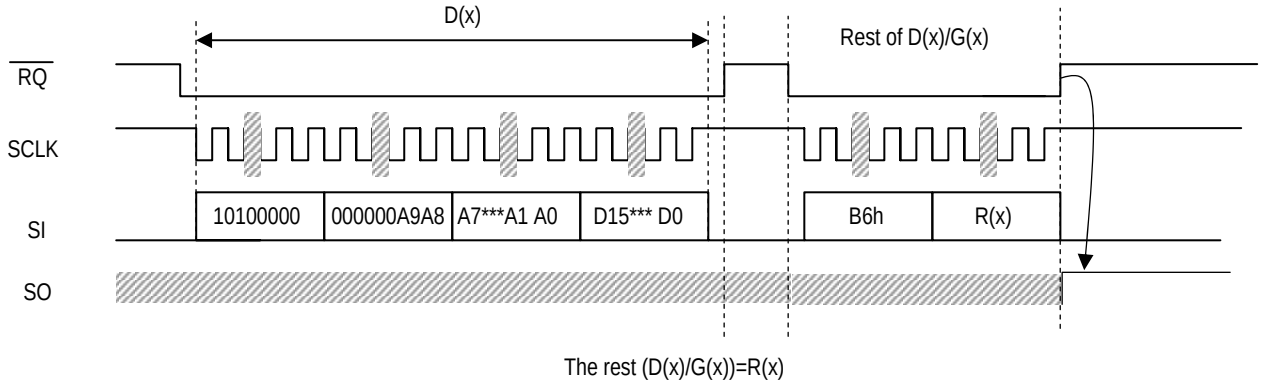
Data translate order

①Command code D6h
②Upper 8bit of R(x) (D15 * * * * * * D8)
③Lower 8bit of R(x) (D7 * * * * * * D0)



Example: Control register writing, reading

3) CRC Check



The rest of D(x)/G(x)=R(x) CRC Check example.

4) Example of the R(x) made from D(x).

Examples	D(X)	R(X)
1	D6ABCDh	1E51h
2	D2A5A5h	0C30h
3	A855557777AAAA0000FFFFh	2297h

(8) ADC high-pass filter

The AK7730A incorporates a digital high-pass filter (HPF) for canceling DC offset in the ADC. The HPF cut-off frequency is about 1 Hz (fs = 48 kHz). This cut-off frequency is proportional to the sampling frequency (fs).

	96kHz	48kHz	44.1kHz	32kHz	8kHz
Cut-off frequency	1.86Hz	0.93Hz	0.86Hz	0.62Hz	0.16Hz

(9) Interface for the EEPROM

1) How to use

AK7730A has an interface for the EEPROM. After release of initial reset, it can load the data of PRAM, CRAM, OFRAM and its control register setting value automatically. This function can save the memory area of microcomputer.
The proper EEPROM is the AKM AK6510C or AK6512C.
In case of using this function, it should write a data as 2) Program Map of EEPROM.

How to use this function is as following ;
At first set the EESEL to “H”, (after crystal oscillator start, in case of using crystal), then $\overline{\text{INIT\_RESET}}$ pin sets to “H”.

By this action, the internal counter starts to work and the AK7730A generate the control signal $\overline{\text{EECS}}$, EESK and EESI for EEPROM. Then the AK7730A is loaded the data from EESO pin of the EEPROM. When it finishes all data reading, then EESK and EESI change to ”L” and $\overline{\text{EECS}}$ changes to “H”. EEST pin changes from “L” to “H” to signify the finish of loading. After EEST changes from “L” to “H”, the microcomputer interface pins are able to use even if EESEL pin leaving “H”.

In case of RELOAD again, leave EEST “H” and control the initial reset pin, (After sets $\overline{\text{INIT\_RESET}}$ =”L” then sets $\overline{\text{INIT\_RESET}}$ =”H” again.)

In case of using the AK6512C, it can set another program for writing in 1000h of EEPROM address. The EEADR pin can use for this selection.

For error check, it can write R(x) (16bit) on CRCDATA of the program map address 0000h to 0FFBh. By writing this data it can check the error of data transfer from EEPROM to AK7730A. After loading (EEST = “H”), SO pin output “H” if CRC data is correct otherwise SO outputs “L”. So, SO output “L” means data loading is not correct.
(Generator polynomial $G(x) = x^{16}+x^{12}+x^5+1$ (X.25 of CCITT standard order of hexadecimal is 11021h).The rest of D(x) divides by G(x) is R(x). See page 52)

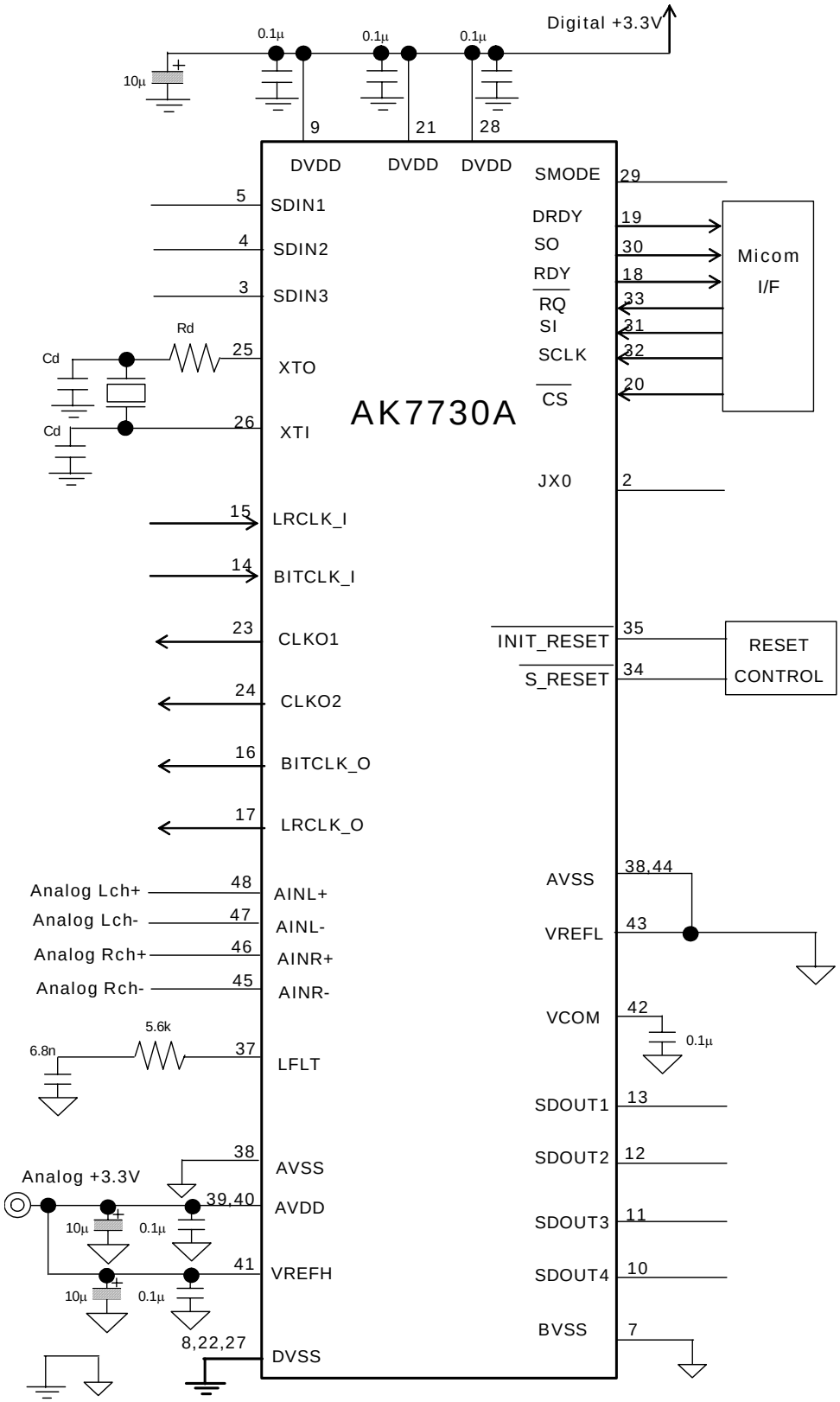
When the AK7730A power up and initial reset is released in EESEL=”H” and $\overline{\text{S\_RESET}}$ =”H” condition, during EEPROM download, internal system reset is active and after loading all data, then system reset releases automatically. This function makes it possible to self boot up without microcomputer.

2) Program map for EEPROM

EEPROMADDRESS	DATA	Note
0000h	C0h	PRAM WRITE Command code
0001h	00h	PRAM address MSB side
0002h	00h	PRAM address LSB side
0003h	PRAM0 DATA31-24	PRAM address 0 MSB 8bit data
0004h	PRAM0 DATA23-16	PRAM address 0 MSB-1 8bit data
0005h	PRAM0 DATA15-8	PRAM address 0 MSB-2 8bit data
0006h	PRAM0 DATA7-0	PRAM address 0 LSB 8bit data
0007h	PRAM1 DATA31-24	PRAM address 1 MSB 8bit data
…….	……..	……
0BFEh	PRAM766 DATA7-0	PRAM address 766 LSB 8bit data
0BFFh	PRAM767 DATA31-24	PRAM address 767 MSB 8bit data
0C00h	PRAM767 DATA23-16	PRAM address 767 MSB-1 8bit data
0C01h	PRAM767 DATA15-8	PRAM address 767 MSB-2 8bit data
0C02h	PRAM767 DATA7-0	PRAM address 767 LSB 8bit data
0C03h	A0h	CRAM WRITE command code
0C04h	00h	CRAM address MSB side
0C05h	00h	CRAM address LSB side
0C06h	CRAM0 DATA15-8	CRAM address 0 MSB 8bit data
0C07h	CRAM0 DATA7-0	CRAM address 0 LSB 8bit data
0C08h	CRAM1 DATA15-8	CRAM address 1 MSB 8bit data
……..	…….	…….
0F59h	CRAM425 DATA7-0	CRAM address 425 LSB 8bit data
0F5Ah	CRAM426 DATA15-8	CRAM address 426 MSB 8bit data
0F5Bh	CRAM426 DATA7-0	CRAM address 426 LSB 8bit data
0F5Ch	90h	OFRAM WRITE command code
0F5Dh	00h	OFRAM address
0F5Eh	OFRAM0 DATA23-16	OFRAM address 0 MSB 8bit data
0F5Fh	OFRAM0 DATA15-8	OFRAM address 0 MSB-1 8bit data
0F60h	OFRAM0 DATA7-0	OFRAM address 0 LSB 8bit data
0F61h	OFRAM1 DATA23-16	OFRAM address 1 MSB 8bit data
……	……..	
0FEAh	OFRAM46 DATA7-0	OFRAM address 46 LSB 8bit data
0FEBh	OFRAM47 DATA23-16	OFRAM address 47 MSB 8bit data
0FECh	OFRAM47 DATA15-8	OFRAM address 47 MSB-1 8bit data
0FEDh	OFRAM47 DATA7-0	OFRAM address 47 LSB 8bit data
0FEEh	60h	CONT0 WRITE command code
0FEFh	DATA	CONT0 data
0FF0h	62h	CONT1 WRITE command code
0FF1h	DATA	CONT1 data
0FF2h	64h	CONT2 WRITE command code
0FF3h	DATA	CONT2 data
0FF4h	66h	CONT3 WRITE command code
0FF5h	DATA	CONT3 data
0FF6h	68h	CONT4 WRITE command code
0FF7h	DATA	CONT4 data
0FF8h	6Ah	CONT5 WRITE command code
0FF9h	DATA	CONT5 data
0FFAh	00h	Reserve
0FFBh	00h	Reserve
0FFCh	B6h	CRC WRITE command code
0FFDh	CRC DATA15-8	CRC MSB 8bit data
0FFEh	CRC DATA7-0	CRC LSB 8bit data
0FFFh	00h	Reserve

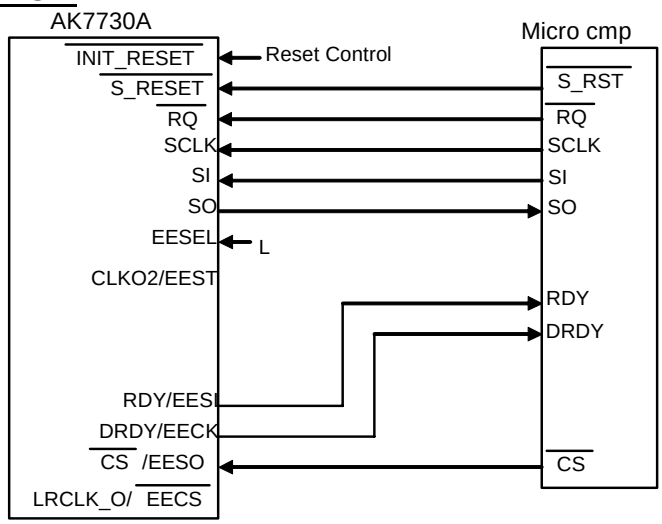
9. System Design

(1) Connection example

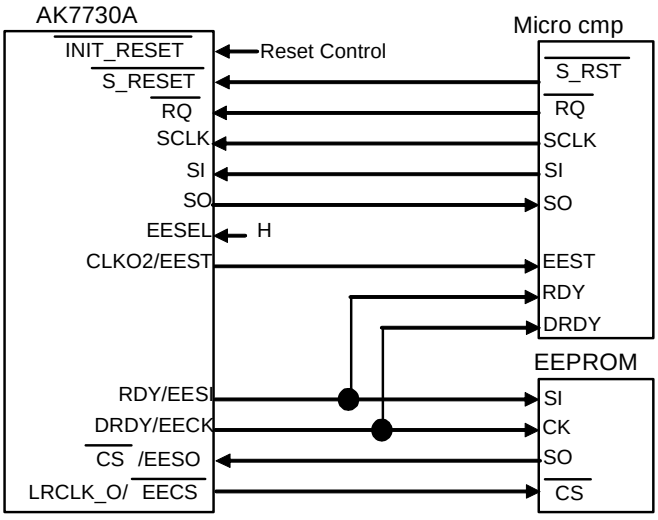


(2) Peripheral circuit

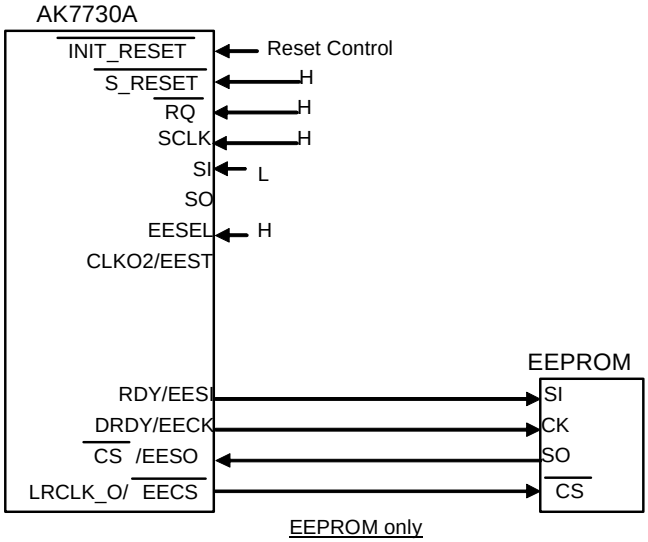
1) Connect with EEPROM



4line control



4line control + EEPROM



EEPROM only

2) Ground and power supply

To minimize digital noise coupling, AVDD and DVDD should be individually de-coupled at the AK7730A. System analog power is supplied to AVDD.

Generally, power supply and ground wires must be connected separately according to the analog and digital systems. Connect them at a position close to the power source on the PCB board. Decoupling capacitors and ceramic capacitors of small capacity in particular, should be connected at positions as close as possible to the AK7730A.

3) Reference voltage

The input voltage difference between the VREFH pin and the AVSS pin determines the full scale of analog input. Normally, connect AVDD to VREFH, and connect 0.1μF ceramic capacitors from them to AVSS. To shut out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor in particular should be connected as close as possible to the pin. To avoid coupling to the AK7730A, digital signals and clock signals should be kept away as far as possible from the VREFH pin.

VCOM is used as the common voltage of the analog signal.To shut out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor should be connected as close as possible to the pin. Do not draw current from the VCOM pin.

4) Analog input

Analog input signals are applied to the modulator through the differential input pins of each channel. The input voltage is equal to the differential voltage between AIN+ and AIN- (ΔVAIN = (AIN+) - (AIN-)), and the input range is ±FS = ±(VRADH - VRADL) × 0.4. When VRADH = 3.3V and VRADL = 0V, the input range is within ±1.32V. The output code format is given in terms of 2's complements.

When fs = 48 kHz, the AK7730A samples the analog input at 3.072 MHz. The digital filter eliminates noise from 30 kHz to 3.042 MHz. However, noise is not rejected in the bandwidth close to 3.072 MHz. Most audio signals do not have large noise in the vicinity of 3.072 MHz, so a simple RC filter is sufficient.

The analog source voltage to the AK7730A is +3.3V(Typ.). Voltage of AVDD + 0.3 V or more, voltage of AVSS - 0.3 V or less, and current of 10 mA or more must not be applied to analog input pins (AINL and AINR). Excessive current will damage the internal protection circuit and will cause latch-up, thereby damaging the IC. Accordingly, if the surrounding analog circuit voltage is ±15 V, the analog input pins must be protected from signals with the absolute maximum rating or more.

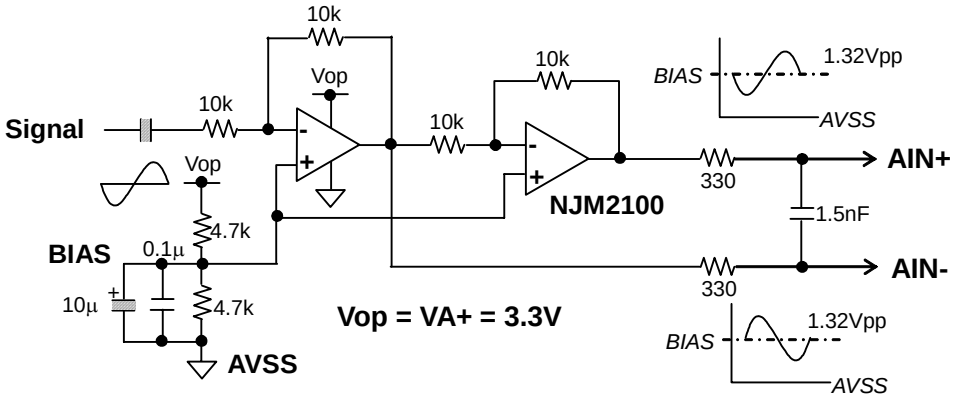


Fig. 1 Example of input buffer circuit (differential input)

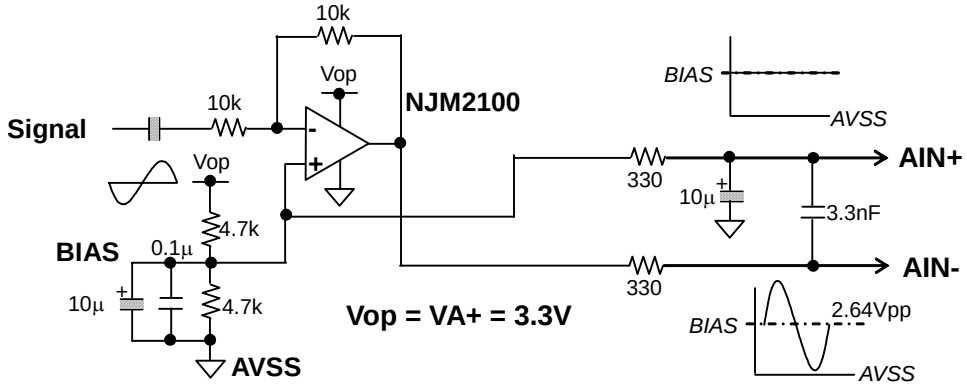


Fig. 2 Example of input buffer circuit (single ended input)

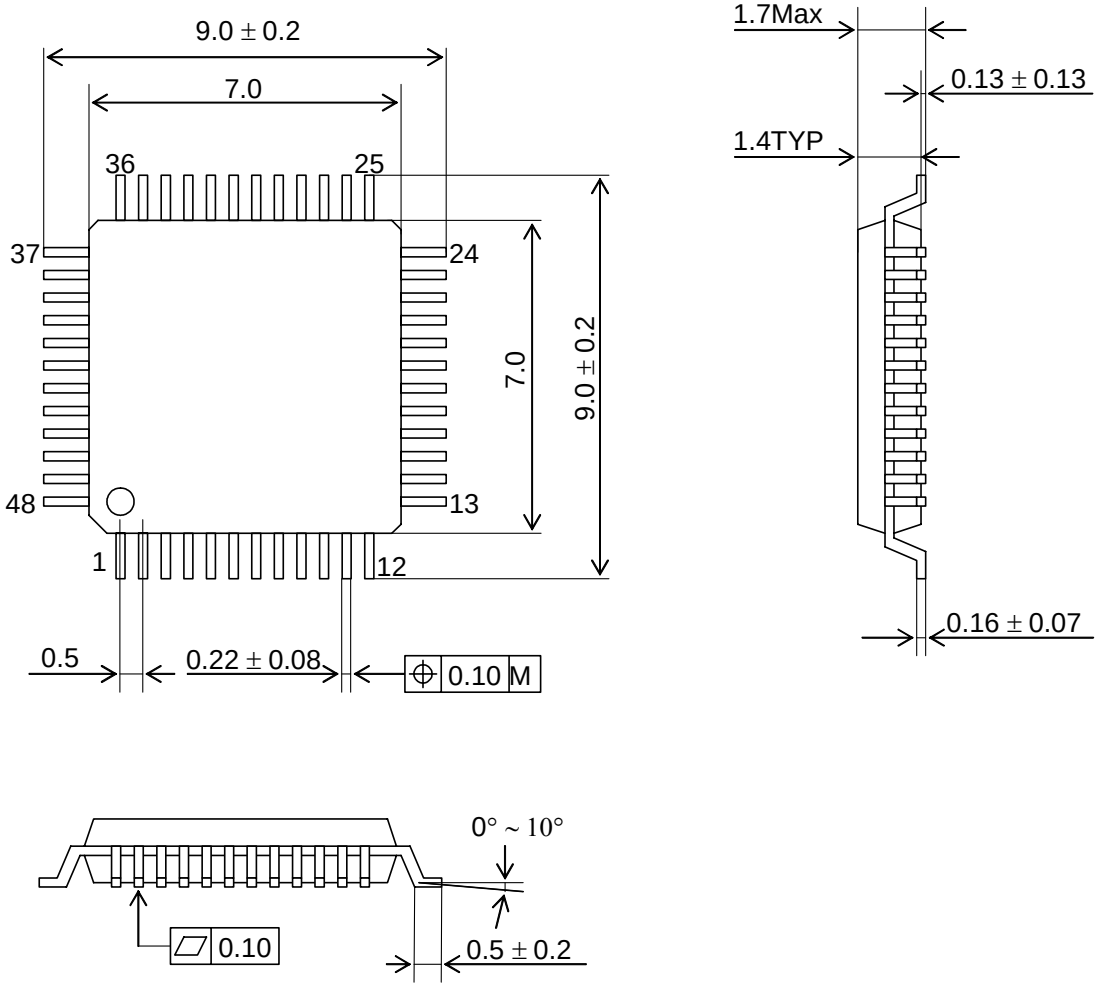
An analog signal can be applied to the AK7730A is single ended mode. In this case, apply the analog signal (the full scale is 2.64Vpp when the internal reference voltage is used) to the AIN-input, and bias to the AIN+input. However, use of a low saturated operational amplifier is recommended if the operational amplifier is driven by the 3.3-volt power supply. The electrolytic capacitor connected to AIN+ is effective for reducing the second harmonics.
(See Fig. 2.)

5) Connection to digital circuit

To minimize the noise resulting from the digital circuit, connect low voltage logic to the digital output. The applicable logic family includes the 74LV, 74LV-A, 74ALVC and 74AVC series.

10. Package

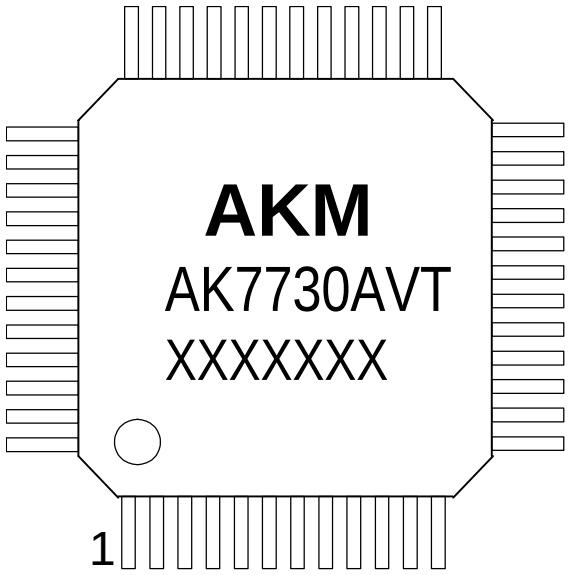
48pin LQFP(Unit:mm)



- Material & Lead finish

  Package: Epoxy
  Lead-frame: Copper
  Lead-finish: Soldering plate

11. Marking



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK7730AVT
4) Asahi Kasei Logo