TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (Ultra-High-Speed U-MOSIII)

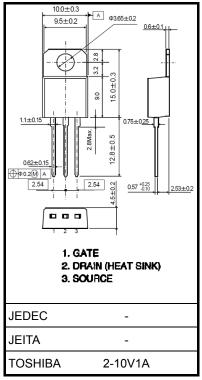
TK70D06J1

Switching Regulator Application

- High-Speed switching
- Small gate charge: Q_g = 87 nC (typ.)
- Low drain-source ON resistance: $R_{DS (ON)}$ = 5.1 m Ω (typ.)
- High forward transfer admittance: $|Y_{fs}| = 80 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = 10 \ \mu A \ (max) \ (V_{DS} = 60 \ V)$
- Enhancement-mode: V_{th} = 1.1 to 2.3 V (V_{DS} = 10 V, I_D = 1 mA)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V _{DSS}	60	V
Drain-gate voltage (F	R _{GS} = 20 kΩ)	V _{DGR}	60	V
Gate-source voltage		V _{GSS}	±20	V
Drain current	DC (Note 1) I _D	70	А
	Pulse (Note 1) I _{DP}	280	A
Drain power dissipat	ion (Tc = 25°C)	PD	140	W
Single pulse avalance	he energy (Note 2) E _{AS}	751	mJ
Avalanche current		I _{AR}	70	А
Repetitive avalanche	energy (Note 3) E _{AR}	10.3	mJ
Channel temperature	9	T _{ch}	150	°C
Storage temperature	range	T _{stg}	-55~150	°C



Weight: 1.35 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R _{th (ch-c)}	0.89	°C/W
Thermal resistance, channel to ambient	R _{th (ch-a)}	83.3	°C/W

Internal Connection



Note 1: Ensure that the channel & lead temperature does not exceed 150°C.

Note 2: V_{DD} = 25 V, T_{ch} = 25^{\circ}C, L = 200 \ \mu\text{H}, I_{AR} = 70 \text{ A}, R_{G} = 1 \ \Omega

Note 3: Repetitive rating: pulse width limited by maximum channel temperature.

This transistor is an electrostatic-sensitive device. Handle with care.

Unit: mm

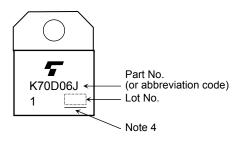
Electrical Characteristics (Ta = 25°C)

Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{GS}=\pm 16~V,~V_{DS}=0~V$			±10	μA
Drain cut-OFF current		I _{DSS}	$V_{DS}=60~V,~V_{GS}=0~V$	_		10	μA
Drain-source breakdown voltage		V (BR) DSS	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	60		_	v
		V (BR) DSX	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	45	_	_	
Gate threshold voltage		V _{th}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1 \text{ mA}$	1.1		2.3	V
Drain-source ON resistance		R _{DS (ON)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 35 \text{A}$		5.8	7.6	mΩ
			$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 35 \text{ A}$	_	5.1	6.4	
Forward transfer	admittance	Y _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 35 \text{ A}$	40	80	_	S
Input capacitance		C _{iss}		_	5450	_	
Reverse transfer capacitance		C _{rss}	$V_{DS} = 10V, V_{GS} = 0 V, f = 1 MHz$		320	_	pF
Output capacitance		C _{oss}			1420		
Switching time	Rise time	tr	$V_{GS}^{10 V}$ $V_{GS}^{0 V}$ $V_{GS}^{0 V}$ $V_{DD}^{0 V}$ $V_{DD}^{0 V}$ $V_{DD}^{0 V}$ $V_{DD}^{0 V}$ $V_{DD}^{0 V}$ $V_{DU}^{0 V}$ $V_{DU}^{0 V}$	_	9	_	ns
	Turn-ON time	t _{on}			24		
	Fall time	t _f			21		
	Turn-OFF time	t _{off}		—	106	_	
Total gate charge (gate-source plus gate-drain)		Qg	$V_{DD}\simeq 48~V,~V_{GS}=5~V,~I_D=70A$		47		
			$V_{DD}\simeq 48~V,~V_{GS}=10~V,~I_D=70A$	_	87		
Gate-source charge 1		Q _{gs1}			16		nC
Gate-drain ("miller") charge		Q _{gd}	$V_{DD}\simeq 48~V,~V_{GS}=10~V,~I_D=70A$	_	19	_	
Gate switch charge		Q _{sw}		_	30	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	—		_	70	А
Pulse drain reverse current (Note 1)	I _{DRP}	—	_	_	280	А
Forward voltage (diode)	V _{DSF}	$I_{DR} = 70 \text{ A}, V_{GS} = 0 \text{ V}$	_	-1.0	-1.2	V
Reverse recovery time	t _{rr}	$I_{DR} = 70 \text{ A}, V_{GS} = 0 \text{ V},$	_	60	_	ns
Reverse recovery charge	Q _{rr}	dI _{DR} /dt = 50 A/µs		51	_	nC

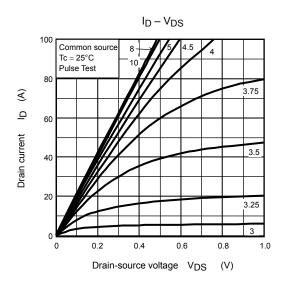
Marking

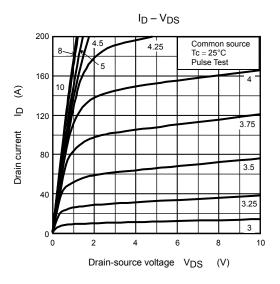


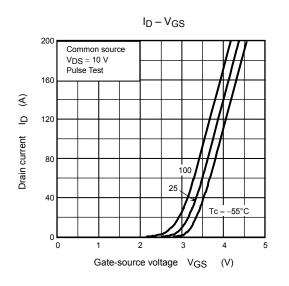
Note 4: A line under a Lot No. identifies the indication of product Labels. Not underlined: [[Pb]]/INCLUDES > MCV Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

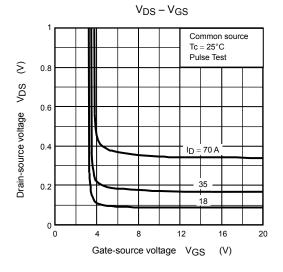
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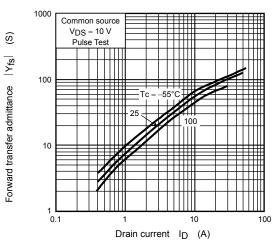




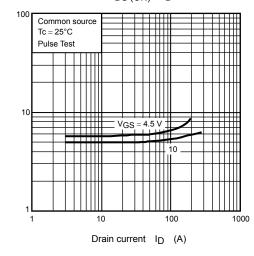








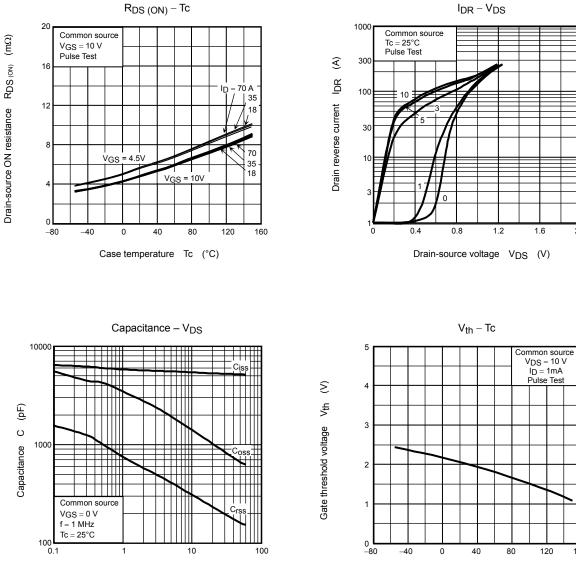
 $R_{DS(ON)} - I_D$

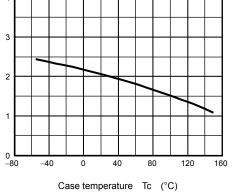


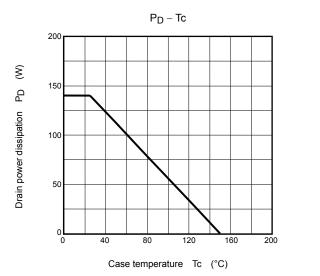
(MQ)

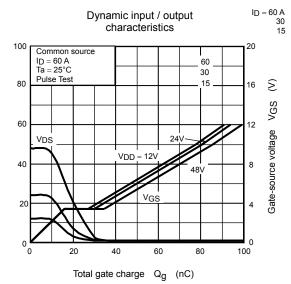
Drain-source ON resistance RDS (ON)

2.0



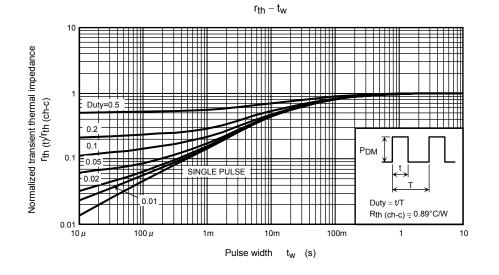




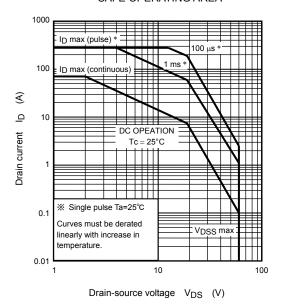


S

Drain-source voltage VDS



SAFE OPERATING AREA



 $\mathsf{E}_{AS}-\mathsf{T}_{ch}$ 1000 (ſш) 800 EAS 600 Avalanche energy 400 200 0 50 100 125 150 75 25 Channel temperature (initial) T_{ch} (°C) **B**_{VDSS} 20 V –5 V IAR VDD VDS Test circuit Waveform

 $\begin{array}{l} \mathsf{R}_{G} = 1 \; \Omega \\ \mathsf{V}_{DD} = 25 \; \mathsf{V}, \; \mathsf{L} = 200 \; \mu \mathsf{H} \end{array} \qquad \mathsf{E}_{AS} = \frac{1}{2} \cdot \mathsf{L} \cdot \mathsf{I}^{2} \cdot \left(\frac{\mathsf{B}_{VDSS}}{\mathsf{B}_{VDSS} - \mathsf{V}_{DD}} \right)$

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