

Linear Systems replaces discontinued Siliconix 2N4117A

The LS4117A is an Ultra-High Input Impedance N-Channel JFET

The LS4117A provides ultra-high input impedance. The device is specified with a 1-pA limit and typically operates at 0.2 pA. The part is ideal for use as a high-impedance sensitive front-end amplifier.

LS4117A Benefits:

- Insignificant Signal Loss / Error Voltage with High-Impedance Source
- Low Power Consumption (Battery)
- Maximum Signal Output, Low Noise
- High Sensitivity to Low-Level Signals

LS4117A Applications:

- High-Impedance Transducer
- Smoke Detector Input
- Infrared Detector Amplifier
- Precision Test Equipment

FEATURES

DIRECT REPLACEMENT FOR SILICONIX 2N4117A

LOW POWER

$I_{DSS} < 90 \mu A$

MINIMUM CIRCUIT LOADING

$I_{GSS} < 1 pA$

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature

-65°C to +175°C

Operating Junction Temperature

-55°C to +150°C

Maximum Power Dissipation

Continuous Power Dissipation

300mW

MAXIMUM CURRENT

Gate Current (Note 1)

50mA

MAXIMUM VOLTAGES

Gate to Drain or Gate to Source (Note 2)

-40V

LS4117A ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP.	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-40	--	--	V	$I_G = -1 \mu A, V_{DS} = 0V$
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.6	--	-1.8	V	$V_{DS} = 10V, I_D = 1nA$
I_{DSS}	Gate to Source Saturation Current	0.03	--	0.09	mA	$V_{DS} = 10V, V_{GS} = 0V$
I_{GSS}	Gate Leakage Current	--	--	-1	pA	$V_{GS} = -20V, V_{DS} = 0V$
		--	--	-2.5		$V_{GS} = -20V, V_{DS} = 0V, 150^\circ C$
g_{fs}	Forward Transconductance (Note 3)	70	--	210	μmho	$V_{DS} = 10V, V_{GS} = 0V, f = 1kHz$
g_{os}	Output Conductance	--	--	3		
C_{iss}	Input Capacitance	--	--	3		
C_{rss}	Reverse Transfer Capacitance	--	--	1.5	pF	$V_{DS} = 10V, V_{GS} = 0V, f = 1MHz$

NOTES

1. Absolute maximum ratings are limiting values above which LS4117A serviceability may be impaired.
2. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged
3. This parameter is measured during a 2ms interval 100ms after power is applied. (Not a JEDEC condition.)

Micross Components Europe

Available Packages:

TO-71 (Bottom View)



LS4117A in TO-71
LS4117A in bare die.

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Please contact Micross for full package and die dimensions

