ALPHA & OMEGA SEMICONDUCTOR

AO4478
30V N-Channel MOSFET

General Description

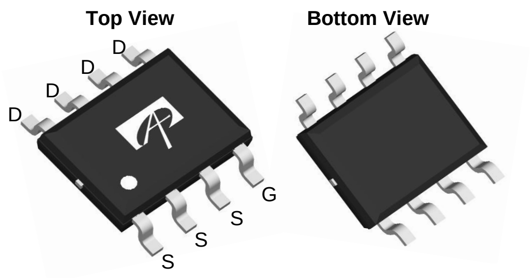
The AO4478 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device is suitable for use as general puspose, PWM and a load switch applications.

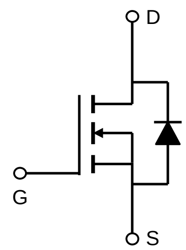
Product Summary

V_{DS} (V) = 30V
I_D = 9A (V_{GS} = 10V)
$R_{DS(ON)}$ <19mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ <26mΩ (V_{GS} = 4.5V)

100% UIS Tested
100% Rg Tested

SOIC-8





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_A=25°C	I_D	9.0	A
	T_A=70°C		7.0	
Pulsed Drain Current [C]		I_{DM}	60	
Avalanche Current [C]		Iar	17	
Repetitive avalanche energy L=0.1mH [C]		Ear	14	mJ
Power Dissipation [B]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2.0	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient [AD]	Steady-State		59	75	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	16	24	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	uA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±25V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	1.6	2	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	60			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=9A		16	19	mΩ
		T_J=125°C		25	30	
		V_{GS}=4.5V, I_D=8A		21	26	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=10A		24		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.70	1	V
I_S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		466	560	pF
C_{oss}	Output Capacitance			90		pF
C_{rss}	Reverse Transfer Capacitance			61		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		3.7	5.6	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=9A		9.3	11	nC
Q_g(4.5V)	Total Gate Charge			4.3	5.2	nC
Q_{gs}	Gate Source Charge			1		nC
Q_{gd}	Gate Drain Charge			2.3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.65Ω, R_{GEN}=3Ω		5		ns
t_r	Turn-On Rise Time			8		ns
$t_{D(off)}$	Turn-Off DelayTime			20		ns
t_f	Turn-Off Fall Time			5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=9A, dI/dt=500A/µs		7.5	9	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=9A, dI/dt=500A/µs		9.8		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.
C. Ratings are based on low frequency and duty cycles to keep initialT_J=25°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse ratin g.

Rev1: Nov. 2010

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

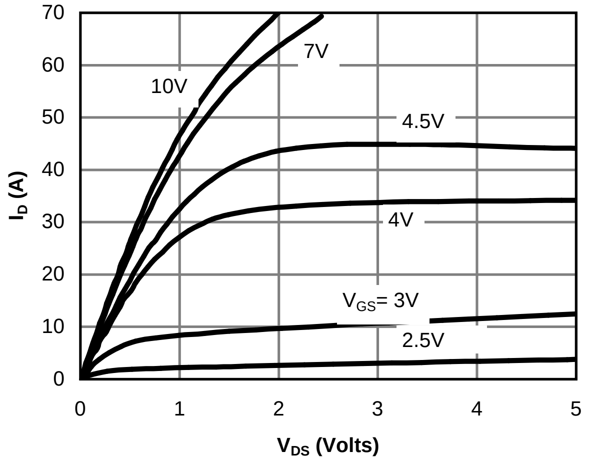


Figure 1: On-Region Characteristics(Note E)

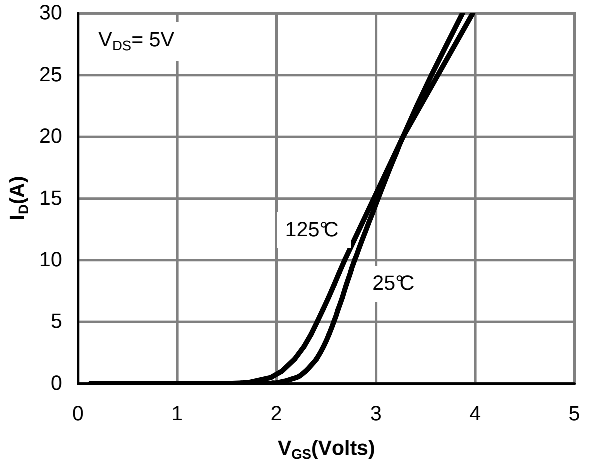


Figure 2: Transfer Characteristics(Note E)

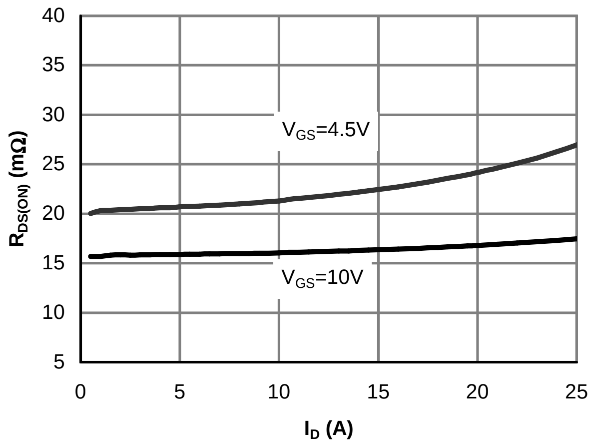


Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

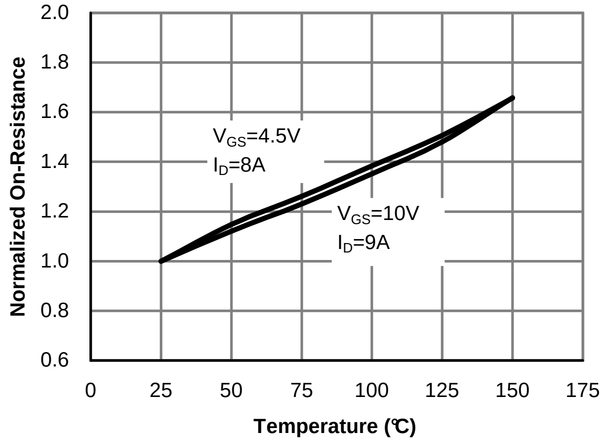


Figure 4: On-Resistance vs. Junction Temperature(Note E)

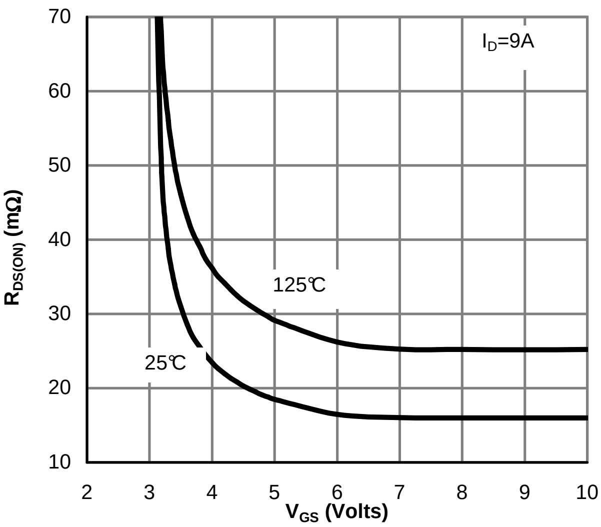


Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)

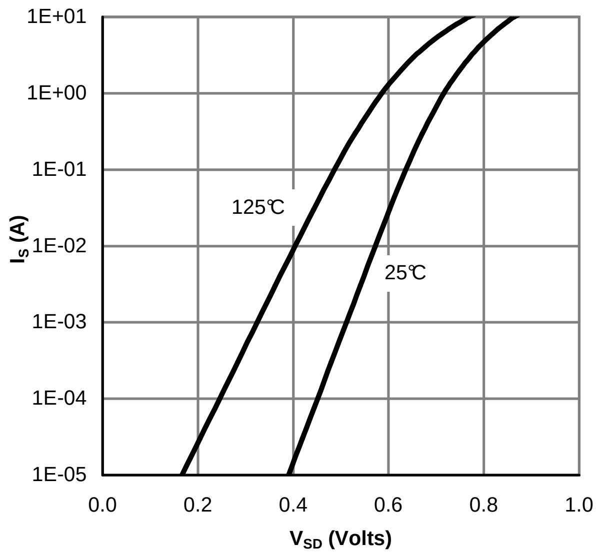


Figure 6: Body-Diode Characteristics(Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

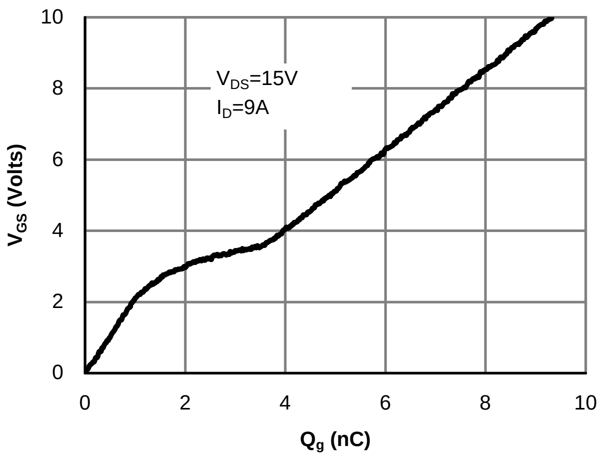


Figure 7: Gate-Charge Characteristics

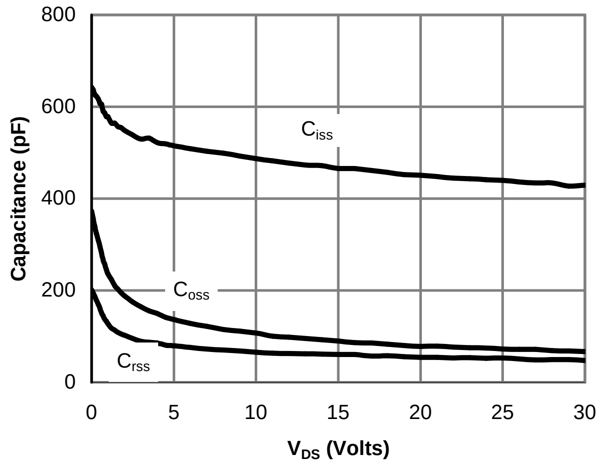


Figure 8: Capacitance Characteristics

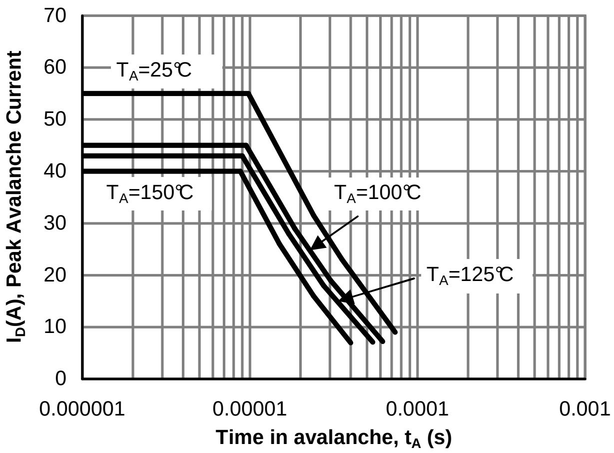


Figure 9: Single Pulse Avalanche capability (Note C)

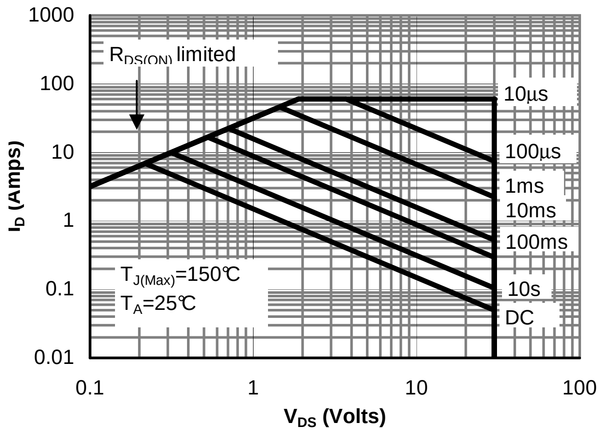


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

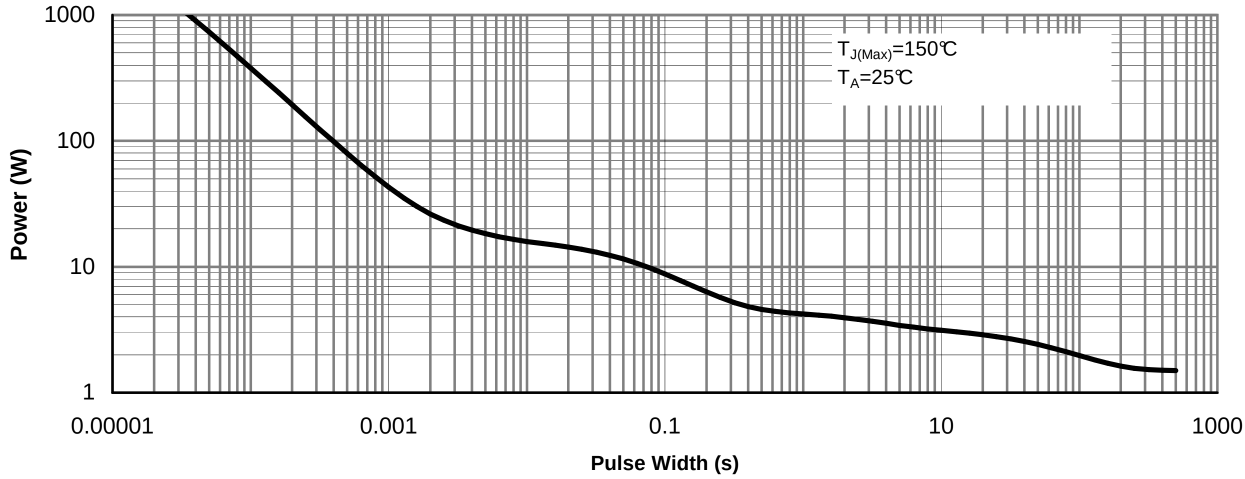


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

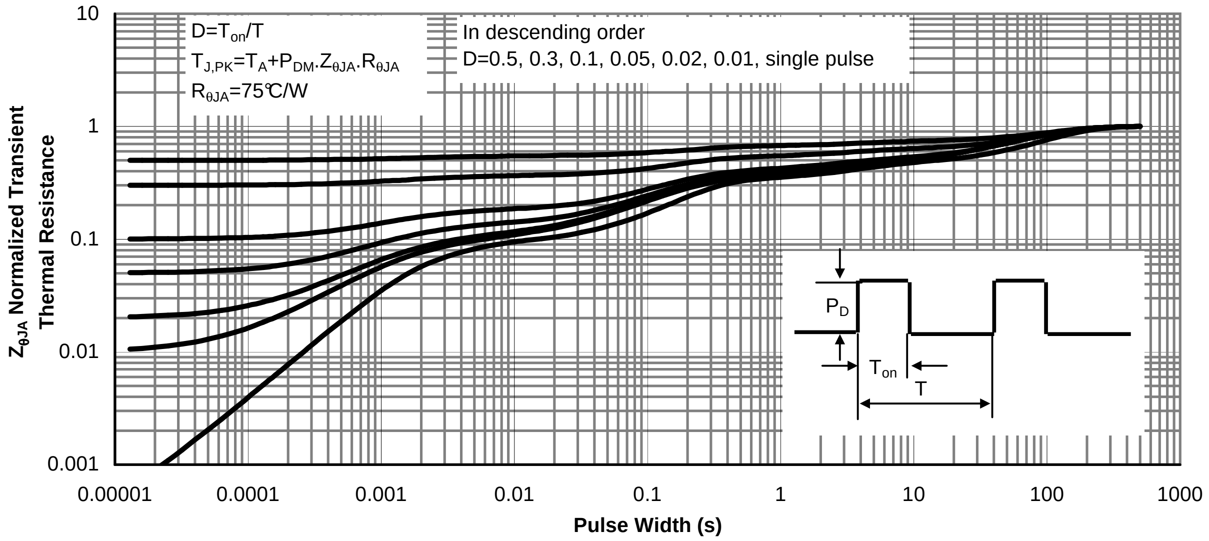
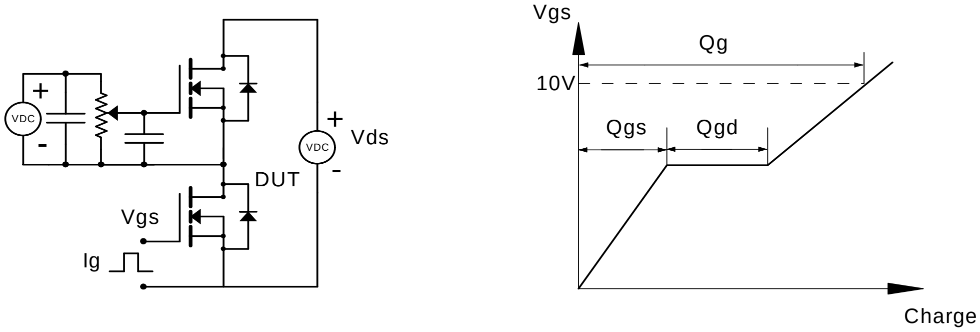
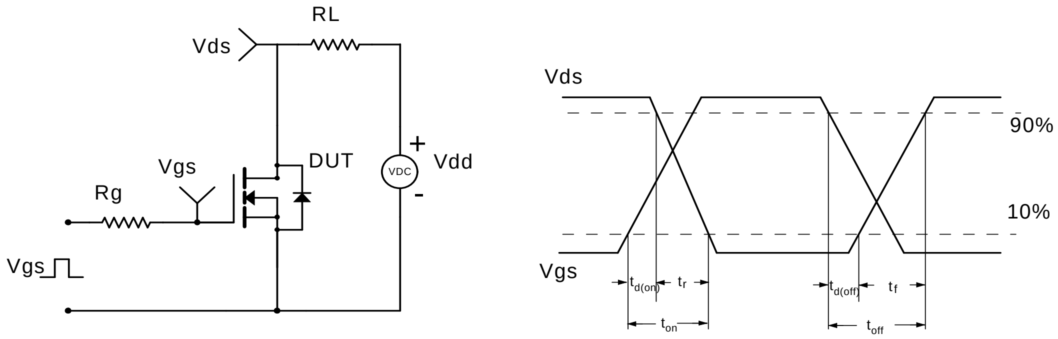


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

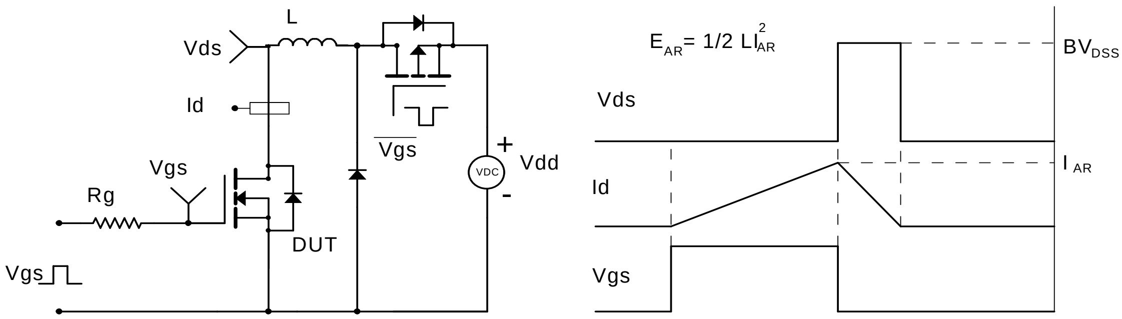
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms