SONY

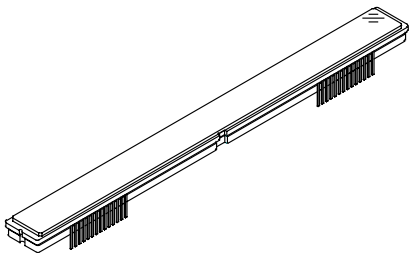
ILX734LA

10500 × 3 pixel CCD Linear Sensor (Color)

Description

The ILX734LA is a reduction type CCD linear sensor developped for color image scanner, and has shutter function per each color. This sensor reads A4-size documents at a density of 1200 DPI.

56 pin SDIP (Cer-DIP)



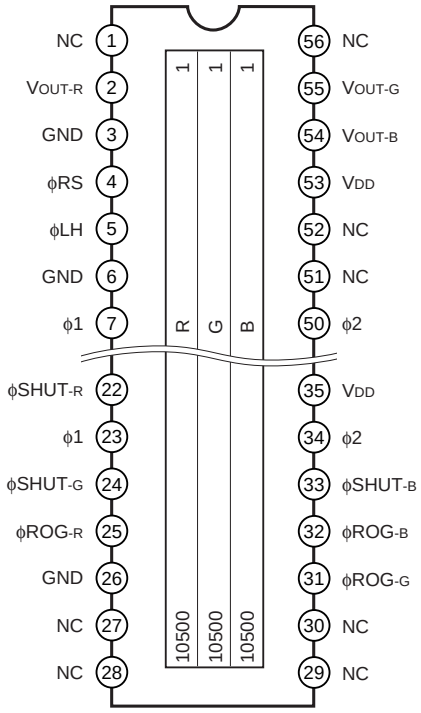
Features

- Number of effective pixels: 31500 pixels (10500 pixels × 3)
- Pixel size: 8µm × 8µm (8µm pitch)
- Distance between line: 64µm (8 lines)
- Single-sided readout
- Shutter function
- Ultra low lag/High sensitivity
- Single 12V power supply
- Input Clock Pulse: CMOS 5V drive
- Number of output 3 (R, G, B)
- Package: 56 pin SDIP (400 mil)

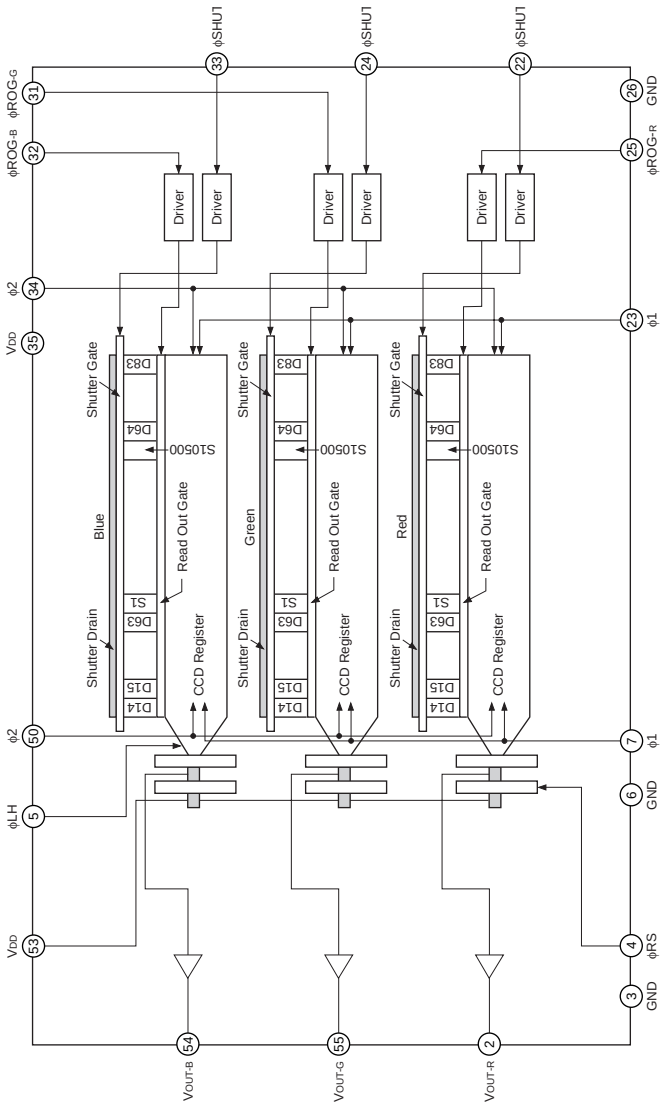
Absolute Maximum Ratings

• Supply voltage	V_{DD}	15	V
• Operating temperature		–10 to +55	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



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E99216-PS

Pin Description (Pins other than below are defined as NC.)

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC	NC	31	φROG-G	Clock pulse input
2	VOUT-R	Signal out (red)	32	φROG-B	Clock pulse input
3	GND	GND	33	φSHUT-B	Clock pulse input
4	φRS	Clock pulse input	34	φ2	Clock pulse input
5	φLH	Clock pulse input	35	VDD	12V power supply
6	GND	GND	50	φ2	Clock pulse input
7	φ1	Clock pulse input	51	NC	NC
22	φSHUT-R	Clock pulse input	52	NC	NC
23	φ1	Clock pulse input	53	VDD	12V power supply
24	φSHUT-G	Clock pulse input	54	VOUT-B	Signal out (blue)
25	φROG-R	Clock pulse input	55	VOUT-G	Signal out (green)
26	GND	GND	56	NC	NC

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
VDD	11.4	12	12.6	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of φ1, φ2	Cφ1, Cφ2	—	1600	—	pF
Input capacity of φLH	CφLH	—	10	—	pF
Input capacity of φRS	CφRS	—	10	—	pF
Input capacity of φROG, φSHUT*1	CφROG, CφSHUT	—	10	—	pF

*1 It indicates that φROG-R, φROG-G, φROG-B as φROG, φSHUT-R, φSHUT-G, φSHUT-B as φSHUT.

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
φ1, φ2, φLH, φRS	fφ1, fφ2, fφLH, fφRS	—	1	5	MHz

Input Clock Pulse Voltage Condition

Item		Min.	Typ.	Max.	Unit
φ1, φ2, φLH, φRS, φROG, φSHUT pulse voltage	High level	4.75	5.0	5.25	V
	Low level	—	0	0.1	V

Electrooptical Characteristics (Note 1)

(Ta = 25°C, V_{DD} = 12V, $f\phi_{RS}$ = 1MHz, Input clock = 5Vp-p, Light source = 3200K, IR cut filter CM-500S (t = 1.0mm))

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	1.3	2.0	2.7	V/(lx · s)	Note 2
	Green	R_G	2.1	3.2	4.3		
	Blue	R_B	1.6	2.5	3.4		
Sensitivity nonuniformity		PRNU	—	6	20	%	Note 3
Saturation output voltage		V_{SAT}	2	3.2	—	V	Note 4
Saturation exposure	Red	SE_R	0.74	1.6	—	lx · s	Note 5
	Green	SE_G	0.46	1	—		
	Blue	SE_B	0.58	1.28	—		
Dark voltage average		V_{DRK}	—	0.3	2.2	mV	Note 6
Dark signal nonuniformity		DSNU	—	1.5	5.5	mV	Note 6
Image lag		IL	—	0.02	—	%	Note 7
Supply current		I_{VDD}	—	26	50	mA	—
Total transfer efficiency		TTE	92	95	—	%	—
Output impedance		Zo	—	250	—	Ω	—
Offset level		V_{OS}	—	6.5	—	V	Note 8
Dynamic range		DR	1000	10670	—	—	Note 9

Notes)

1. In accordance with the given electrooptical characteristics, the black level is defined as the average value of D2, D3 to D12.
2. For the sensitivity test light is applied with a uniform intensity of illumination.
3. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

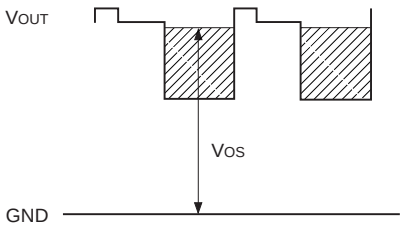
   V_{OUT-G} = 500mV (Typ.)

   $$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

   Where the 10500 pixels are divided into blocks of 100. The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
4. Use below the minimum value of the saturation output voltage.
5. Saturation exposure is defined as follows.

   $$SE = V_{SAT}/R$$

   Where R indicates R_R, R_G, R_B, and SE indicates SE_R, SE_G, SE_B.
6. Optical signal accumulated time τ int stands at 11ms.
7. V_{OUT-G} = 500mV (Typ.)
8. Vos is defined as indicated bellow.
   V_{OUT} indicates V_{OUT-R}, V_{OUT-G}, and V_{OUT-B}.

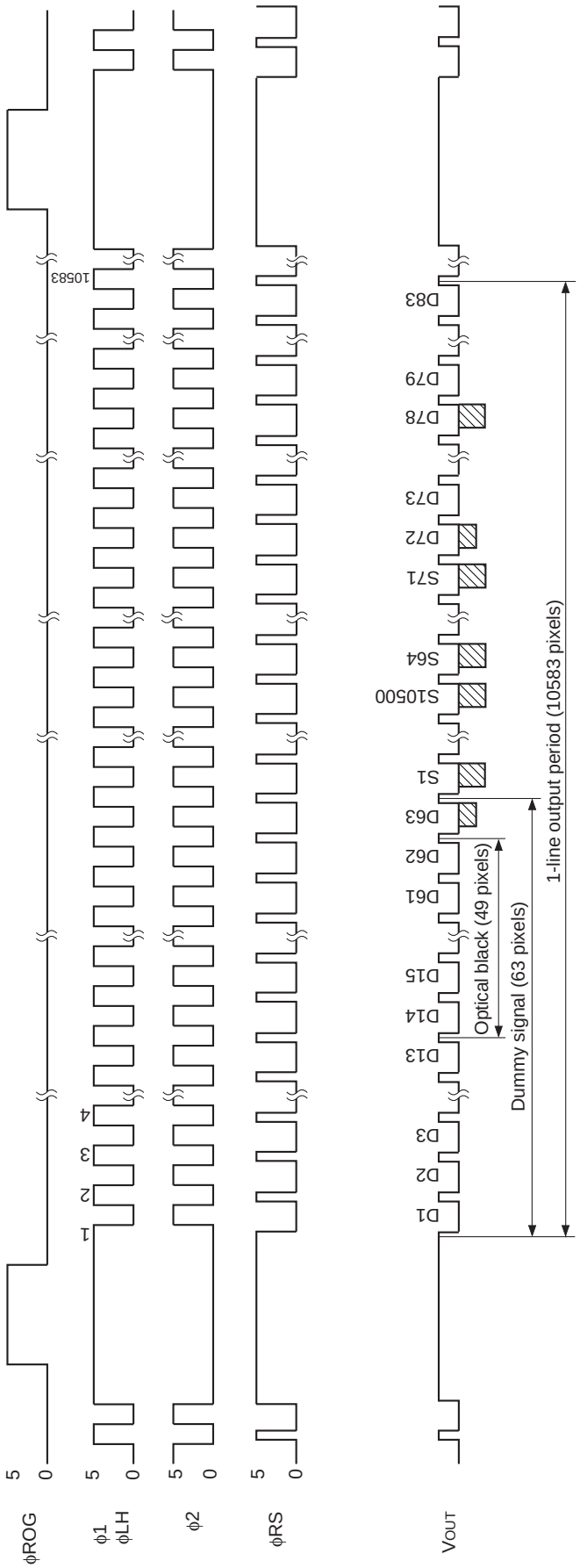


9. Dynamic range is defined as follows.

   $$DR = V_{SAT}/V_{DRK}$$

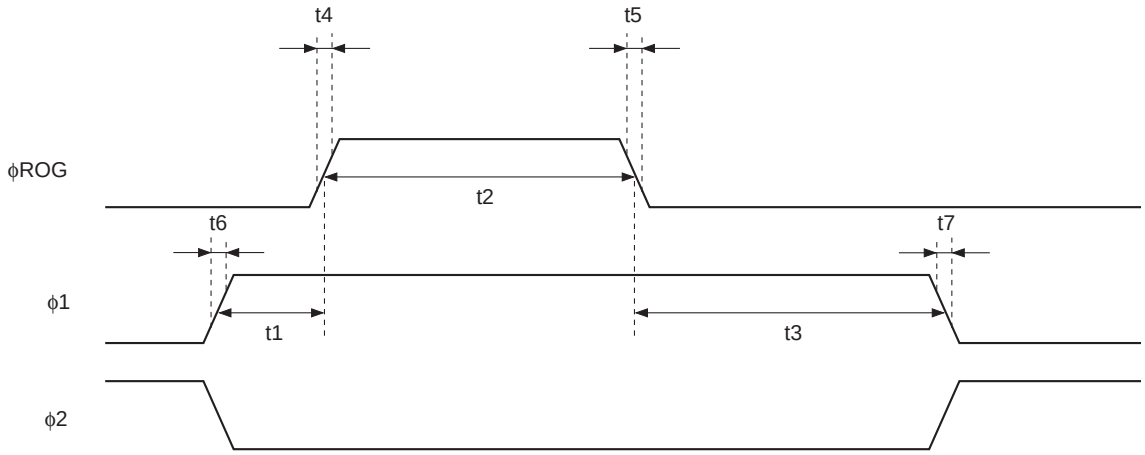
   When the optical signal accumulated time is shorter, the dynamic range gets wider because the optical signal accumulated time is in proportion to the dark voltage.

Clock Timing Chart 1

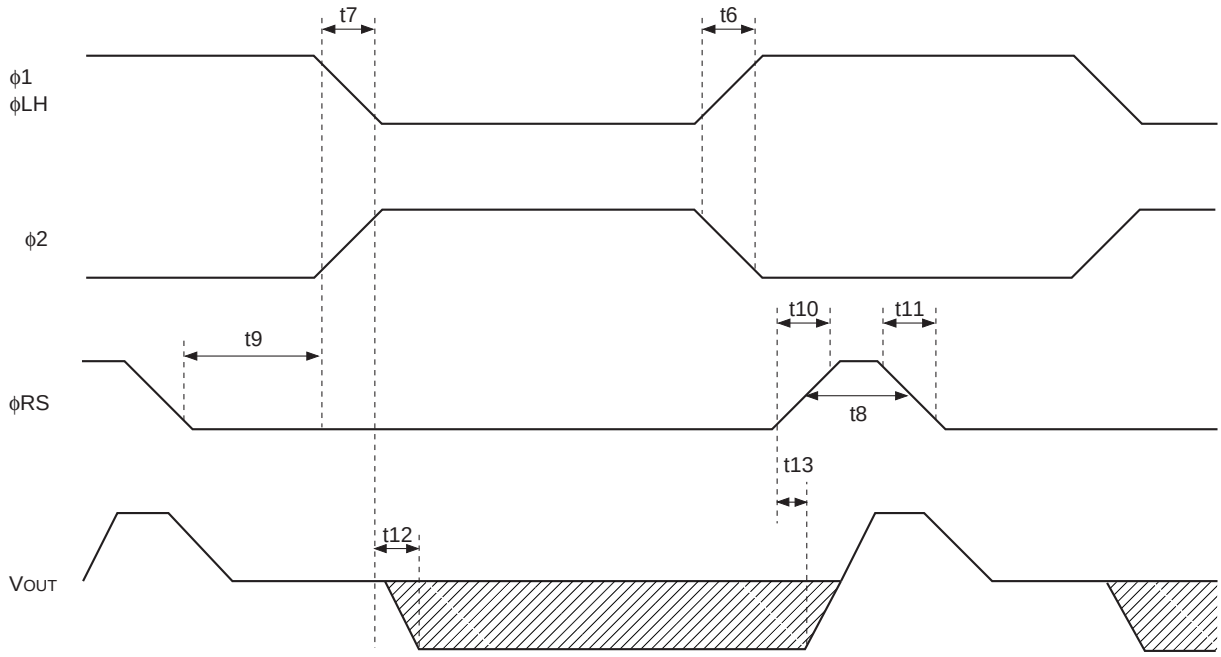


Note) The transfer pulses (φ1, φ2, φLH) must have more than 10583 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

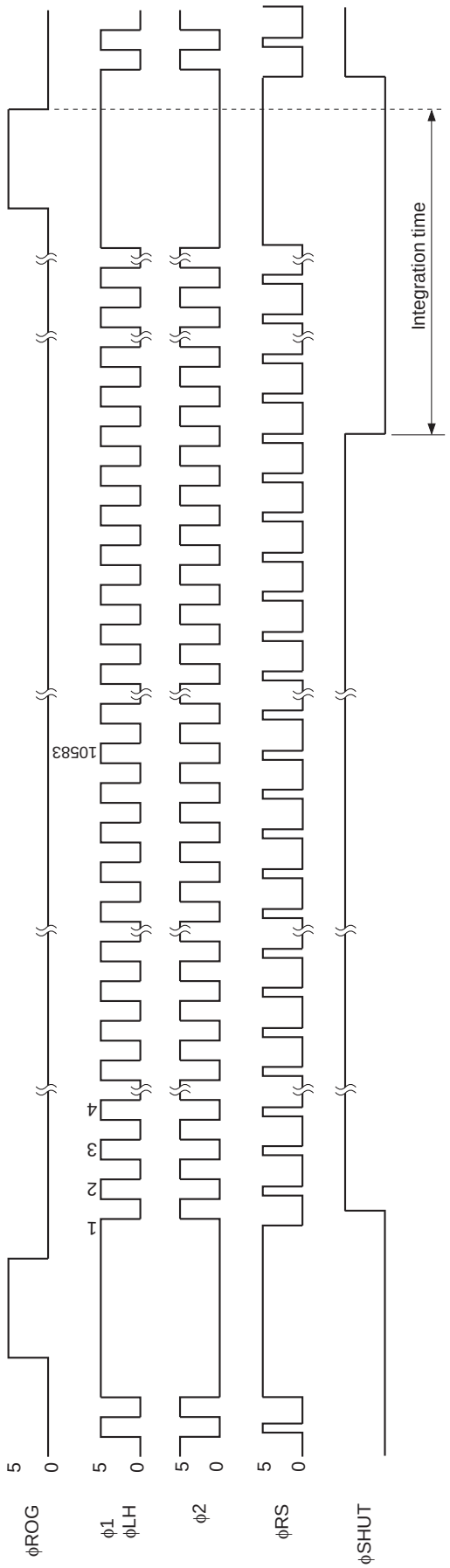
Clock Timing Chart 2



Clock Timing Chart 3



Clock Timing Chart 4 (Shutter Operation)



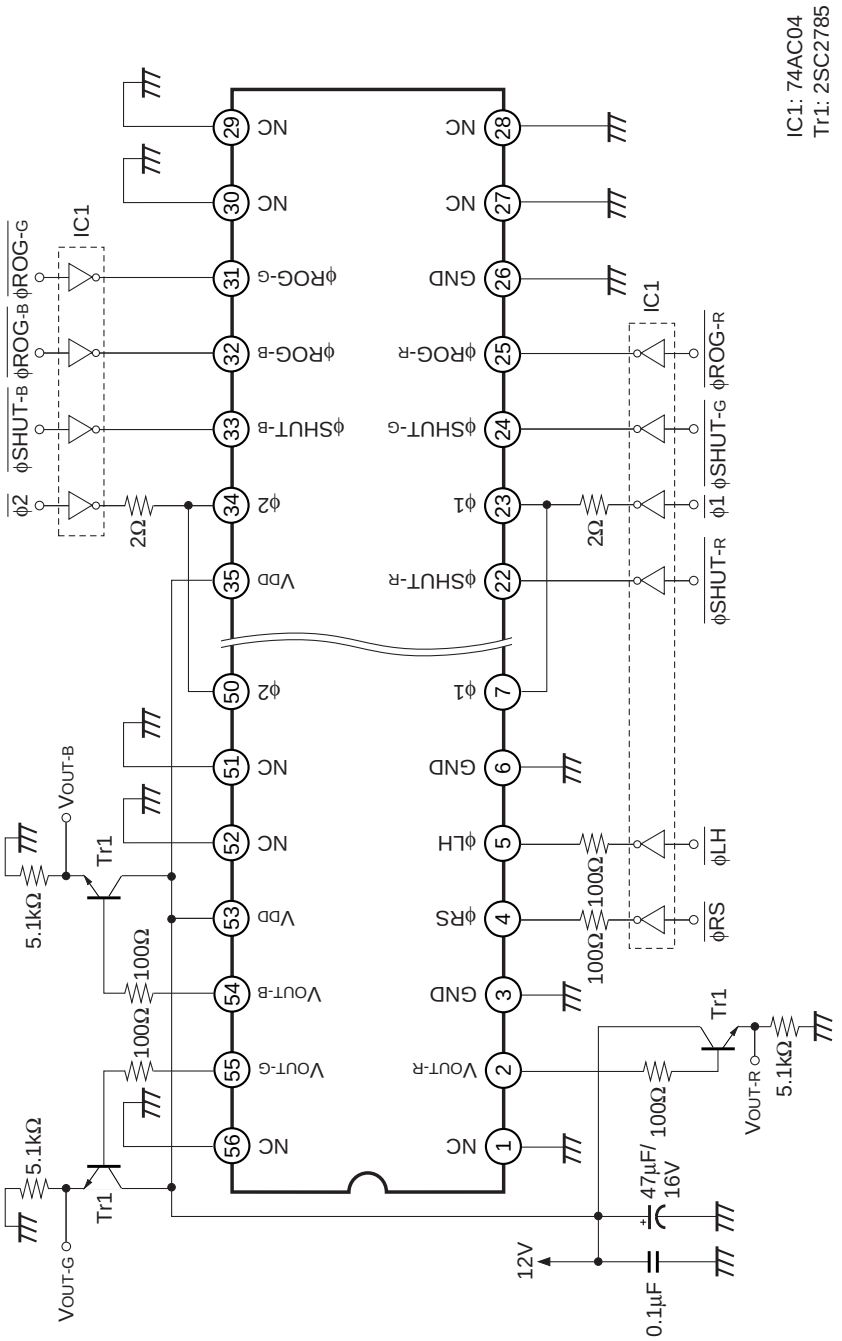
Note) Shutter pulse must not be low level during from 2 to 10583 of φ1.
Integration time can be controlled by changing the timing φSHUT fall.

Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φ1 pulse timing	t1	50	100	—	ns
φROG pulse high level period	t2	1200	3000	—	ns
φROG, φ1 pulse timing	t3	1200	3000	—	ns
φROG pulse rise time	t4	0	5	10	ns
φROG pulse fall time	t5	0	5	10	ns
φ1 pulse rise time/φ2 pulse fall time	t6	0	20	60	ns
φ1 pulse fall time/φ2 pulse rise time	t7	0	20	60	ns
φRS pulse high level period	t8	45	250*1	—	ns
φRS, φLH pulse timing	t9	45	250*1	—	ns
φRS pulse rise time	t10	0	10	30	ns
φRS pulse fall time	t11	0	10	30	ns
Signal output delay time	t12	—	10	—	ns
	t13	—	10	—	ns

*1 These timing data are the recommended condition under $f_{\phi RS}$ = 1MHz.

Application Circuit*1



*1 Data rate $f_{\phi RS}$ = 1MHz. In the case of $f_{\phi RS}$ = 5MHz, 3 pieces of 74AC04 are recommended to use for φ1 and φ2 driver.

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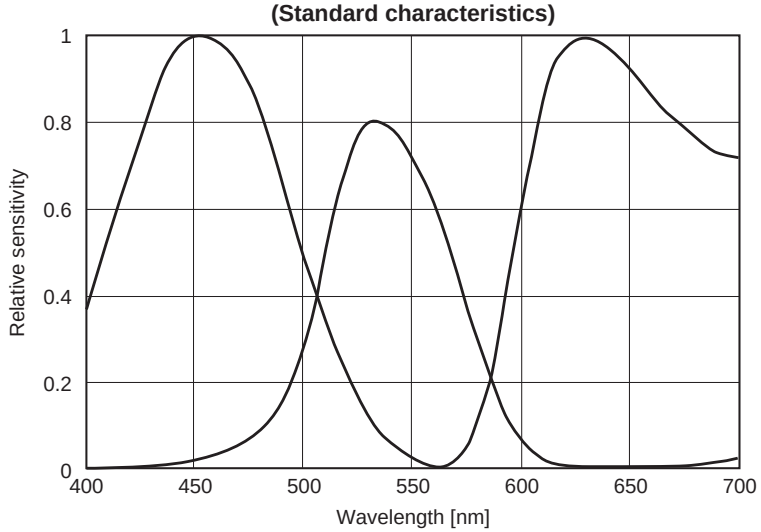
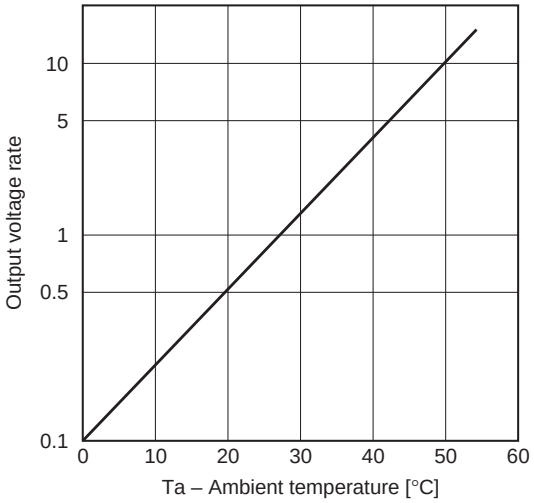
Example of Representative Characteristics (V_{DD} = 12V, Ta = 25°C)

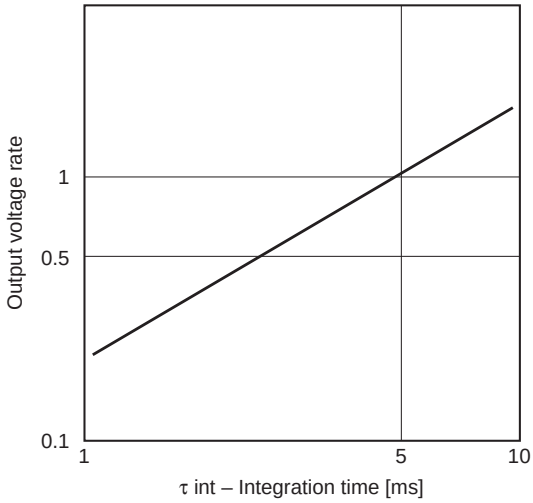
Spectral sensitivity characteristics (Standard characteristics)



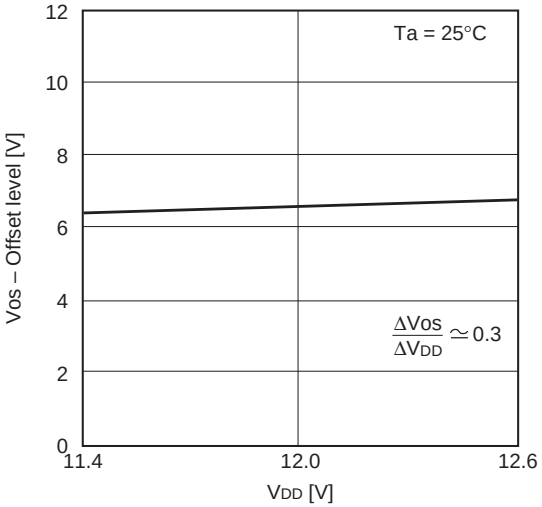
Dark signal output temperature characteristics (Standard characteristics)



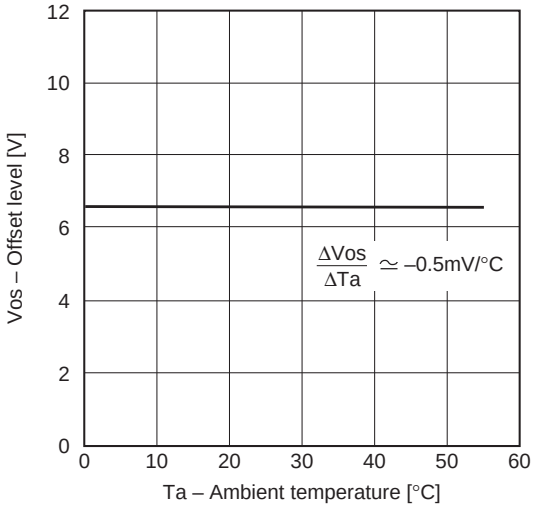
Integration time output voltage characteristics (Standard characteristics)



Offset level vs. V_{DD} characteristics (Standard characteristics)



Offset level vs. temperature characteristics (Standard characteristics)



Notes of Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

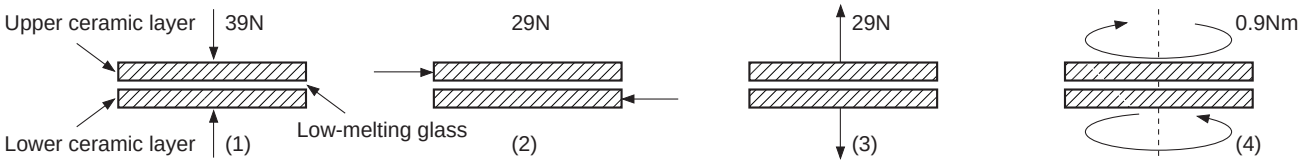
a) Remain within the following limits when applying static load to the ceramic portion of the package:

(1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)

(2) Shearing strength: 29N/surface

(3) Tensile strength: 29N/surface

(4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,

(1) Applying repetitive bending stress to the external leads.

(2) Applying heat to the external leads for an extended period of time with soldering iron.

(3) Rapid cooling or heating.

(4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.

(5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

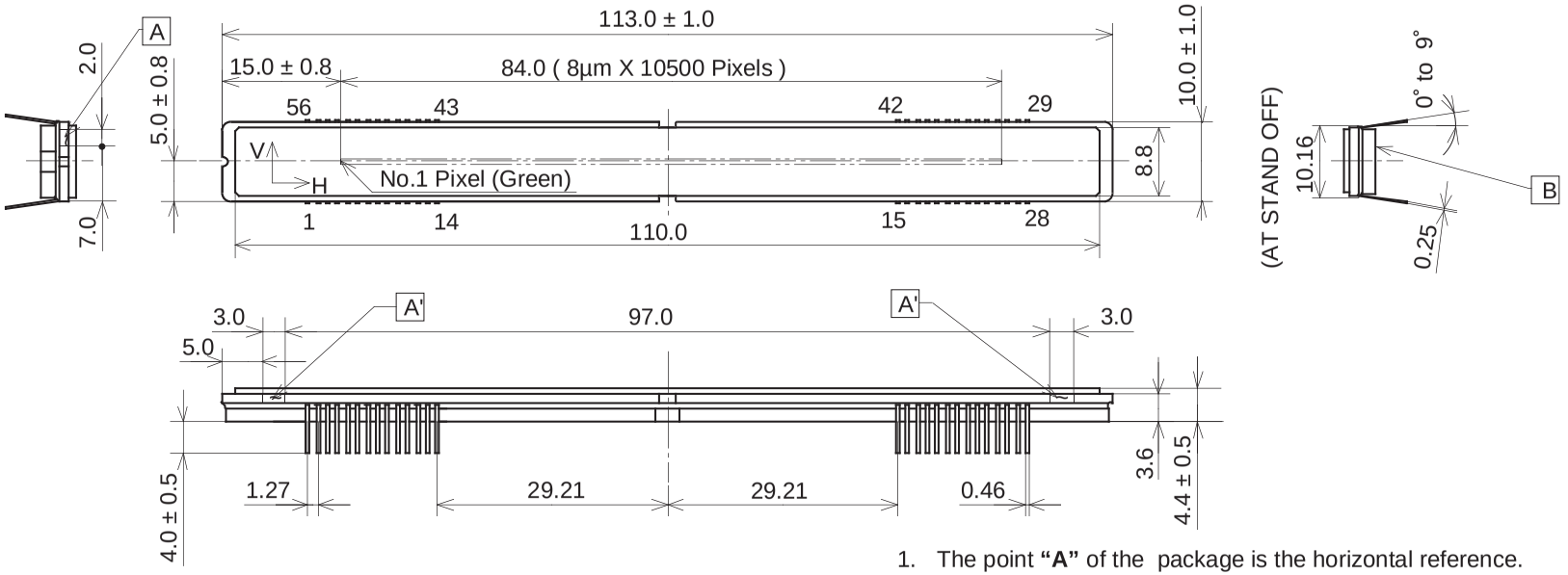
4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

56Pin DIP (400mil)



1. The point **"A"** of the package is the horizontal reference.
   The two points **"A'"** of the package are the vertical reference.
2. The height from the bottom **"B"** to the effective image area is 2.4 ± 0.30mm.
3. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.
4. The notch of the package must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42ALLOY
PACKAGE MASS	13.5g
DRAWING NUMBER	LS-E4(E)