SSP MODULE

SSP Module Silicon/Data Sheet Errata

The PICmicro® microcontrollers you have received all exhibit anomalous behavior in their Synchronous Serial Port (SSP) modules, as described in this document. They otherwise conform functionally to the descriptions provided in their respective Device Data Sheets and Reference Manuals, as amended by silicon release errata for particular devices.

Users are encouraged to review the latest Device Data Sheets and errata available for additional information concerning an individual device. These documents may be obtained directly from the Microchip corporate web site, at **www.microchip.com**.

This issue is expected to be resolved in future silicon revisions of the designated parts.

This issue effects all silicon revisions of the following devices:

- PIC14000
- PIC16C62A
- PIC16C62B
- PIC16C63
- PIC16C63A
- PIC16CR63
- PIC16C64A
- PIC16C65A
- PIC16C65B
- PIC16CR65
- PIC16C66
- PIC16C67
- PIC16C72
- PIC16C73A
- PIC16C72A
- PIC16C73B
- PIC16C74A
- PIC16C74B
- PIC16C76
- PIC16C77
- PIC16C923
- PIC16C924
- PIC16C925
- PIC16C926
- PIC16F72
- PIC16F73
- PIC16F74
- PIC16F76
- PIC16F77
- PIC16F818
- PIC16F819

1. Issue: I²C™ (Slave Mode)

In its current implementation, the module may fail to correctly recognize certain Repeated START conditions. For this discussion, a Repeated START is defined as a START condition presented to the bus after an initial valid START condition has been recognized and the START status bit (SSPSTAT<3>) has been set, and before a valid STOP condition is received.

If a Repeated START is not recognized, a loss of synchronization between the Master and Slave may occur; the condition may continue until the module is reset. A NACK condition, generated by the Slave for any reason, will not reset the module.

This failure has been observed only under two circumstances:

- A Repeated START occurs within the frame of a data or address byte. The unexpected START condition may be erroneously interpreted as a data bit, provided that the required conditions for setup and hold times are met.
- A Repeated START condition occurs between two back-to-back slave address matches in the same Slave, with the R/$\overline{W}$ bit set to Read (= 1) in both cases. (This circumstance is regarded as being unlikely in normal operation.)

Work around

A time-out routine should be used to monitor the module's operation. The timer is enabled upon the receipt of a valid START condition; if a time-out occurs, the module is reset. The length of the time-out period will vary from application to application, and will need to be determined by the user.

Two methods are suggested to reset the module:

1. Change the mode of the module to something other than the desired mode by changing the settings of bits SSPM3:SSPM0 (SSPCON<3:0>); then, change the bits back to desired configuration.
2. Disable the module by clearing the SSPEN bit (SSPCON<5>); then, re-enable the module by setting the bit.

Other methods may be available.

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Clarifications/Corrections to the Data Sheets

1. Module: SSP (SPI Mode)

Note: This correction applies to the Data Sheets for the following devices:

- PIC16C62B/72A (DS35008B)
- PIC16C63A/65B/73B/74B (DS30605C)
- PIC16C923/924 (DS30444E)
- PIC16C925/926 (DS39544A)
- PIC16F72 (DS39597B)
- PIC16F73/74/76/77 (DS30325B)
- PIC16F818/819 (DS39598C)

In addition, this clarification applies only to the following devices in the PIC16C6X Data Sheet (DS30234D):

- PIC16C66
- PIC16C67

Any devices not explicitly listed in this section do not implement SPI mode, and are not affected by this clarification.

The description of the operation of the CKE bit (SSPSTAT<6>) is clarified. Please substitute the description in Register 1, below, for all occurrences of the existing text for the SSPSTAT register, bit 6 (new text in **bold**).

Note: This text refers only to the operation of the CKE bit in SPI mode; its operation in I^2C mode is unchanged.

2. Module: SSP (SPI Slave Mode)

Note: This correction applies to the Data Sheets for the following devices:

- PIC16C6X (DS30234D), **except** PIC16C61 (does not implement the SSP module)
- PIC16C62B/72A (DS35008B)
- PIC16C63A/65B/73B/74B (DS30605C)
- PIC16C923/924 (DS30444E)
- PIC16C925/926 (DS39544A)
- PIC16F72 (DS39597B)
- PIC16F73/74/76/77 (DS30325B)
- PIC16F818/819 (DS39598C)

Any other devices not explicitly listed in this section do not implement SPI mode, and are not affected by this clarification.

The description of the operation of SPI Slave mode is clarified as follows:

Before enabling the module in SPI Slave mode, the state of the clock line (SCK) must match the polarity selected for the IDLE state. The clock line can be observed by reading the SCK pin. The polarity of the IDLE state is determined by the CKP bit (SSPCON<4>).

This foregoing text should be added to the appropriate subsections of the “SSP Module” chapter entitled “SPI Mode”, and read in context with any discussions of SPI Slave mode.

In the case of DS30234D, the text applies to both implementations of SPI mode, as described in Sections 11.2 and 11.3.

REGISTER 1: SSPSTAT: SSP STATUS REGISTER (EXCERPT)

bit 6 **CKE:** SPI Clock Select bit

1 = **Transmit occurs on transition from active to IDLE clock state**

0 = **Transmit occurs on transition from IDLE to active clock state**

Note: Polarity of clock state is set by the CKP bit (SSPCON<4>).

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REVISION HISTORY

Revision A Document (7/2002):

Original version (I^2C Slave Issue)

Revision B Document (1/2003):

Clarification of original issue to include Restart conditions. Addition of data sheet clarification 1 (SPI Mode, CKE bit).

Revision C Document (3/2003):

Addition of data sheet clarification 2 (SPI Slave Mode, operation).

NOTES:

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