

NTGS4141N

Power MOSFET

30 V, 7.0 A, Single N-Channel, TSOP-6

Features

- Low $R_{DS(on)}$
- Low Gate Charge
- Pb-Free Package is Available

Applications

- Load Switch
- Notebook PC
- Desktop PC

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	30	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	5.0	
				$T_A = 85^\circ\text{C}$	3.6
	$t \leq 10$ s	$T_A = 25^\circ\text{C}$	7.0		
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.0	
				$t \leq 10$ s	2.0
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	3.5	
				$T_A = 85^\circ\text{C}$	2.5
				$T_A = 25^\circ\text{C}$	P_D
Power Dissipation (Note 2)					
Pulsed Drain Current	$t_p = 10$ μs	I_{DM}	21	A	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	2.0	A	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 30$ V, $I_L = 10.4$ A, $V_{GS} = 10$ V, $L = 1.0$ mH, $R_G = 25$ Ω)		EAS	54	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	125	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	248	

1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0773 in sq).

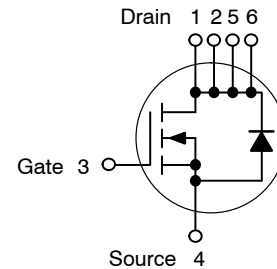


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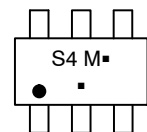
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	21.5 m Ω @ 10 V	7.0 A
	30 m Ω @ 4.5 V	

N-Channel



TSOP-6
CASE 318G
STYLE 1

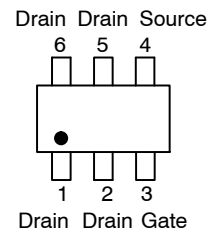
MARKING DIAGRAM



- S4 = Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTGS4141NT1	TSOP-6	3000/Tape & Reel
NTGS4141NT1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTGS4141N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			18.4		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25°C		1.0	μA
			T _J = 125°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0		3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			5.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.0 A		21.5	25	mΩ
		V _{GS} = 4.5 V, I _D = 6.0 A		30	35	
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 7.0 A		30		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 24 V		560		pF
Output Capacitance	C _{OSS}			115		
Reverse Transfer Capacitance	C _{RSS}			75		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 7.0 A		12		nC
Threshold Gate Charge	Q _{G(TH)}			0.85		
Gate-to-Source Charge	Q _{GS}			1.9		
Gate-to-Drain Charge	Q _{GD}			3.0		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 7.0 A		6.0		nC
Threshold Gate Charge	Q _{G(TH)}			0.8		
Gate-to-Source Charge	Q _{GS}			1.85		
Gate-to-Drain Charge	Q _{GD}			3.0		
Gate Resistance	R _G			2.8		Ω

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 24 V, I _D = 7.0 A, R _G = 3.0 Ω		6.0		ns
Rise Time	t _r			15		
Turn-Off Delay Time	t _{d(OFF)}			18		
Fall Time	t _f			4.0		

DRAIN - SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2.0 A	T _J = 25°C	0.78	1.0	V
			T _J = 125°C	0.63		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V di _S /dt = 100 A/μs, I _S = 2.0 A		15		ns
Charge Time	t _a			9.0		
Discharge Time	t _b			6.0		
Reverse Recovery Charge	Q _{RR}			8.0		

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTGS4141N

TYPICAL PERFORMANCE CURVES

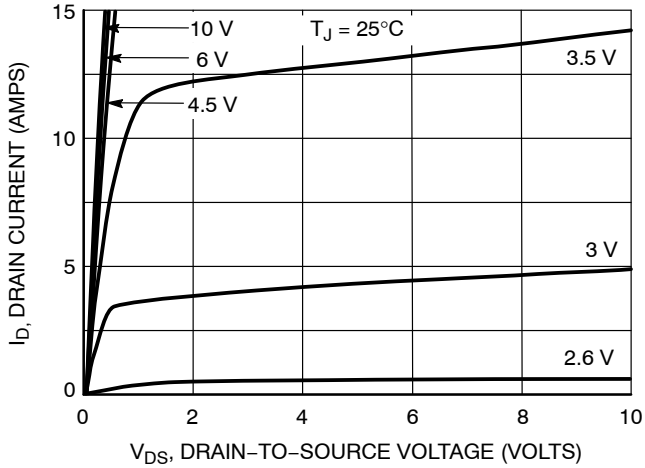


Figure 1. On-Region Characteristics

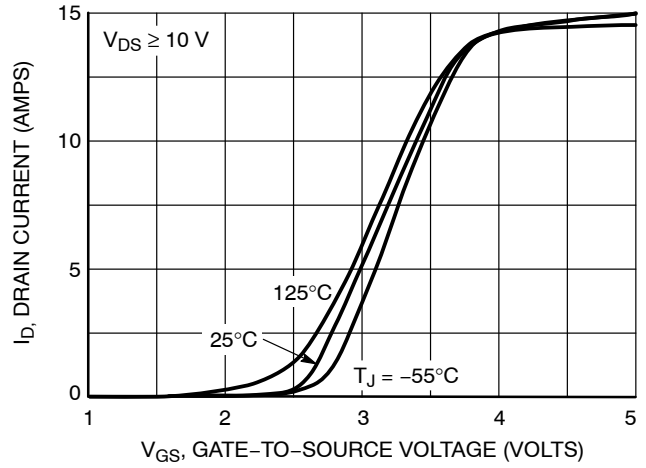


Figure 2. Transfer Characteristics

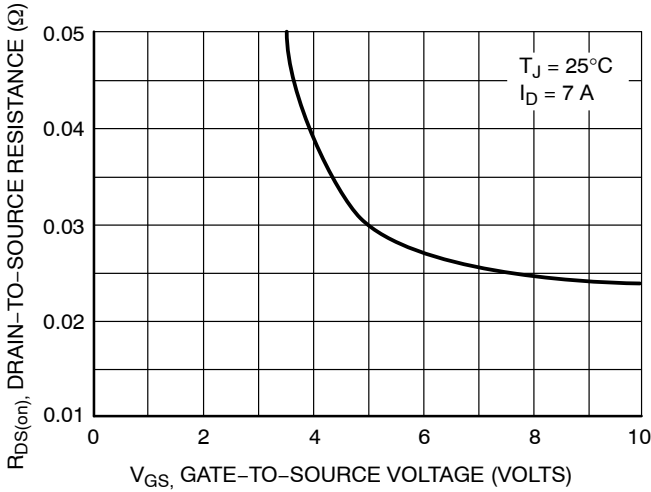


Figure 3. On-Resistance vs. Gate-to-Source Voltage

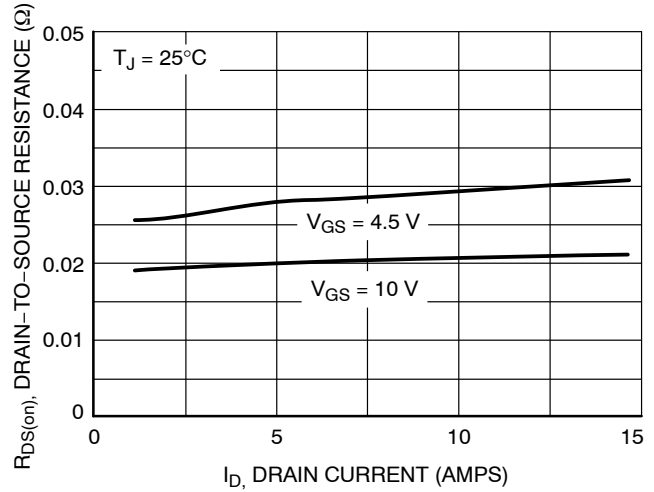


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

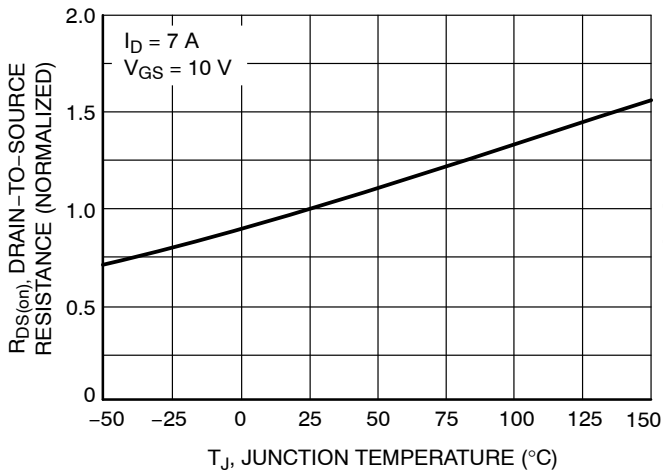


Figure 5. On-Resistance Variation with Temperature

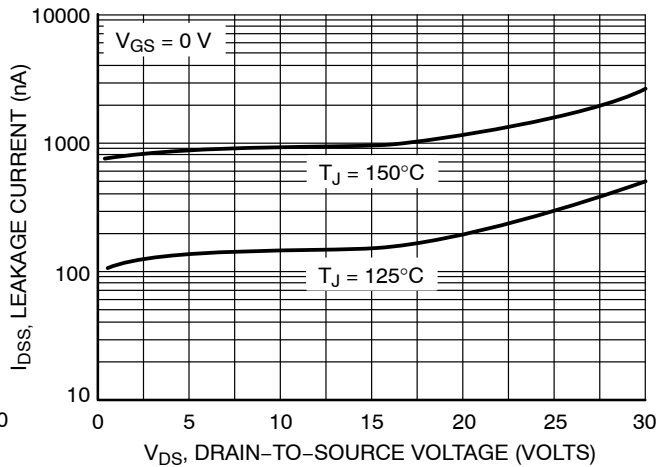
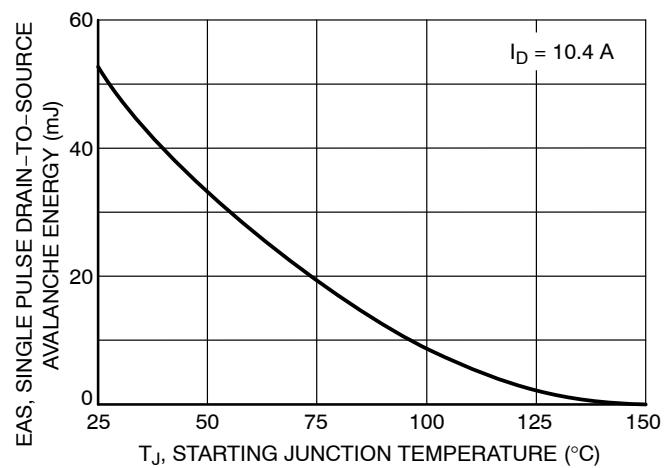
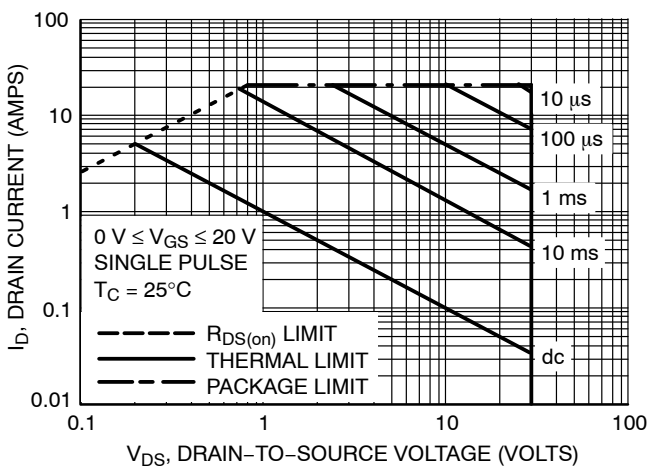
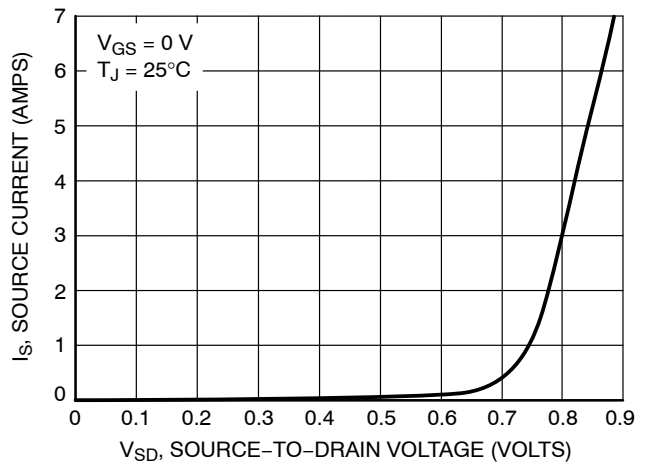
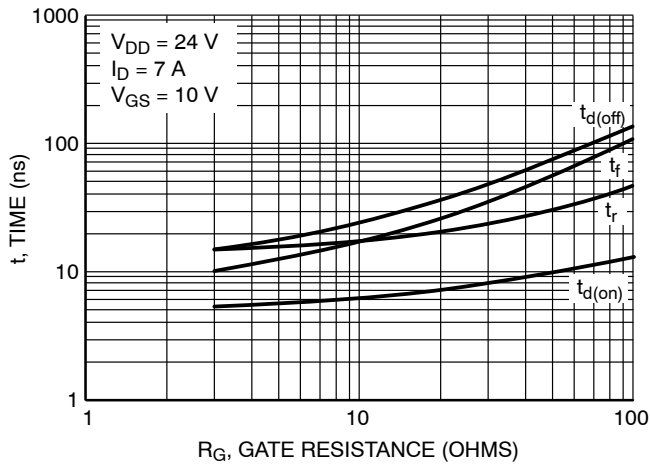
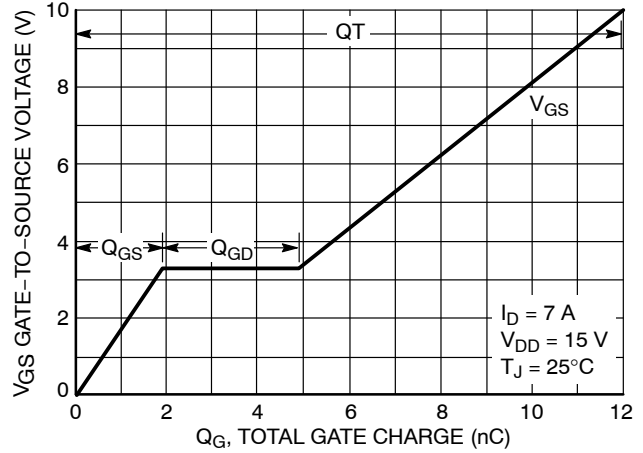
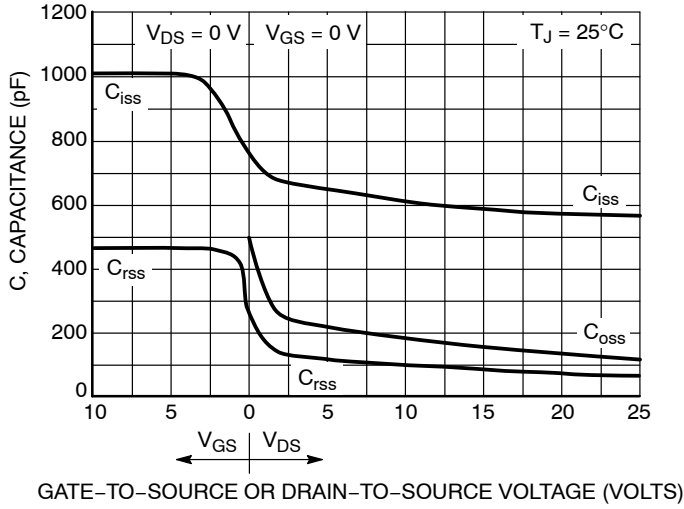


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CURVES



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TYPICAL PERFORMANCE CURVES

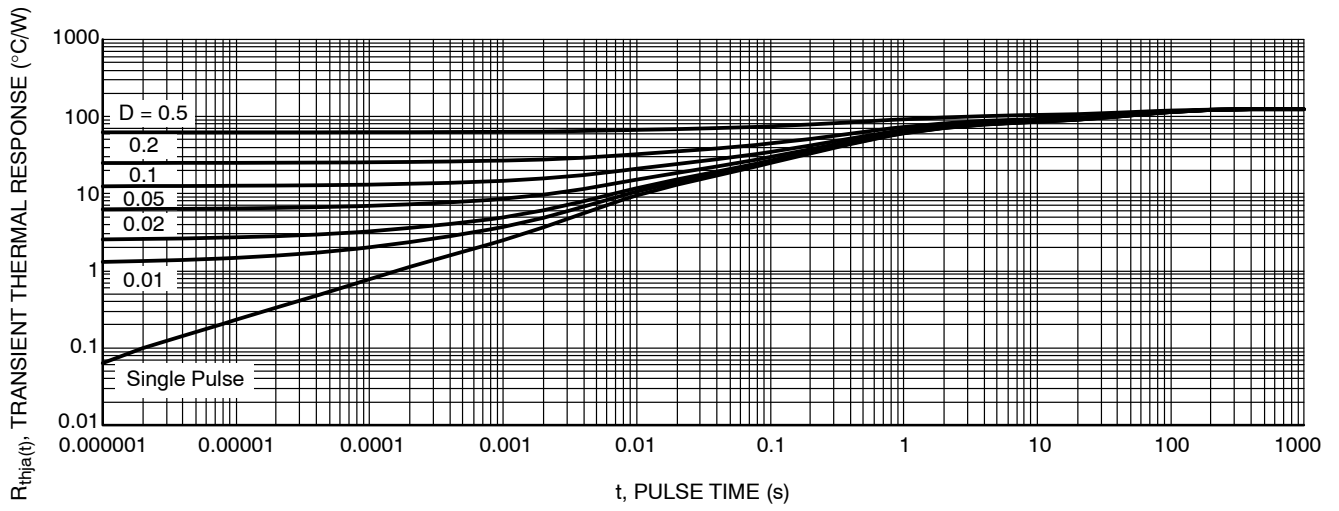
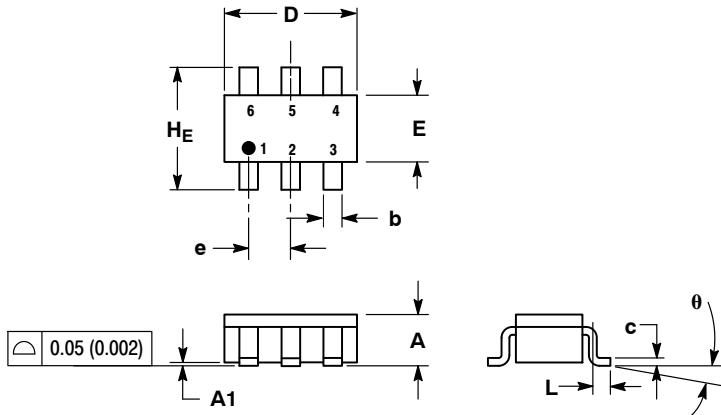


Figure 13. Thermal Response

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PACKAGE DIMENSIONS

TSOP-6
CASE 318G-02
ISSUE T



NOTES:

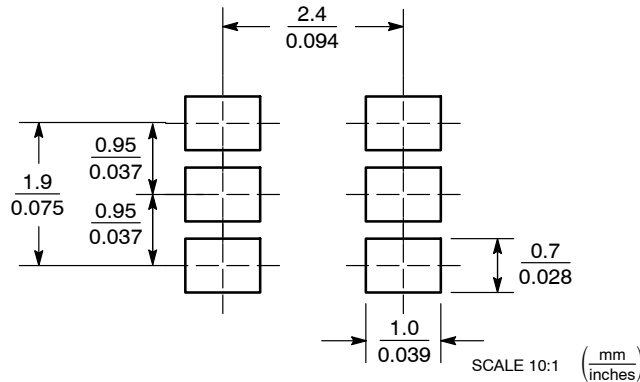
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
theta	0°	-	10°	0°	-	10°

STYLE 1:

1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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