NTGS4141N

Power MOSFET

30 V, 7.0 A, Single N−Channel, TSOP−6

Features

- Low $R_{DS(on)}$
- Low Gate Charge
- Pb−Free Package is Available

Applications

- Load Switch
- Notebook PC
- Desktop PC

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	5.0	A
		T_A = 85°C		3.6	
	t ≤ 10 s	T_A = 25°C		7.0	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.0	W
	t ≤ 10 s			2.0	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	3.5	A
		T_A = 85°C		2.5	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.5	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	21	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	2.0	A
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 30 V, I_L = 10.4 A, V_{GS} = 10 V, L = 1.0 mH, R_G = 25 Ω)			EAS	54	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	125	°C/W
Junction−to−Ambient − t ≤ 10 s (Note 1)	$R_{\theta JA}$	62.5	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	248	

1. Surface−mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0773 in sq).

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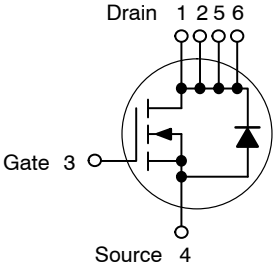
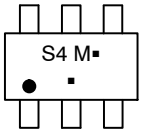
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	21.5 mΩ @ 10 V	7.0 A
	30 mΩ @ 4.5 V	

N−Channel



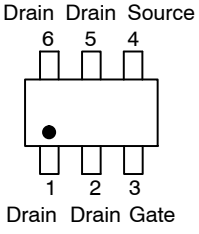
TSOP−6
CASE 318G
STYLE 1

MARKING DIAGRAM



S4 = Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTGS4141NT1	TSOP−6	3000/Tape & Reel
NTGS4141NT1G	TSOP−6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				18.4		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7.0 A			21.5	25	mΩ
		V_{GS} = 4.5 V, I_D = 6.0 A			30	35	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 7.0 A			30		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 24 V			560		pF
Output Capacitance	C_{OSS}				115		
Reverse Transfer Capacitance	C_{RSS}				75		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 7.0 A			12		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.85		
Gate−to−Source Charge	Q_{GS}				1.9		
Gate−to−Drain Charge	Q_{GD}				3.0		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 7.0 A			6.0		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.8		
Gate−to−Source Charge	Q_{GS}				1.85		
Gate−to−Drain Charge	Q_{GD}				3.0		
Gate Resistance	R_G				2.8		Ω
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 24 V, I_D = 7.0 A, R_G = 3.0 Ω			6.0		ns
Rise Time	t_r				15		
Turn−Off Delay Time	$t_{d(OFF)}$				18		
Fall Time	t_f				4.0		
DRAIN − SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.0 A	T_J = 25°C		0.78	1.0	V
			T_J = 125°C		0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 2.0 A			15		ns
Charge Time	t_a				9.0		
Discharge Time	t_b				6.0		
Reverse Recovery Charge	Q_{RR}				8.0		nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

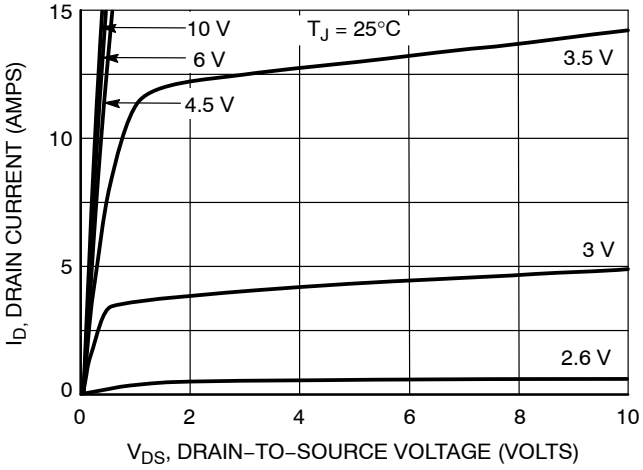


Figure 1. On−Region Characteristics

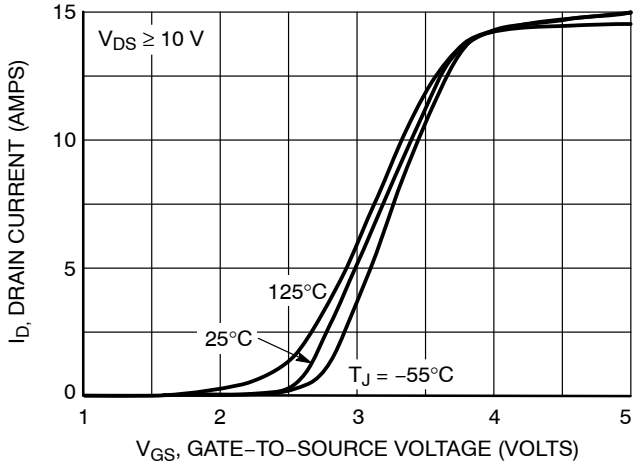


Figure 2. Transfer Characteristics

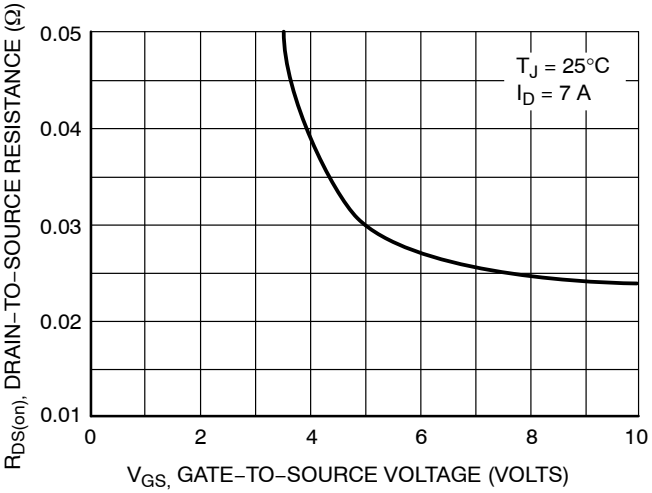


Figure 3. On−Resistance vs. Gate−to−Source Voltage

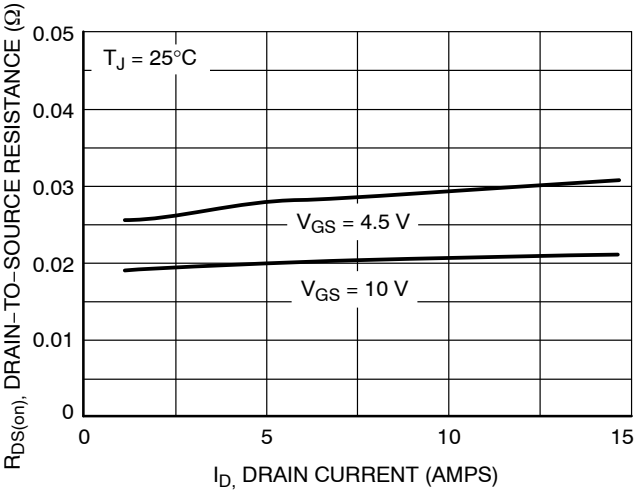


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

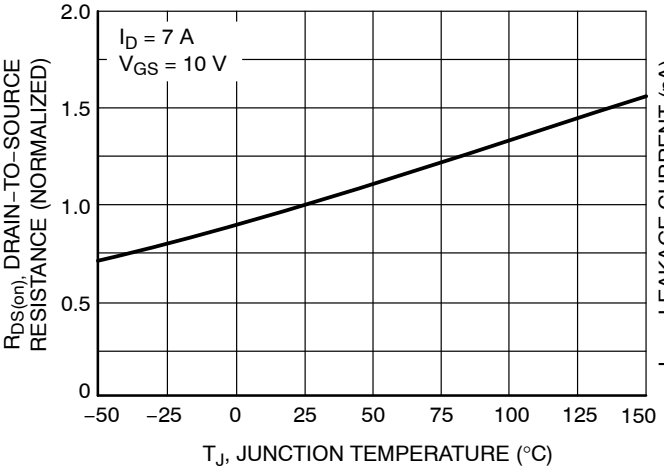


Figure 5. On−Resistance Variation with Temperature

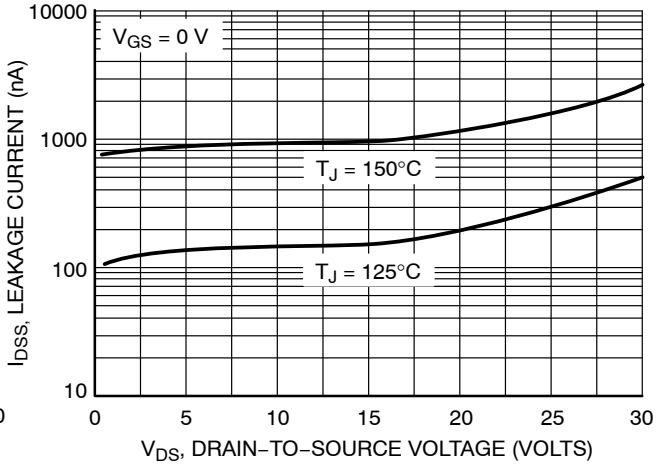


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

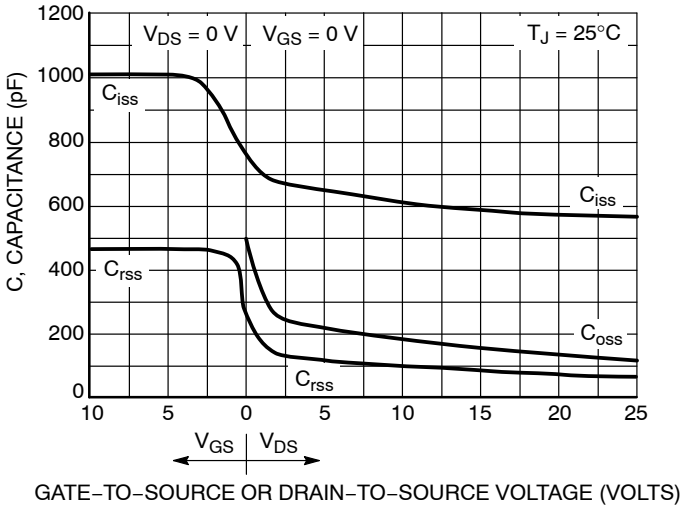


Figure 7. Capacitance Variation

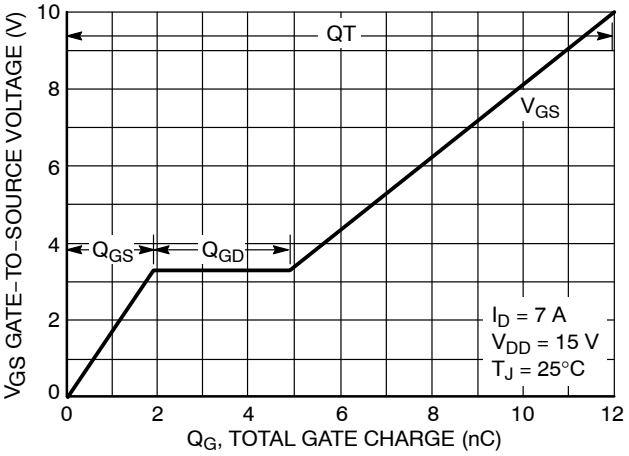


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

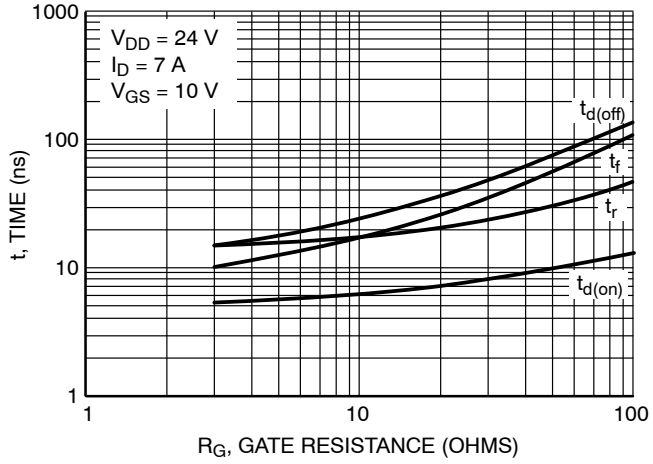


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

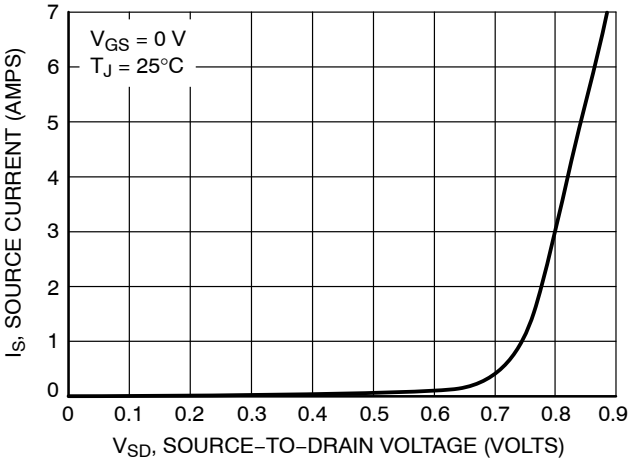


Figure 10. Diode Forward Voltage vs. Current

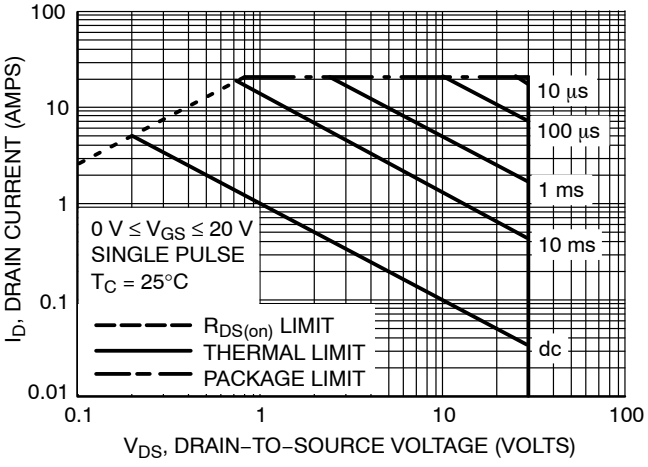


Figure 11. Maximum Rated Forward Biased Safe Operating Area

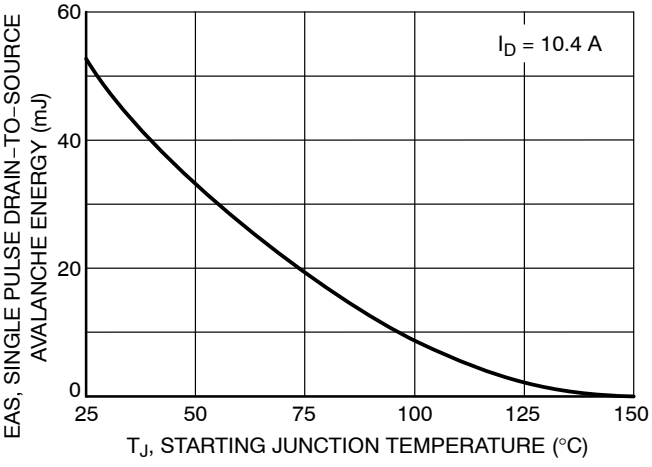


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL PERFORMANCE CURVES

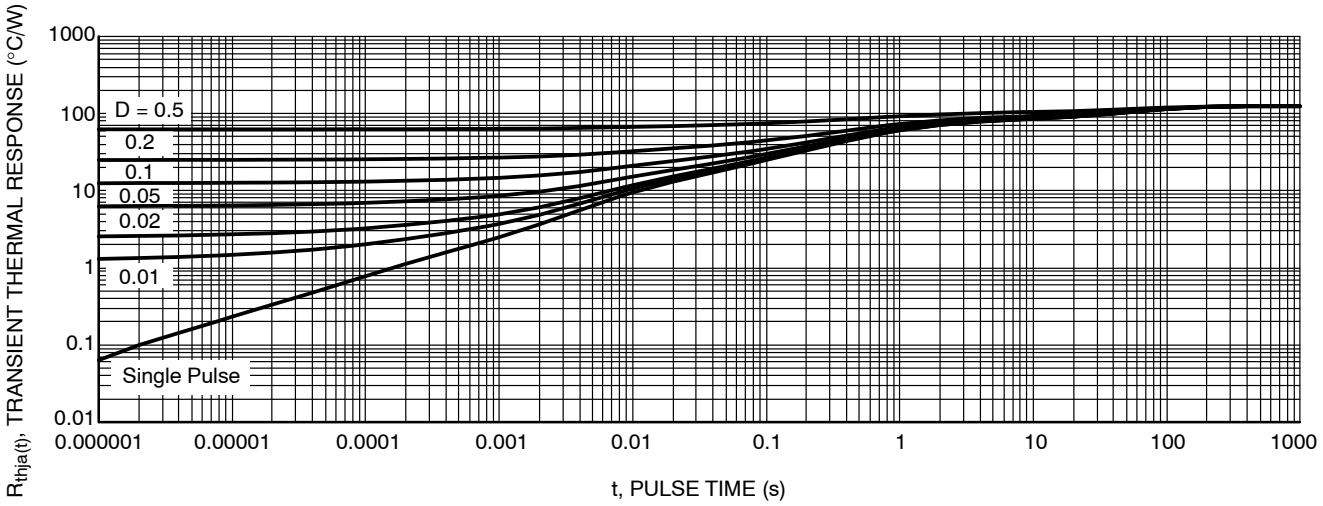
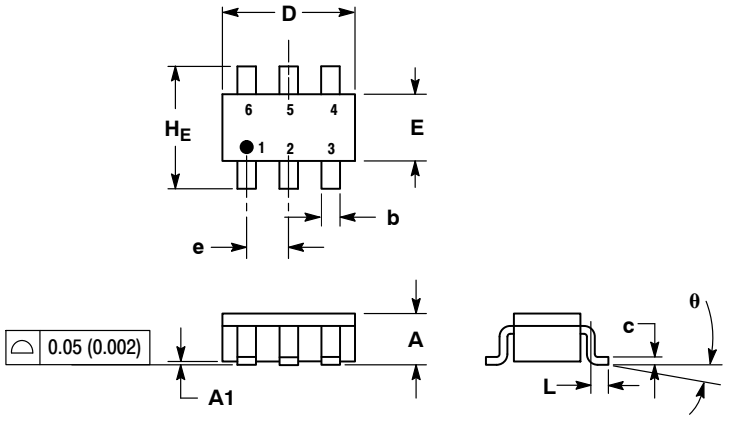


Figure 13. Thermal Response

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE T

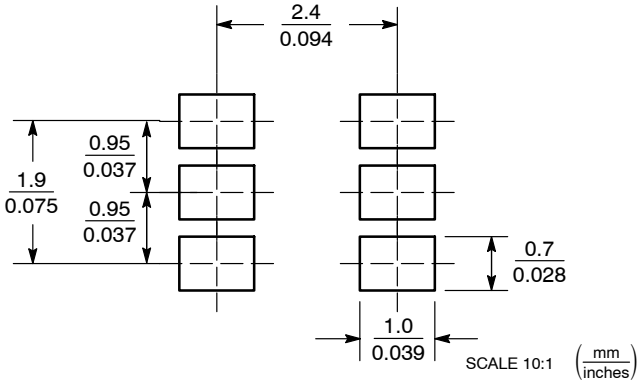


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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