

# FDMA8878

## Single N-Channel Power Trench® MOSFET 30 V, 9.0 A, 16 mΩ

### Features

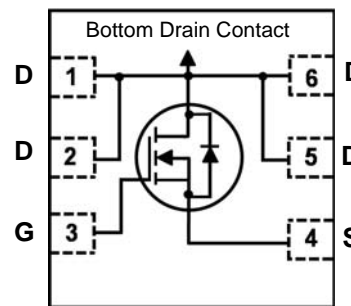
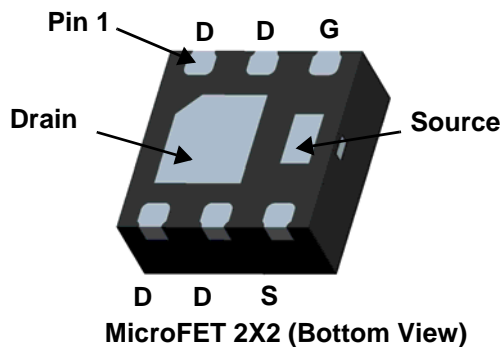
- Max  $r_{DS(on)}$  = 16 mΩ at  $V_{GS} = 10$  V,  $I_D = 9.0$  A
- Max  $r_{DS(on)}$  = 19 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 8.5$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- Fast switching speed
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for  $r_{DS(on)}$ , switching performance.

### Application

- DC/DC Buck Converters
- Load Switch in NB
- Notebook Battery Power Management



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage (Note 3)	±20	V
$I_D$	Drain Current -Continuous (Package Limited) $T_C = 25$ °C	10	A
	-Continuous $T_A = 25$ °C (Note 1a)	9.0	
	-Pulsed	40	
$P_D$	Power Dissipation $T_A = 25$ °C (Note 1a)	2.4	W
	Power Dissipation $T_A = 25$ °C (Note 1b)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
878	FDMA8878	MicroFET 2x2	7 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		26		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.2	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9.0\text{ A}$		13	16	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 8.5\text{ A}$		16	19	
		$V_{GS} = 10\text{ V}$ , $I_D = 9.0\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		17	21	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 9.0\text{ A}$		41		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		539	720	pF
$C_{oss}$	Output Capacitance			172	230	pF
$C_{rss}$	Reverse Transfer Capacitance			24	35	pF
$R_g$	Gate Resistance			1.3		$\Omega$

### Switching Characteristics

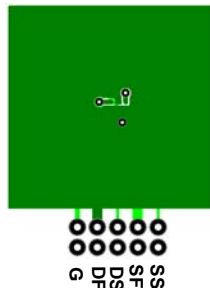
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 9.0\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		6	12	ns
$t_r$	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			14	25	ns
$t_f$	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		8.5	12
	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 15\text{ V}$ $I_D = 9.0\text{ A}$	4.1	5.8	nC
$Q_{gs}$	Total Gate Charge			1.6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.2		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.0\text{ A}$ (Note 2)		0.75	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 9.0\text{ A}$ (Note 2)		0.86	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 9.0\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		16	28	ns
$Q_{rr}$	Reverse Recovery Charge			4	10	nC

#### NOTES:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $52\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



b.  $145\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0 %.

3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

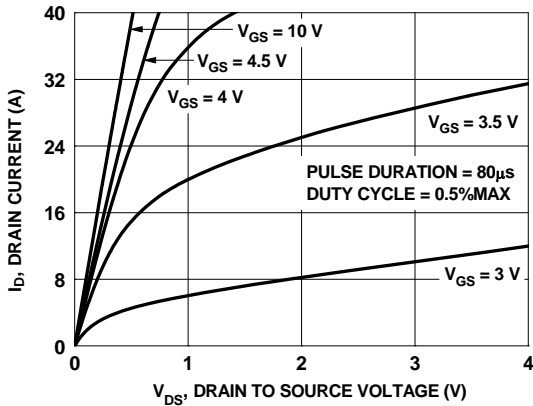


Figure 1. On Region Characteristics

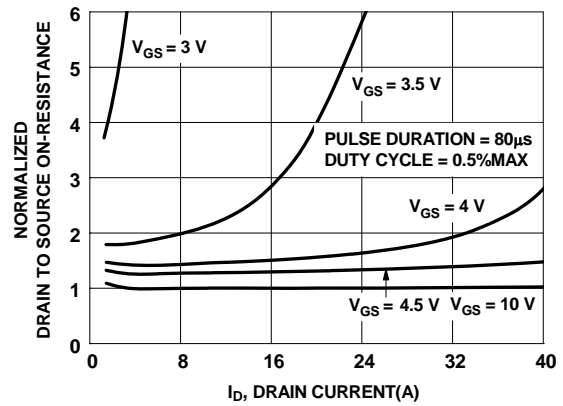


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

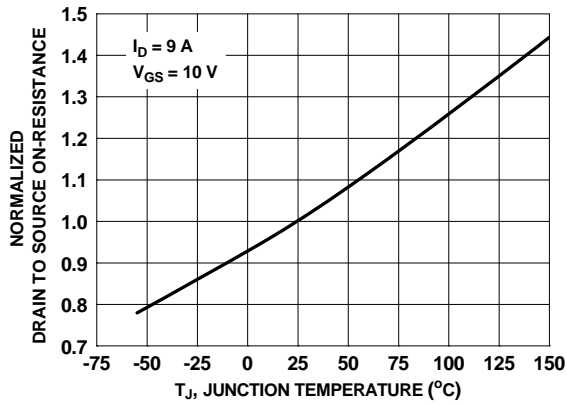


Figure 3. Normalized On Resistance vs Junction Temperature

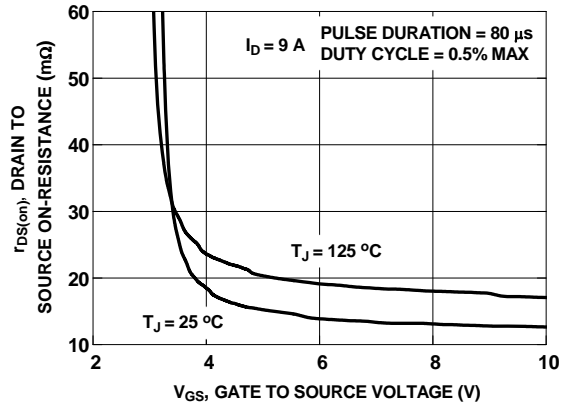


Figure 4. On-Resistance vs Gate to Source Voltage

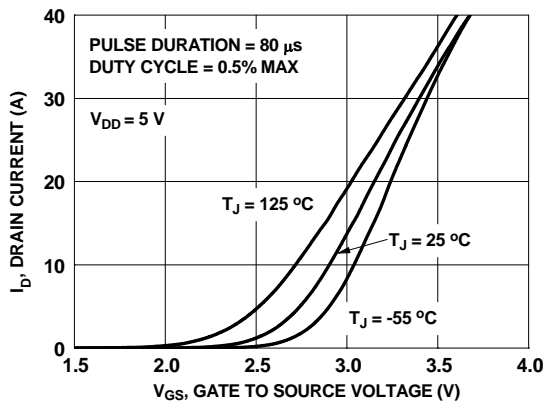


Figure 5. Transfer Characteristics

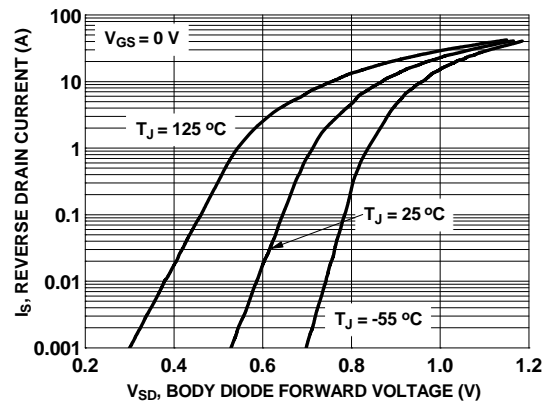
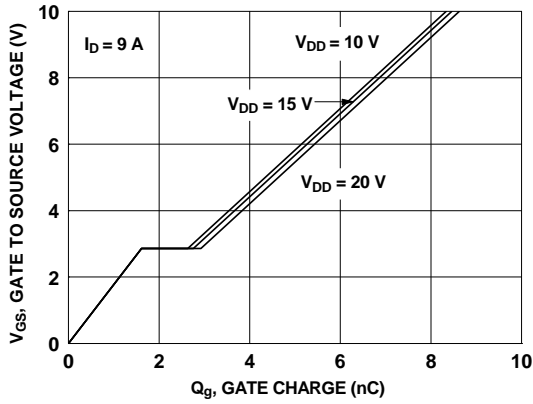
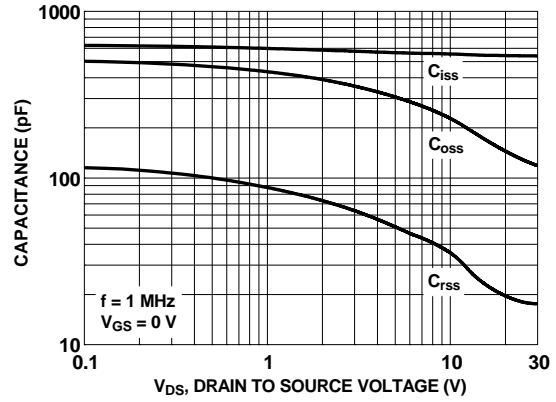


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

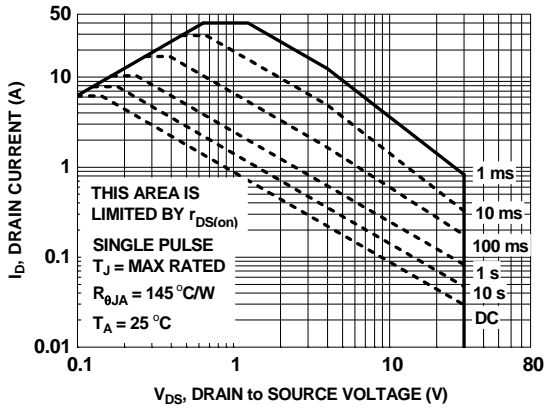
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



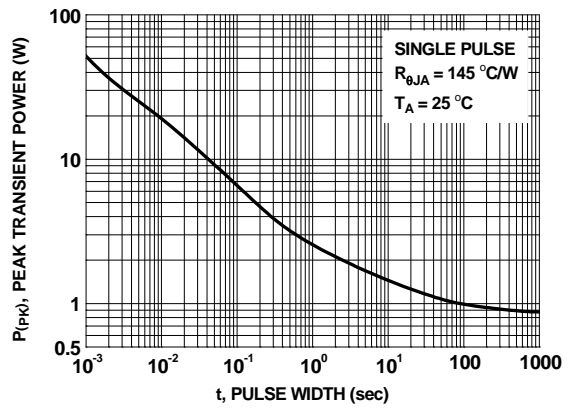
**Figure 7. Gate Charge Characteristics**



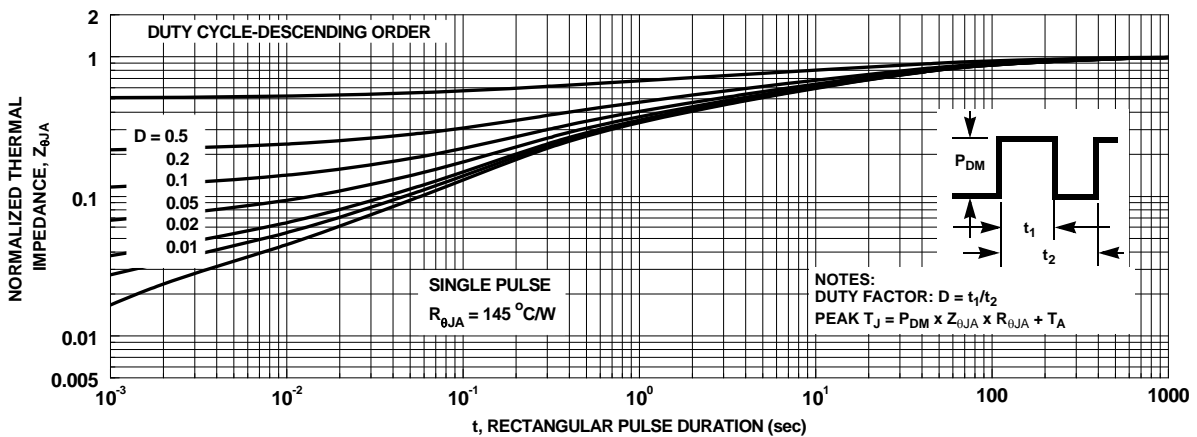
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

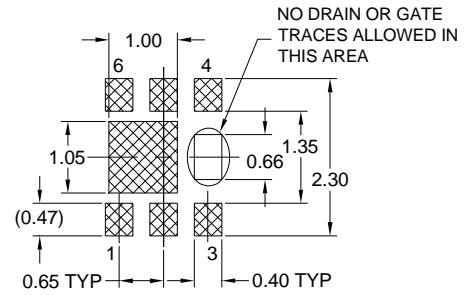
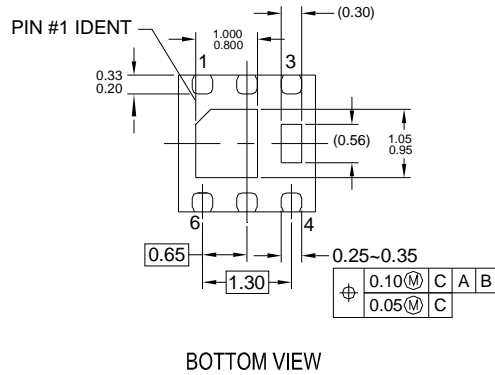
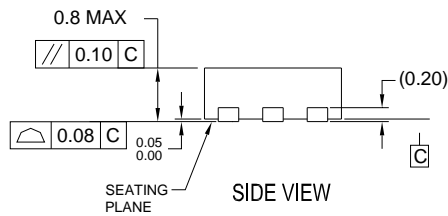
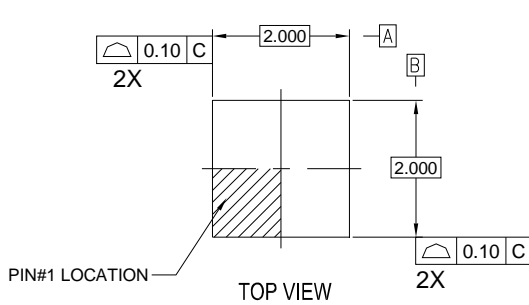


**Figure 10. Single Pulse Maximum Power Dissipation**

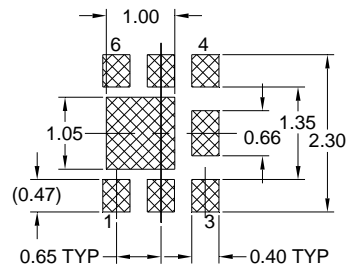


**Figure 11. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

### NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DRAWING FILENAME:



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