

# AKD4421A-SA

## AK4421A Evaluation Board Rev.1

General Description

AKD4421A-SA is an evaluation board for AK4421A (192kHz sampling 24Bit Stereo DAC with 2Vrms Output). AKD4421A-SA has a digital audio interface (AK4115) of Optical input and can easily achieve the interface with digital audio system. Therefore, it is easy to evaluate the sound quality of AK4421A.

■ **Ordering Guide**

AKD4421A-SA ---- AK4421A Evaluation Board

Function

On-board digital audio interface. (AK4115)

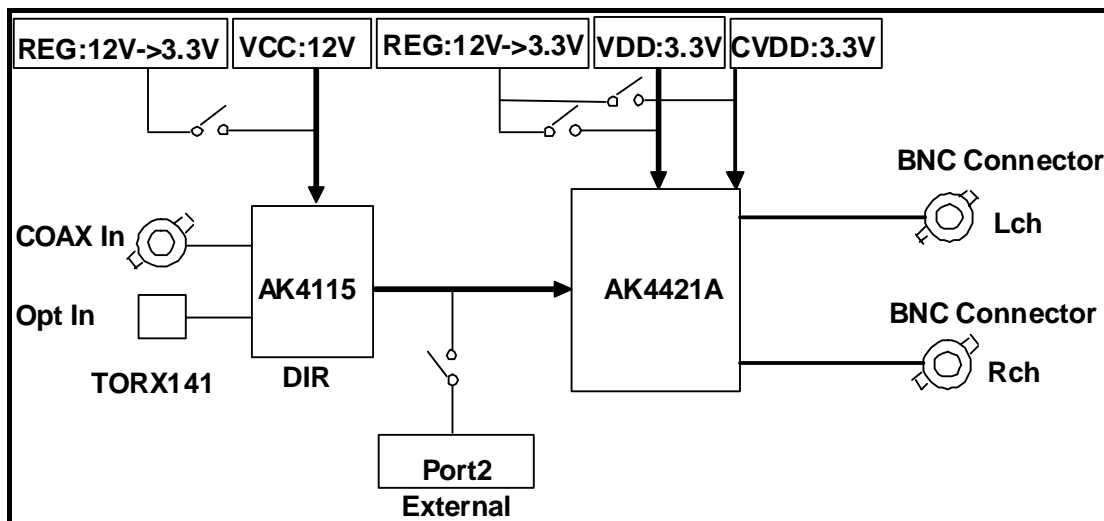


Figure 1. AKD4421A-SA Block diagram  
 (\* Circuit diagram are attached at the end of this manual.)

<b>Board Outline Chart</b>
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■ Outline Chart

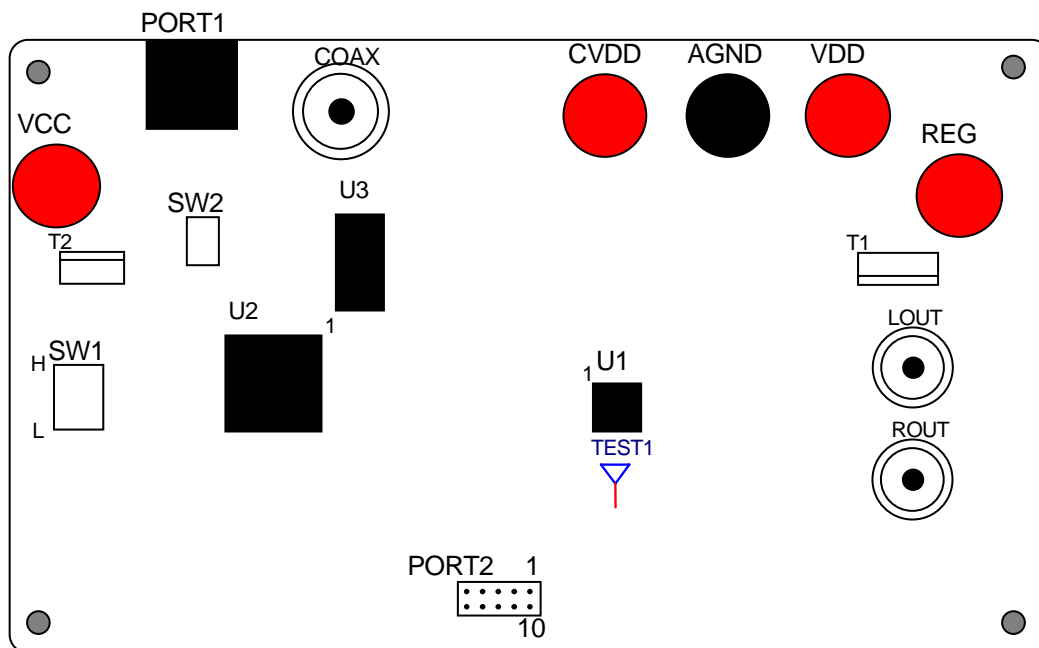


Figure 2. AKD4421A-SA Outline Chart

■ Comment

- (1) LOUT, ROUT (BNC-JACK)  
It is analog signal output Jack. The signal is output from LOUT/ROUT pins.
- (2) COAX, PORT1, PORT2 (Digital signal connector)  
COAX (BNC-JACK): Digital signal (SPDIF, Fs: 24 ~ 48kHz) is input to the AK4115. (Default)  
PORT1 (Optical Connector): Optical digital signal (SPDIF, Fs: 32 ~ 48kHz) is input to the AK4115.  
PORT2 (10 pin header): The clock and data can be input and output with this connector.
- (3) REG, VDD, AGND, CVDD, VCC  
These are the power supply connectors. Connect power supply with these pins.  
As for the detail comments, refer to the setup of power supply in P3.
- (4) SW1, SW2 (Switch)  
SW1: Setting of frequency of MCKO that is output from AK4115.  
SW2: Reset of AK4115. Keep "H" during normal operation.

## ■ Operation sequence

### 1) Set up the power supply lines.

Each supply line should be distributed from the power supply unit.

Name of jack	Color of jack	Typ Voltage	Voltage Range	Using	Default Setting
VCC1 (Note 1)	Red	+12V	+7~+15V	AVDD, DVDD, TVDD, OVDD of AK4115 and VCC of Logic circuit (Regulator:T2)	Connected to +12V
VDD1	Red	+3.3V	+3.0~+3.6V	VDD of AK4421A	Connected to +3.3V
CVDD1	Red	+3.3V	+3.0~+3.6V	CVDD of AK4421A	Connected to +3.3V
AGND2	Black	0V	0V	Ground	Connected to GND (Should be connected)
REG (Note 2)	Red	+12V	+7V~+15V	VDD, CVDD of AK4421A (Regulator:T1)	Open

Table 1.Set up of power supply lines

Note 1 ) In case of using +3.3V power supply to connect VCC1, It is possible to supply the voltage to AK4115 and the Logic circuit without using Regulator.

In this case, change to R36: Open→ Short (0 ); R34,R35: Short (0 ) → Open

Note 2 ) In case of using +12V power supply to connect REG, Use regulator: T1 can supply AK4421A with clean voltage.

In this case, change to R25,R44: Short (0 )→ Open; R37,R43:Open→ Short (0 ); VDD, CVDD should be open.

### 2) DIP Switch setting:

Refer to Table 2 and Table 3

### 3) Power Down:

The AK4115 should be reset once by bringing SW2 (AK4115 PDN) “L” upon power-up.

## ■ Evaluation mode

### 1. Using DIR (Optical Link)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT1: TORX141). It is possible to evaluate the AK4421A by using CD disk.

Setting: R19: Open →470Ω; R33: short (0Ω)→Open

### 2. Using DIR (COAX) (Default)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through BNC connector (J3). It is possible to evaluate the AK4421A by using CD disk.

Setting: R19: Open; R33: short (0Ω); (Default)

\* COAX is recommended for an evaluation of the Sound quality.

### 3. Supply all interface signals that include master clock via PORT2 from external equipments..

Setting: R11: 5.1Ω→Open

R12, R13, R14: 51Ω→Open

R15, R16, R17, R18: Open→51Ω or short (0Ω)

Note) The above work of removing (open) or shorting resistors need to modify the connection by soldering.

### ■ Setting of DIP switch

[SW1]: AK4115 setting

No.	Pin	OFF	ON	Default の状態
1	OCKS1	AK4115's Master Clock setting Look Table 3		ON
2	OCKS0			OFF

Table 2. SW1 setting

OCKS1	OCKS0	MCLK Frequency	Default
0	0/1	256fs @ fs=96kHz	
1	0	512fs @ fs=48kHz	
1	1	128fs @ fs=192kHz	

Table 3. MCLK clock setting

### ■ Setting of SW2 switch

[SW2](PDN): Reset of AK4115. Keep “H” during normal operation.

<b>Measurement Results</b>
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## [Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs (fs=44.1KHz) / 256fs (fs=96KHz) / 128fs (fs=192KHz)
- BICK : 64fs
- fs : 44.1kHz / 96KHz / 192KHz
- Bit : 24bit
- Power Supply : VDD=CVDD=3.3V
- Interface : DIR
- Temperature : Room

**Table Data**

fs=44.1kHz

Parameter	Input signal	Filter condition	Lch	Rch	Unit
S/(N+D)	1kHz, 0dB	20k SPCL	94.6	94.5	dB
DR	1kHz, -60dB	20k SPCL, A-weighted	103.1	103.2	dB
S/N	"0" data	20k SPCL, A-weighted	103.2	103.6	dB

fs=96kHz

Parameter	Input signal	Filter condition	Lch	Rch	Unit
S/(N+D)	1kHz, 0dB	40k SPCL	93.7	94.2	dB
DR	1kHz, -60dB	40k SPCL, A-weighted	103.1	103.3	dB
S/N	"0" data	40k SPCL, A-weighted	103.3	103.5	dB

fs=192kHz

Parameter	Input signal	Filter condition	Lch	Rch	Unit
S/(N+D)	1kHz, 0dB	40k SPCL	93.8	94.1	dB
DR	1kHz, -60dB	40k SPCL, A-weighted	103.1	103.2	dB
S/N	"0" data	40k SPCL, A-weighted	103.3	103.4	dB

Plot Data

fs = 44.1kHz (MCLK=512fs)

AKM

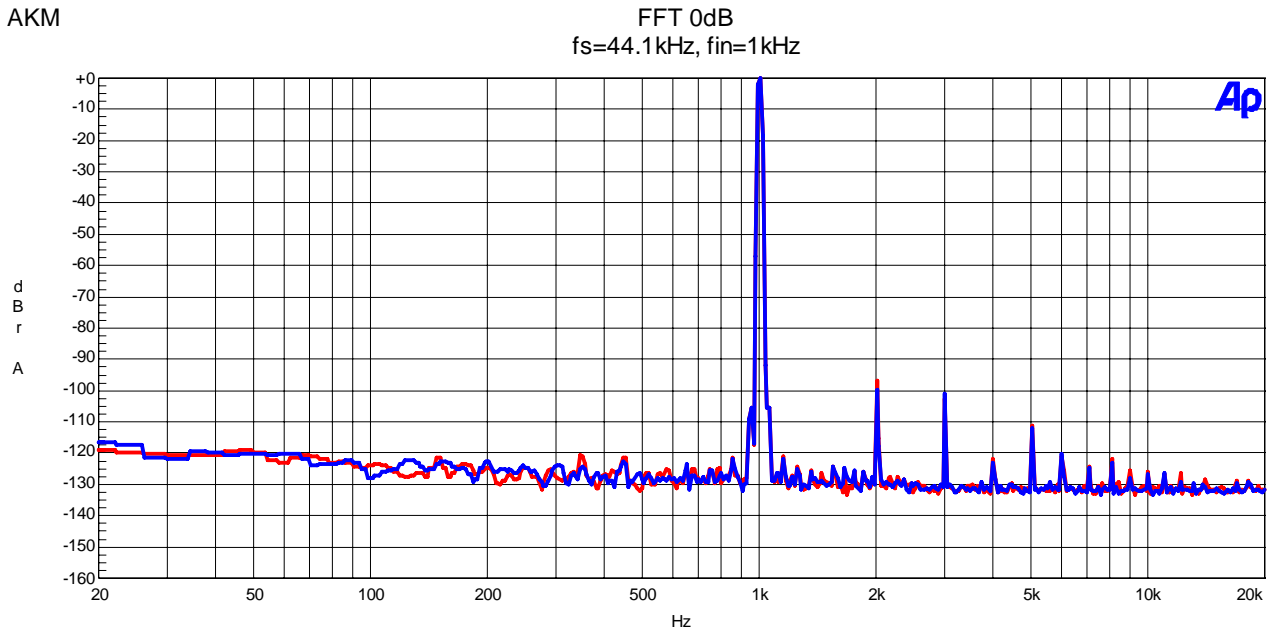


Figure 3 FFT (fin=1kHz, Input Level=0dBFS)

AKM

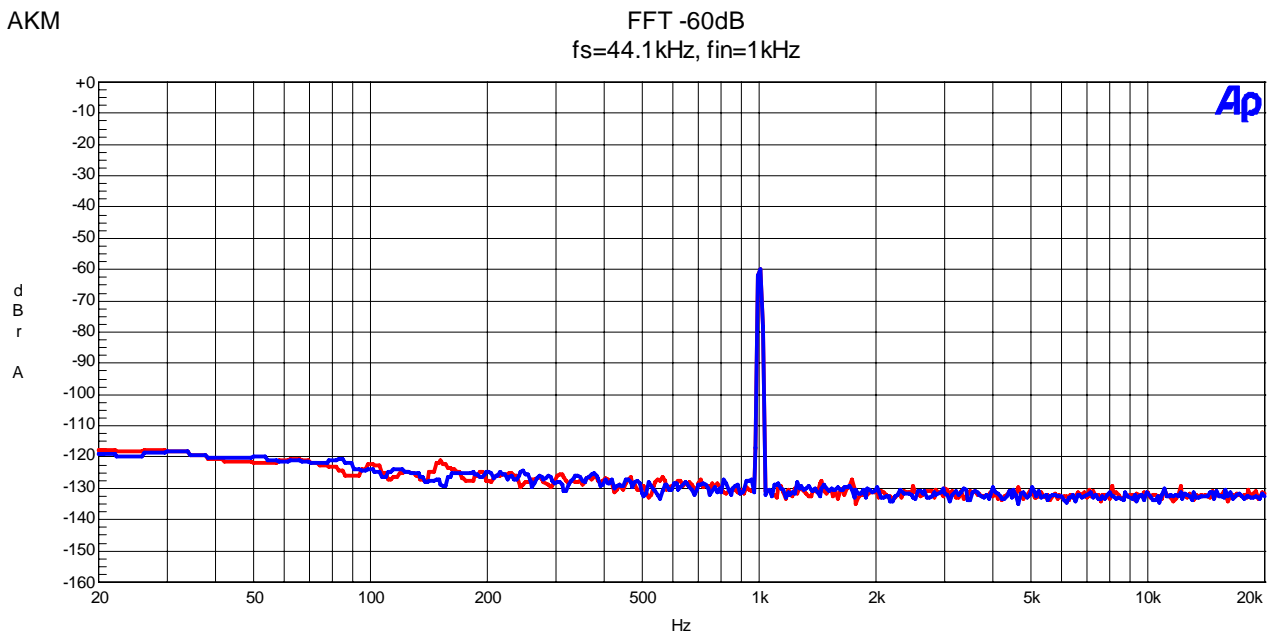


Figure 4 FFT (fin=1kHz, Input Level=-60dBFS)

AKM

FFT No Signal  
fs=44.1kHz

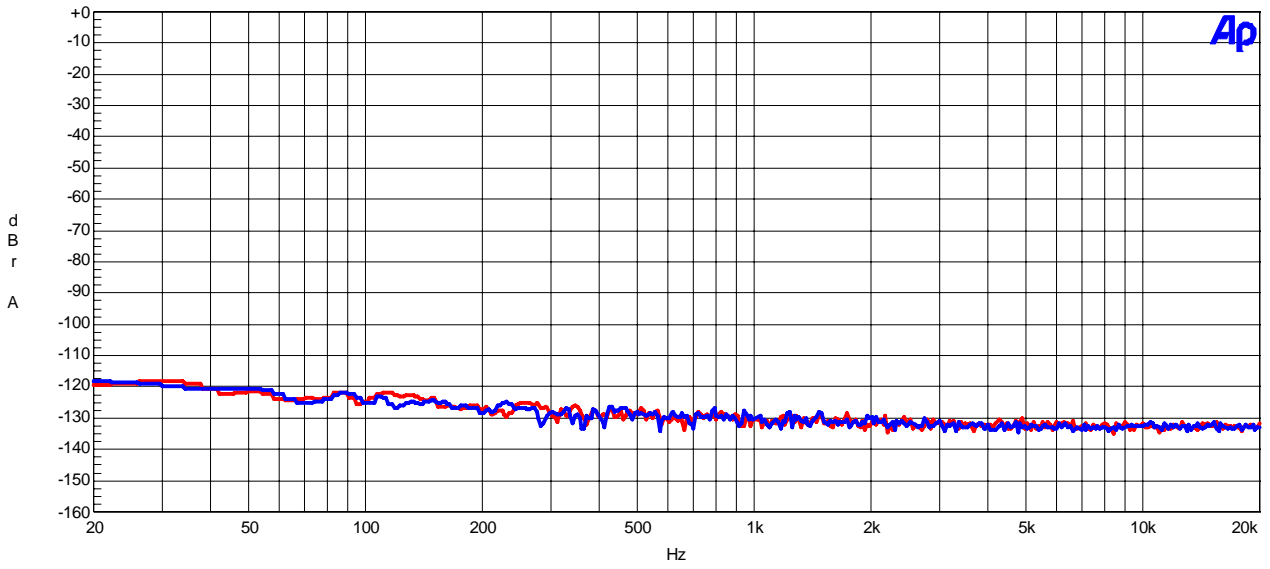


Figure 5 FFT (No Signal)

AKM

FFT Out of Band Noise  
fs=44.1kHz

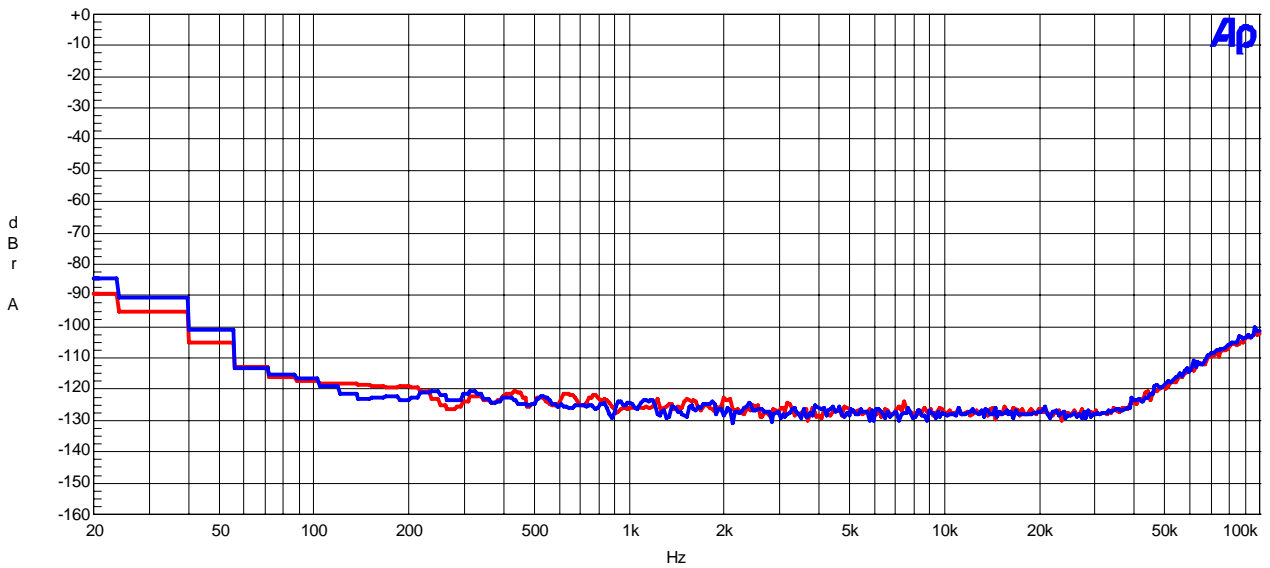


Figure 6 FFT (Out of band noise)

AKM

THD + N vs Input Level  
fs=44.1kHz, fin=1kHz

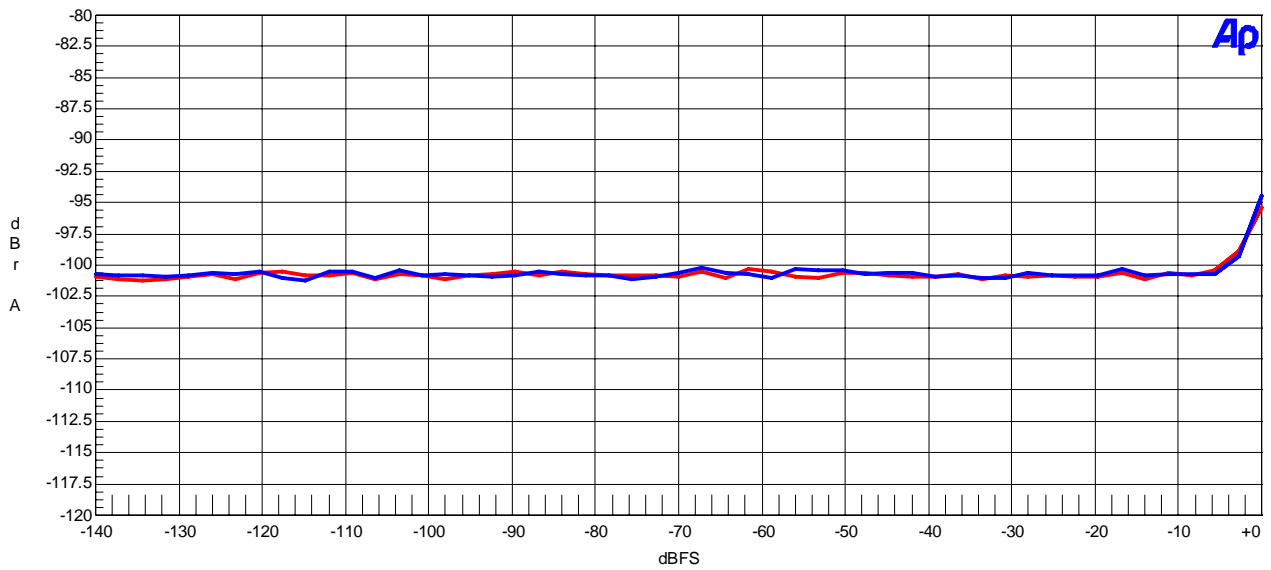


Figure 7 THD+N vs. Input level

AKM

THD + N vs Input Frequency  
fs=44.1kHz, 0dBFS

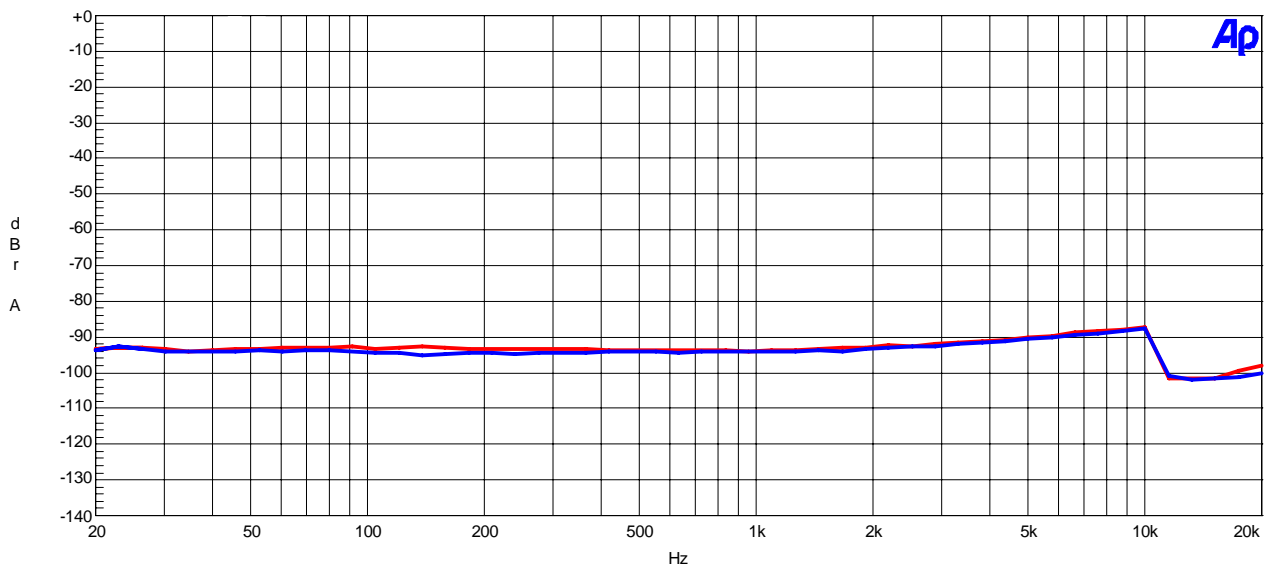


Figure 8 THD+N vs. Input Frequency



AKM

Linearity  
fs=44.1kHz, fin=1kHz

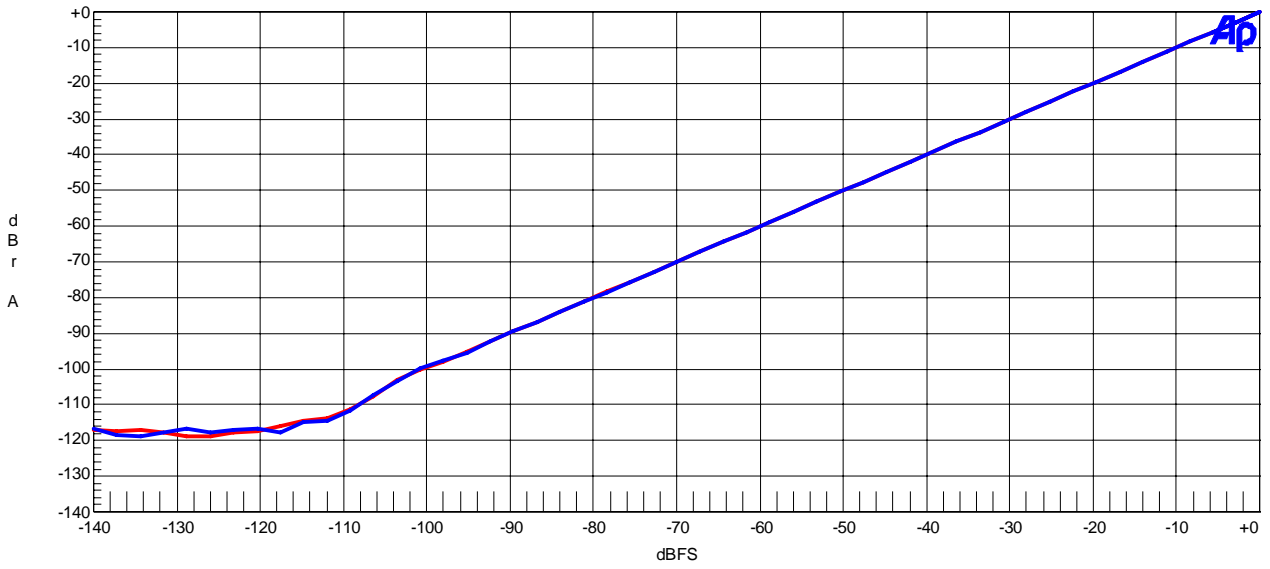


Figure 9 Linearity

AKM

Frequency Response  
fs=44.1kHz, 0dBFS

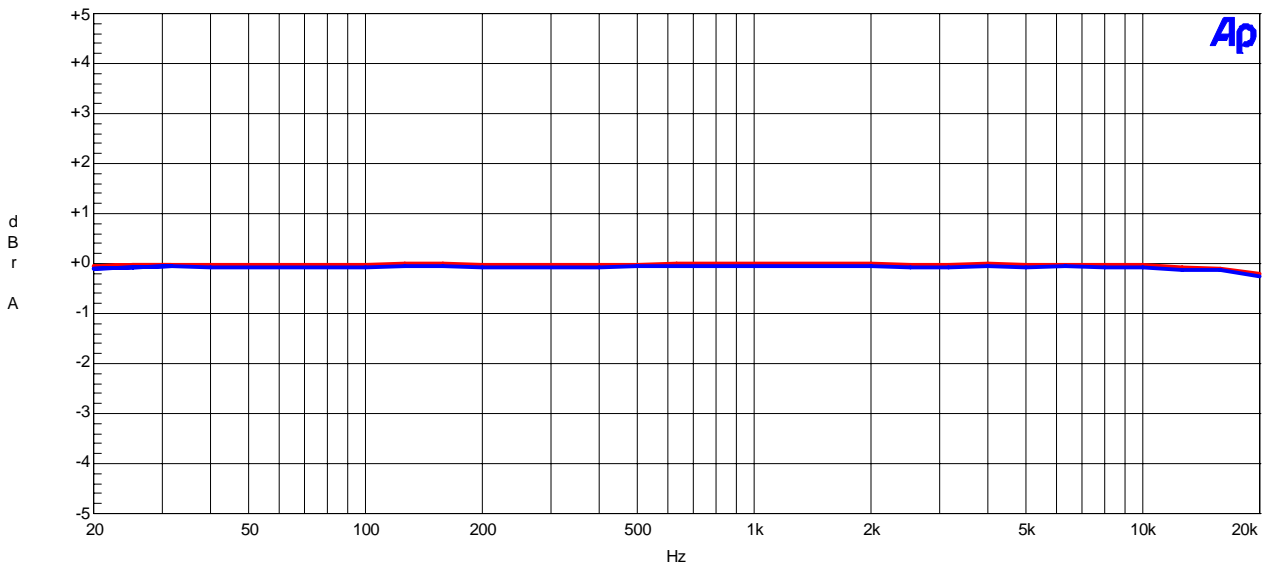


Figure 10 Frequency Response

AKM

Crosstalk  
fs=44.1kHz, 0dBFS

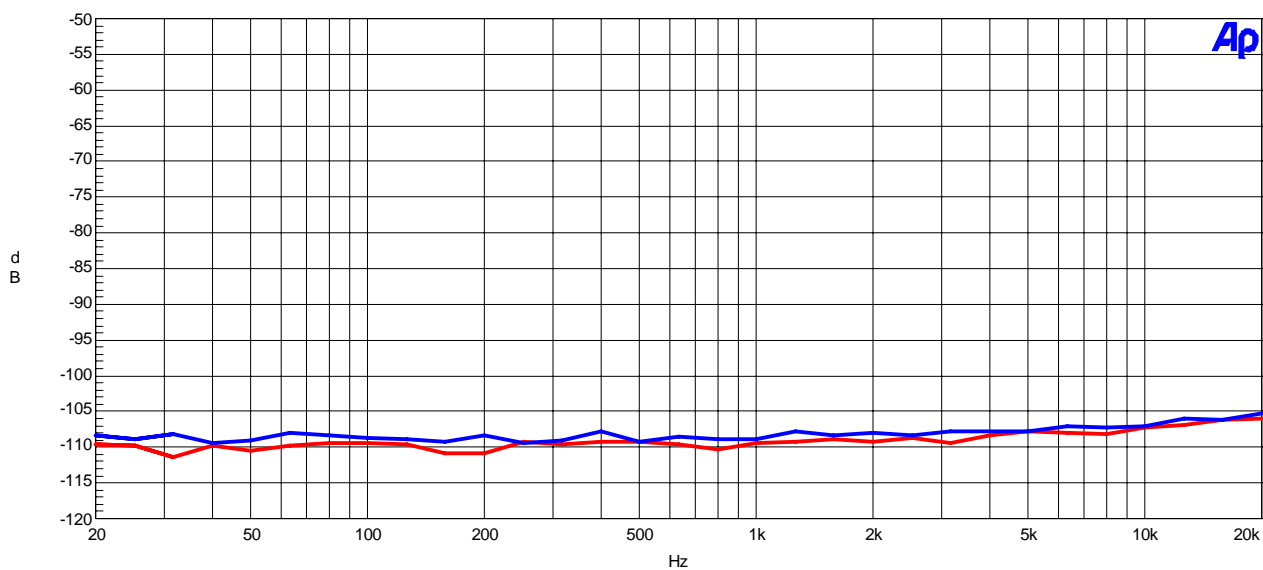


Figure 11 Crosstalk

fs = 96kHz (MCLK=256fs)

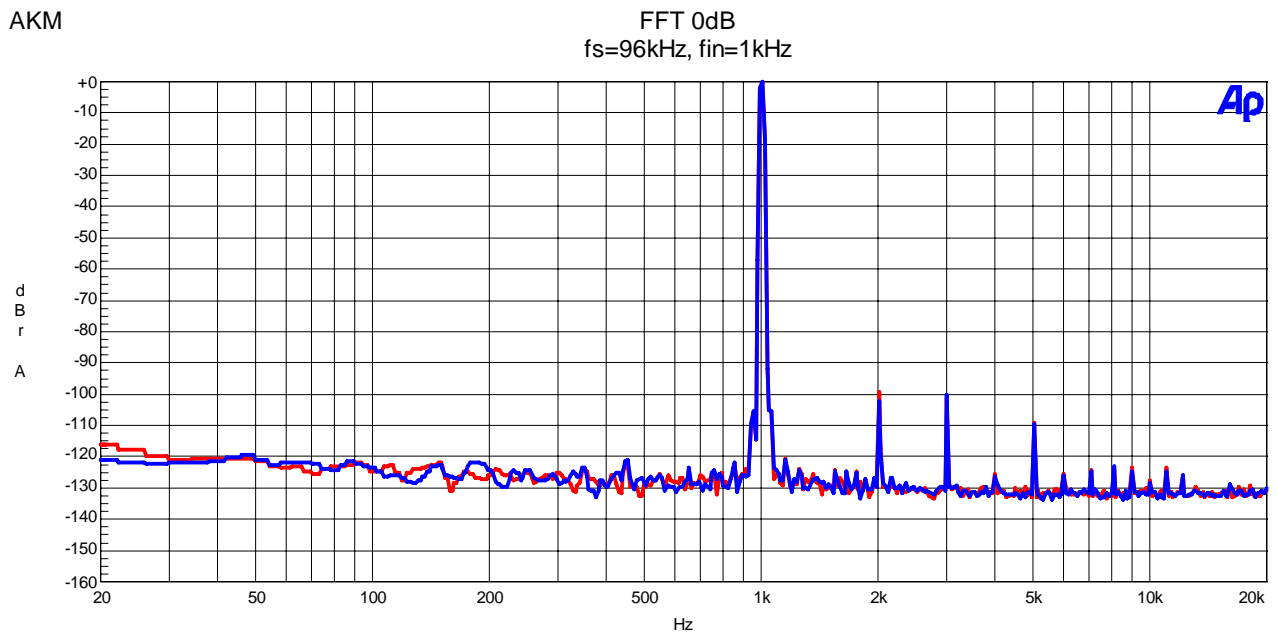


Figure 12 FFT (fin=1kHz, Input Level=0dBFS)

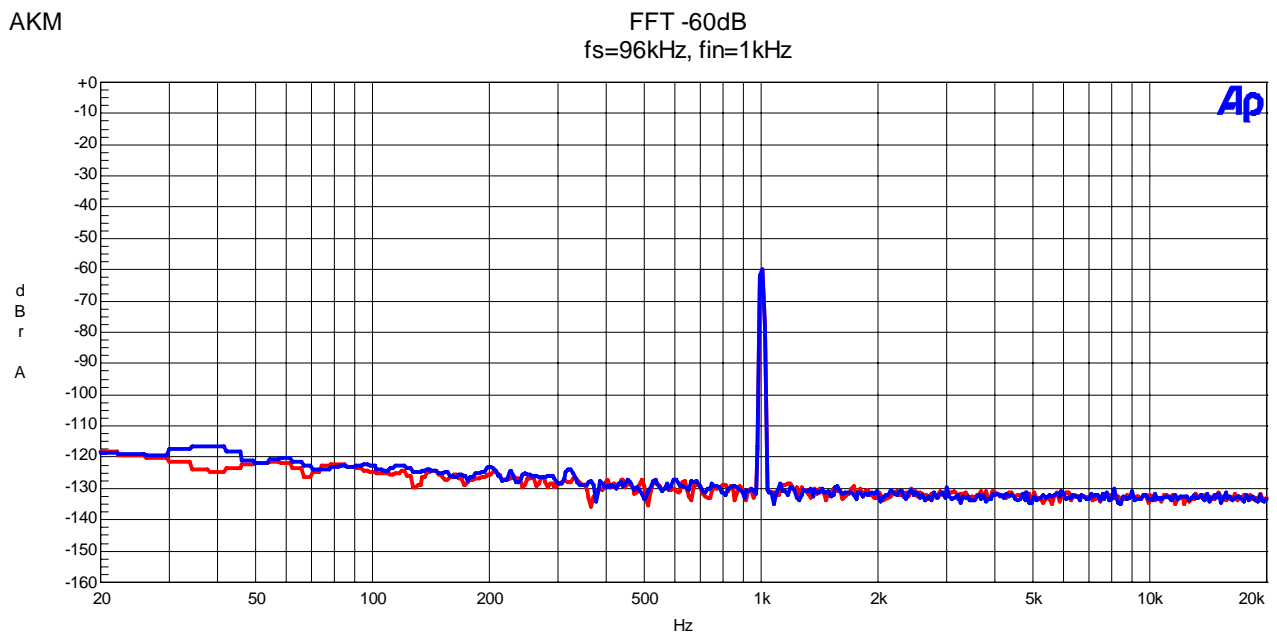


Figure 13 FFT (fin=1kHz, Input Level=-60dBFS)

AKM

FFT No Signal  
fs=96kHz

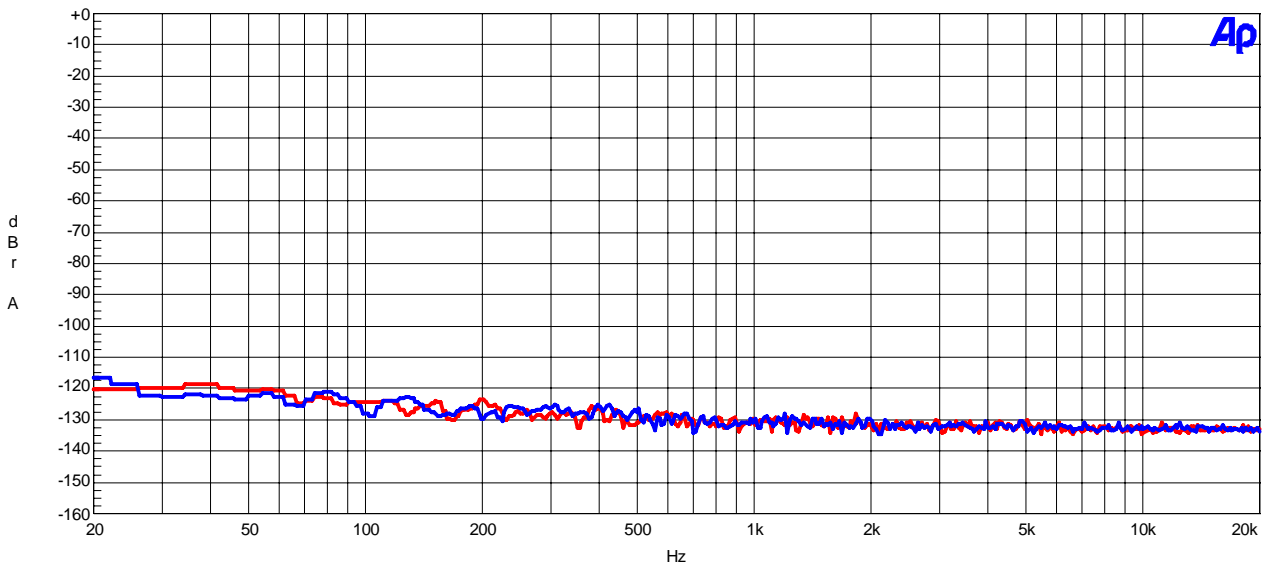


Figure 14 FFT (No Signal)

AKM

FFT Out of Band Noise  
fs=96kHz

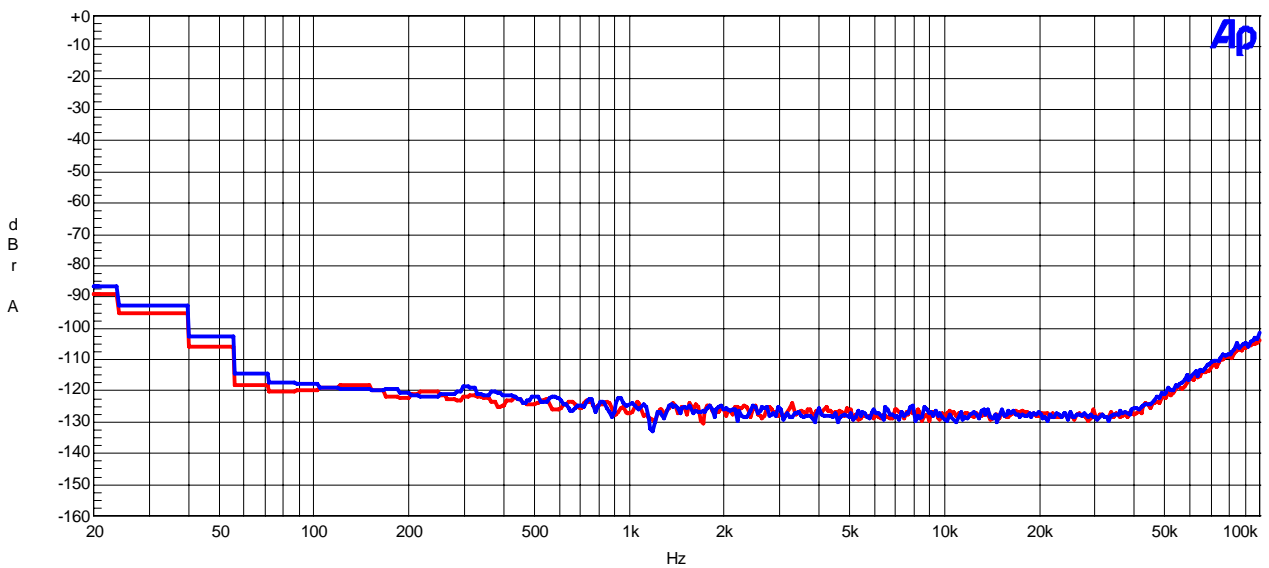


Figure 15 FFT (Out of band noise)

AKM

THD + N vs Input Level  
fs=96kHz, fin=1kHz

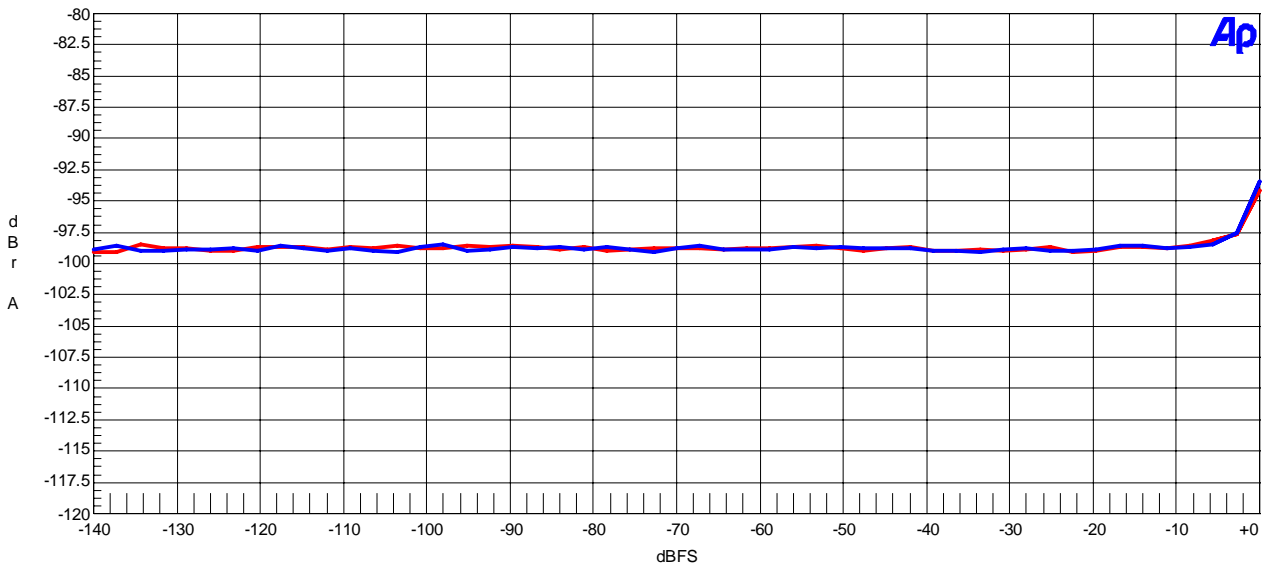


Figure 16 THD+N vs. Input level

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THD + N vs Input Frequency  
fs=96kHz, 0dBFS

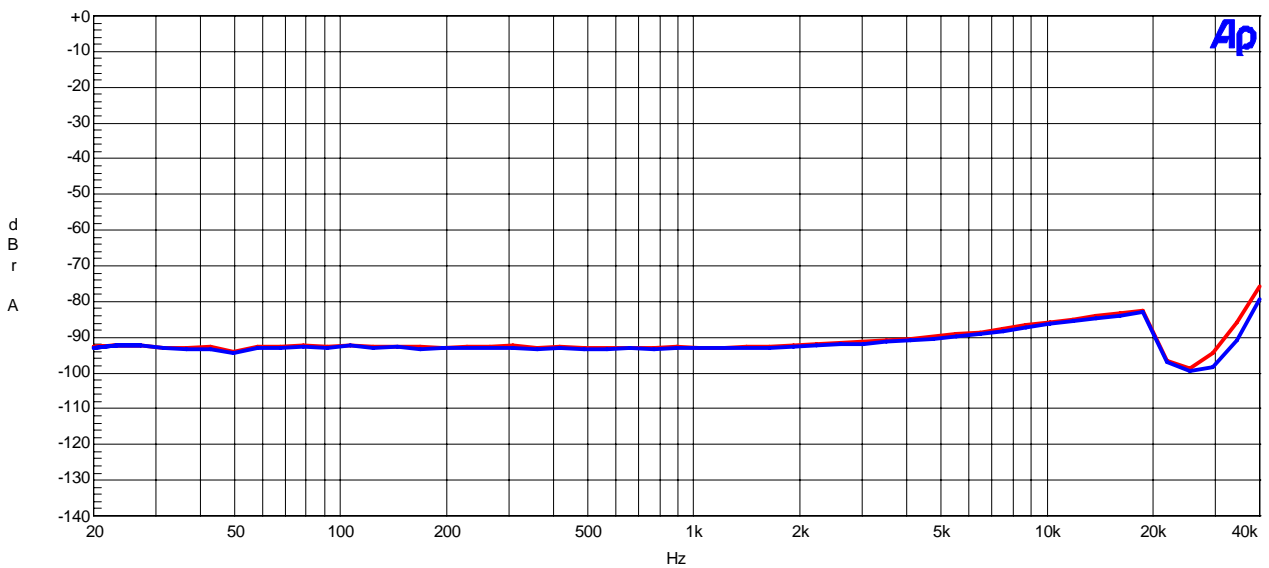


Figure 17 THD+N vs. Input Frequency

AKM

Linearity  
fs=96kHz, fin=1kHz

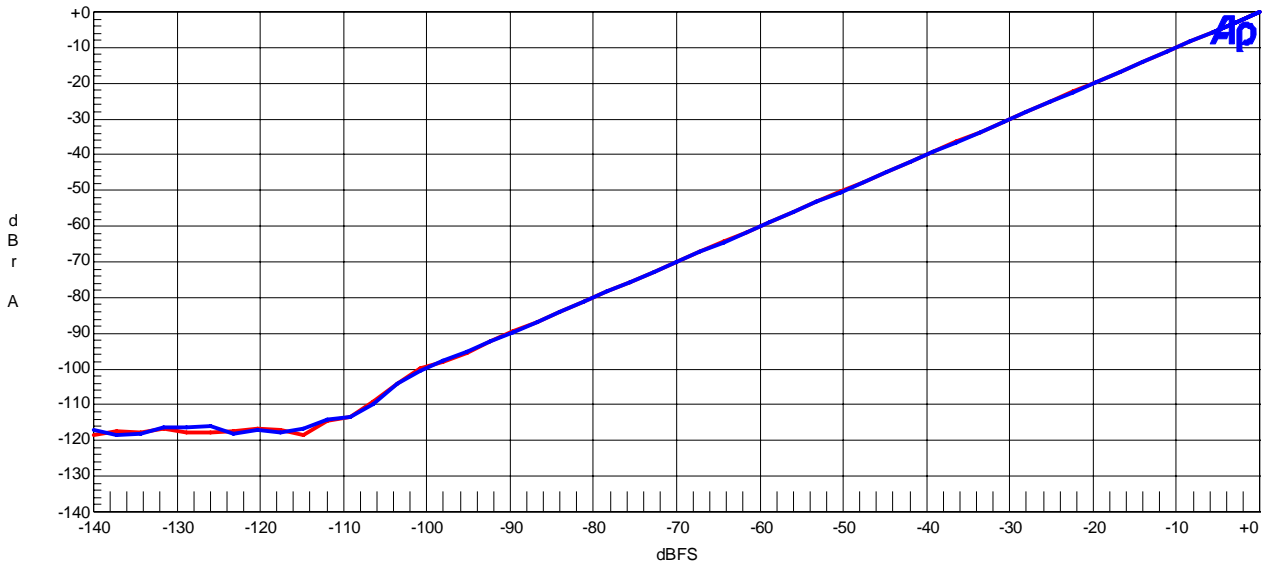


Figure 18 Linearity

AKM

Frequency Response  
fs=96kHz, 0dBFS

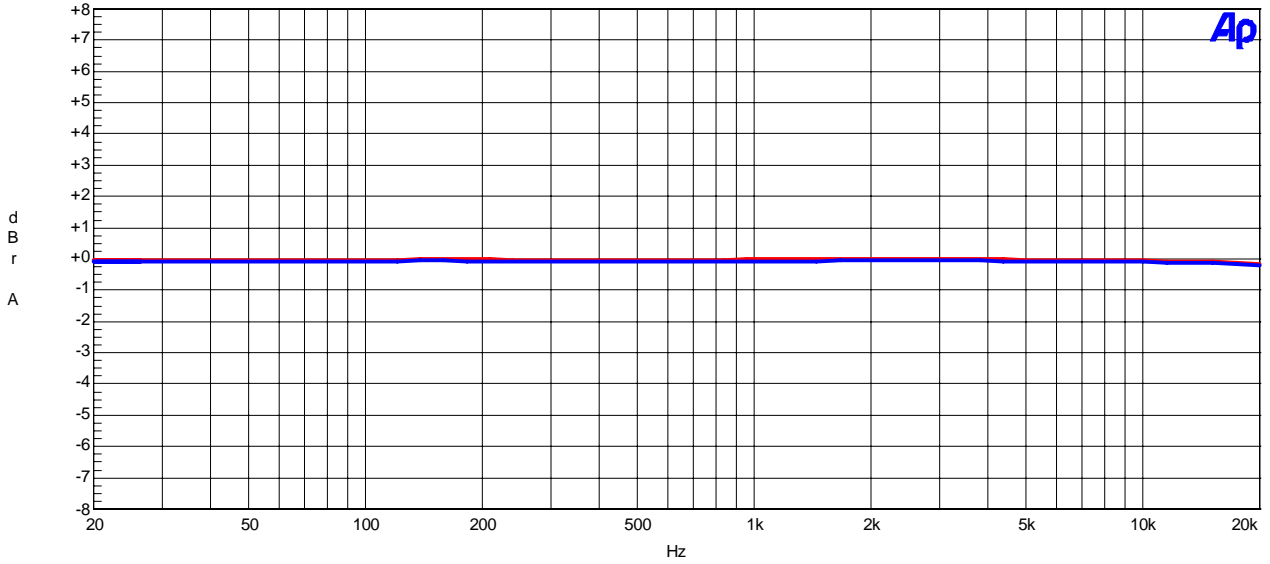


Figure 19 Frequency Response

AKM

Crosstalk  
fs=96kHz, 0dBFS

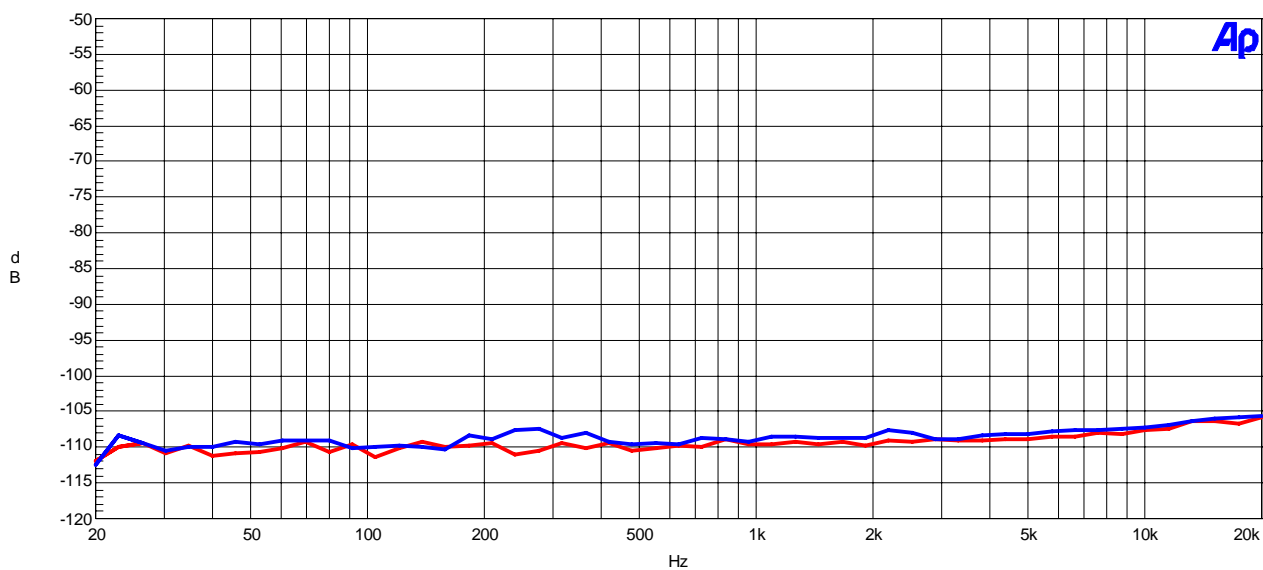


Figure 20 Crosstalk

fs = 192kHz (MCLK=128fs)

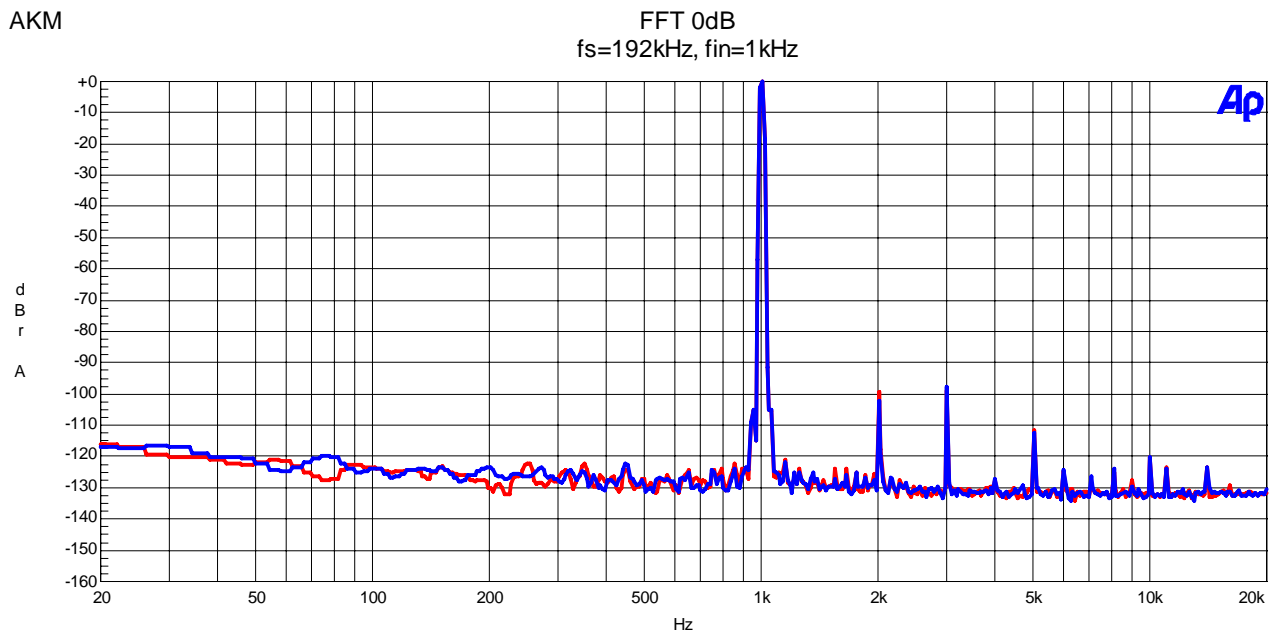


Figure 21 FFT (fin=1kHz, Input Level=0dBFS)

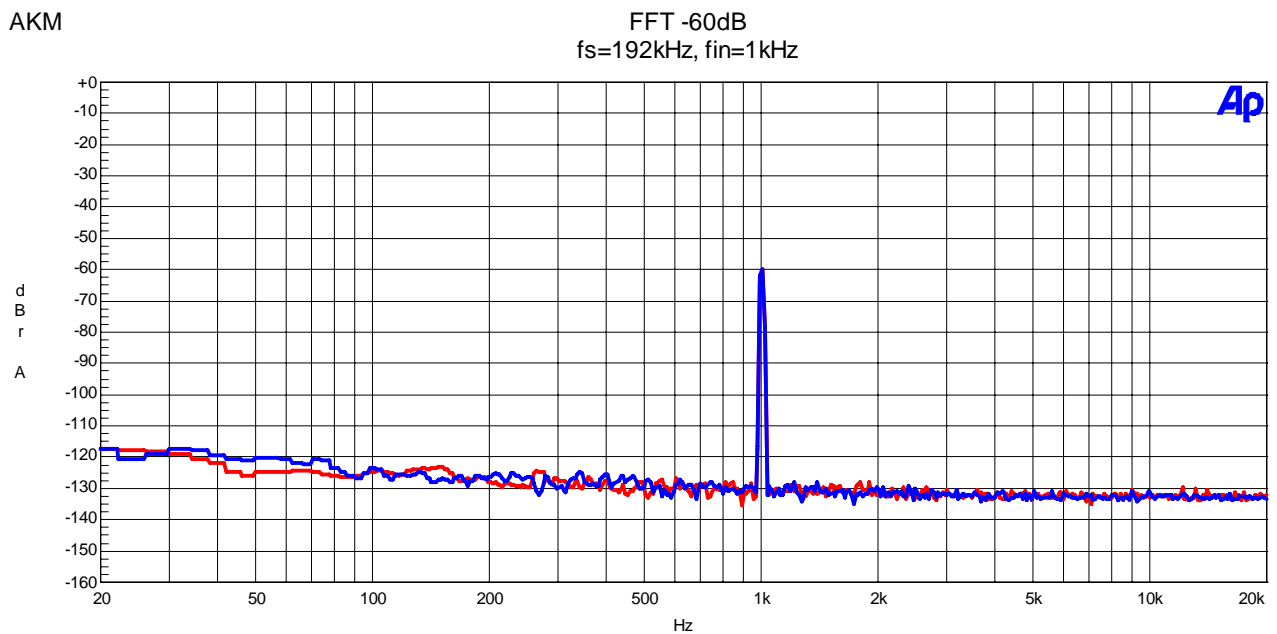


Figure 22 FFT (fin=1kHz, Input Level=-60dBFS)



AKM

FFT No Signal  
fs=192kHz

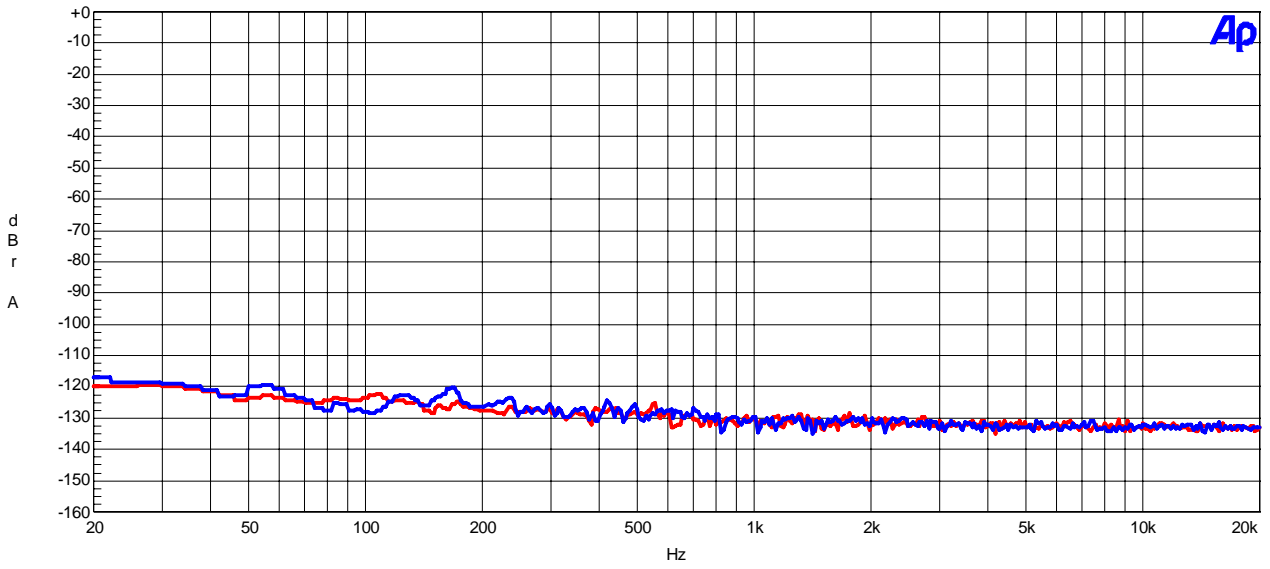


Figure 23 FFT (No Signal)

AKM

FFT Out of Band Noise  
fs=192kHz

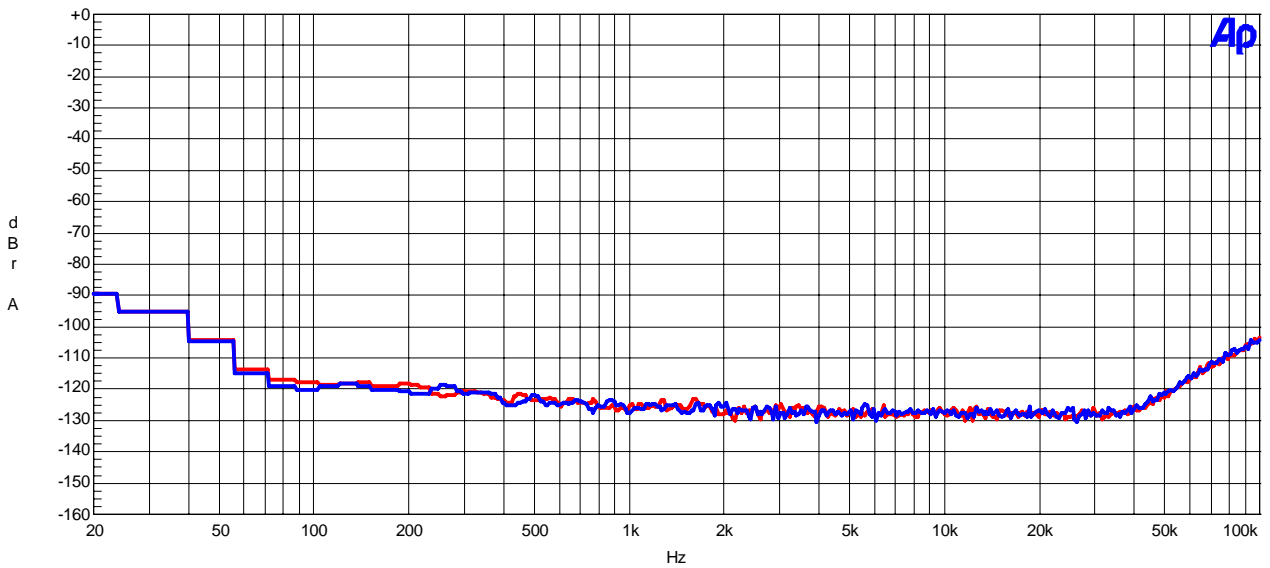


Figure 24 FFT (Out of band noise)

AKM

THD + N vs Input Level  
fs=192kHz, fin=1kHz

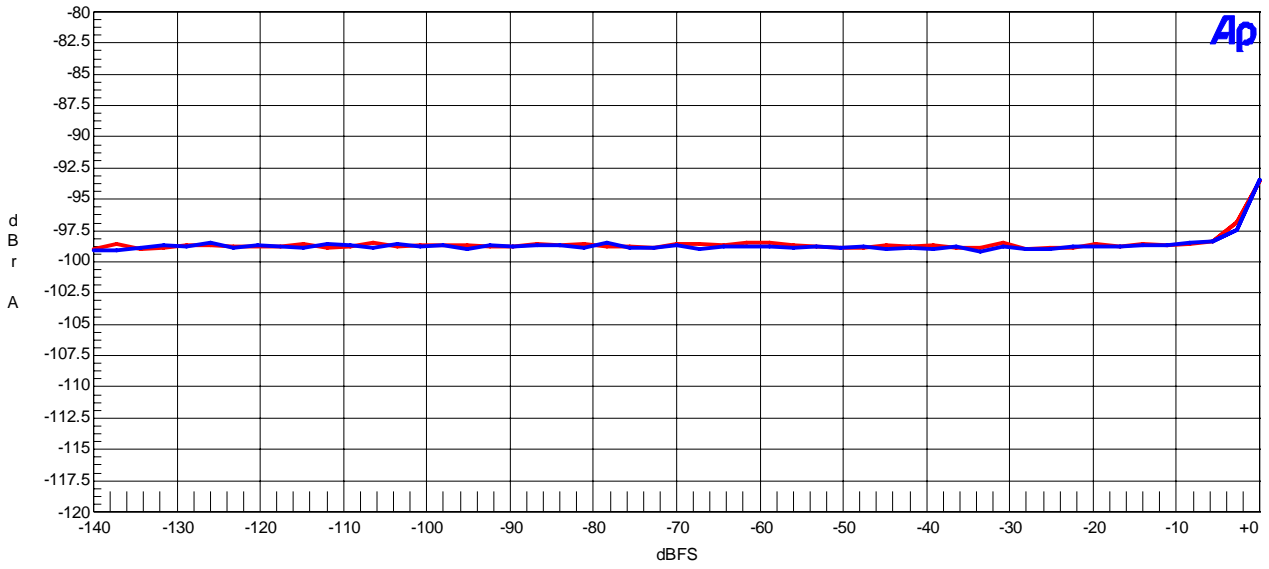


Figure 25 THD+N vs. Input level

AKM

THD + N vs Input Frequency  
fs=192kHz, 0dBFS

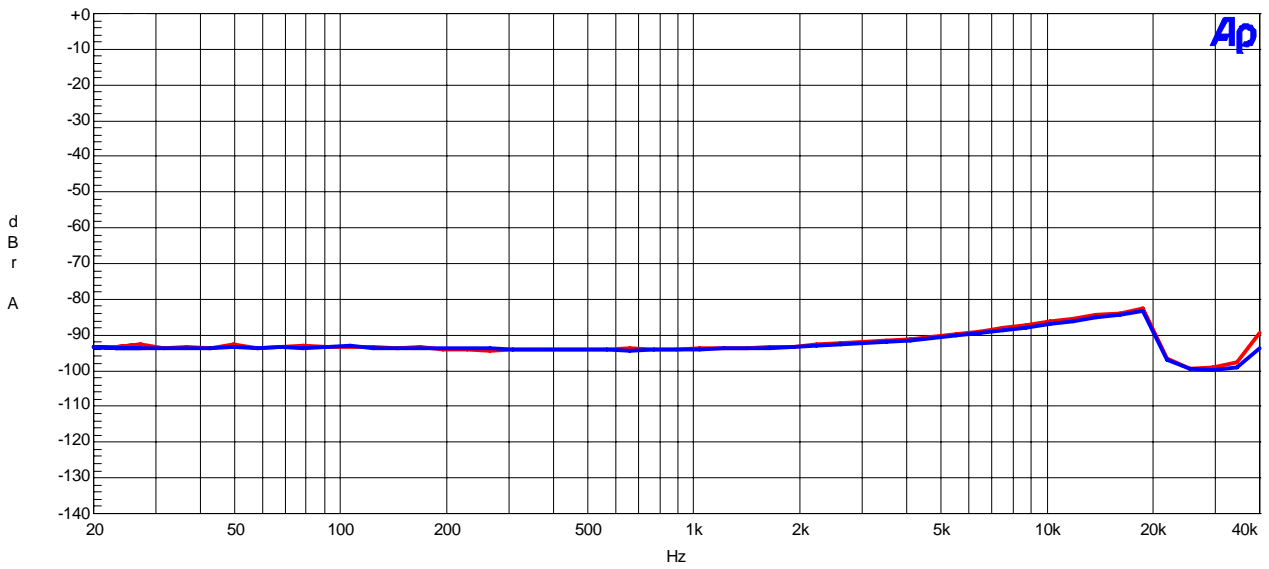


Figure 26 THD+N vs. Input Frequency

AKM

Linearity  
fs=192kHz, fin=1kHz

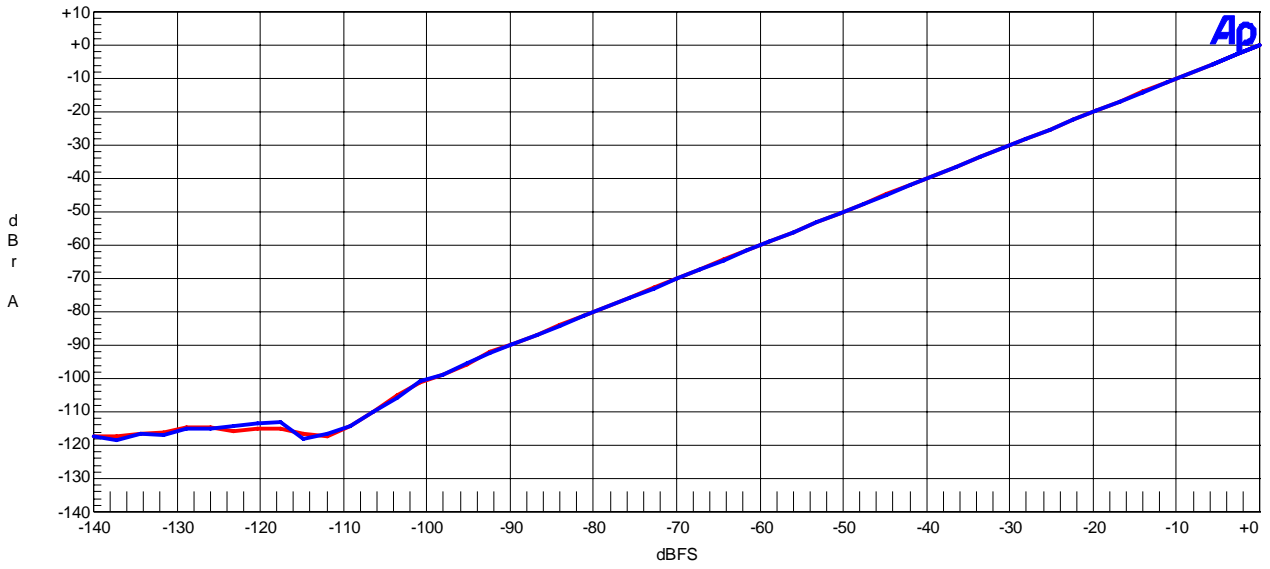


Figure 27 Linearity

AKM

Frequency Response  
fs=192kHz, 0dBFS

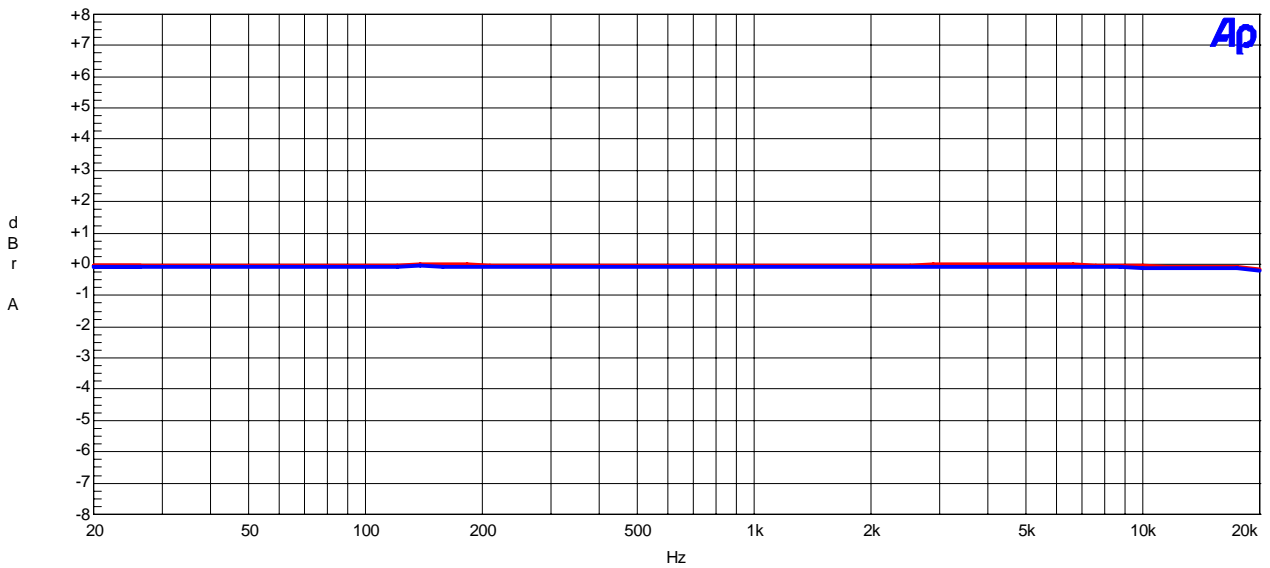


Figure 28 Frequency Response

AKM

Crosstalk  
fs=192kHz, 0dBFS

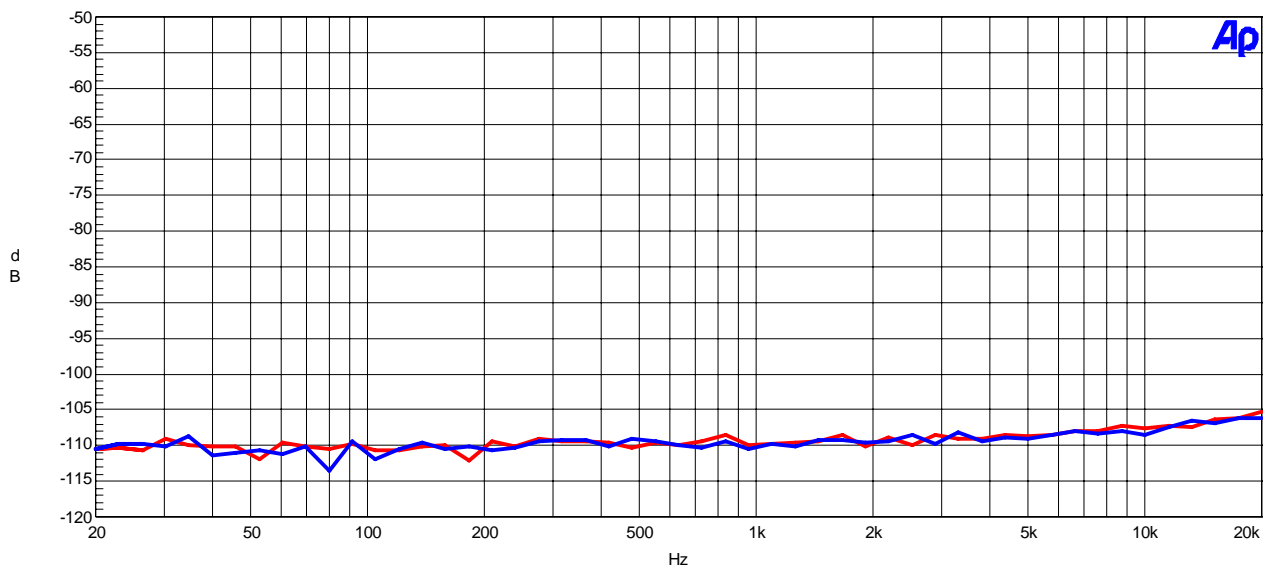


Figure 29 Crosstalk

<b>REVISION HISTORY</b>
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Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
09/02/06	KM098700	0	First Edition		
09/04/23	KM098701	1	Change	22	Circuit diagram were changed. C1, C2 : 1uF → 2.2uF
			Change	5-20	Table data and Plot data were updated.

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