PB51 • PB51A

FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- HIGH OUTPUT CURRENT — 1.5A Continuous (PB51), 2.0A Continuous (PB51A)
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW — 50V/µs Minimum (PB51) 75V/µs Minimum (PB51A)
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 320 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical
- EVALUATION KIT — EK29

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 280V P-P

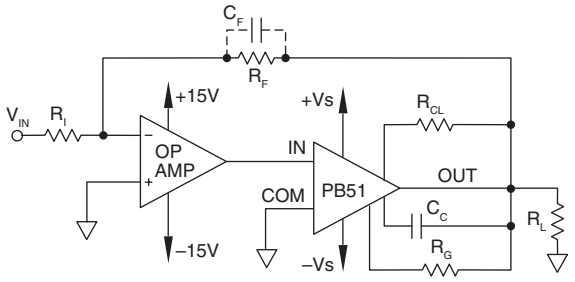
DESCRIPTION

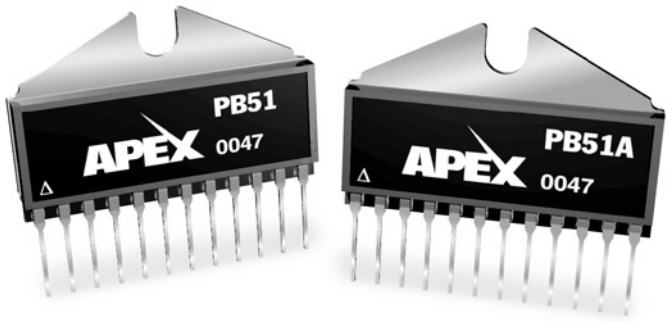
The PB51 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB51 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating second breakdown limitations imposed by Bipolar Transistors. Internal feedback and gainset resistors are provided for a pin-strapable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12-pin Power SIP package is electrically isolated.

TYPICAL APPLICATION

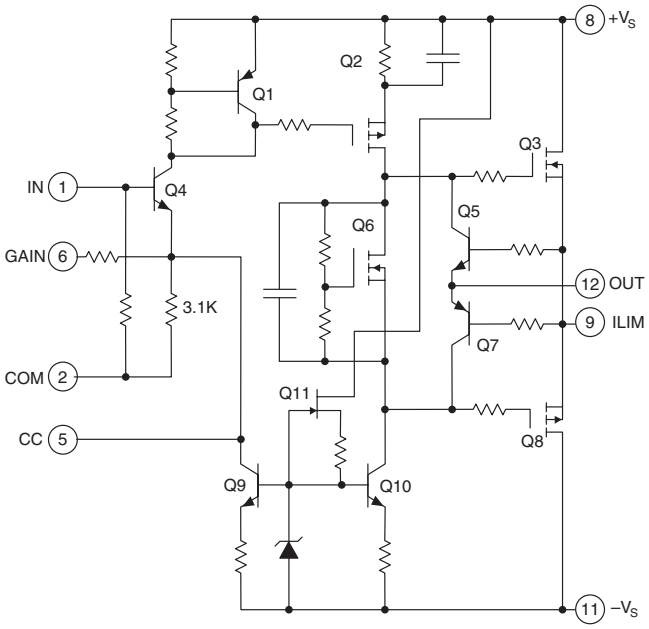




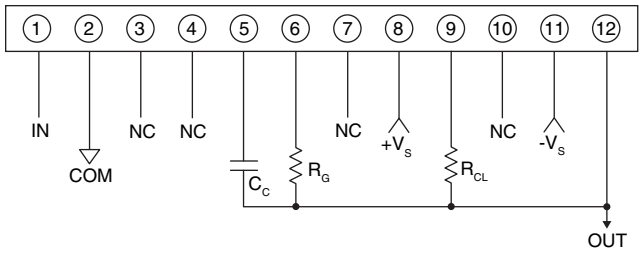
12-PIN SIP
PACKAGE STYLE DP

Formed leads available. See package styles ED & EE

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	2.0A
POWER DISSIPATION, internal at T_C = 25°C[1]	83W
INPUT VOLTAGE, referred to COM	±15V
TEMPERATURE, pin solder—10s max.	260°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE RANGE, storage	–40 to +85°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C

SPECIFICATIONS

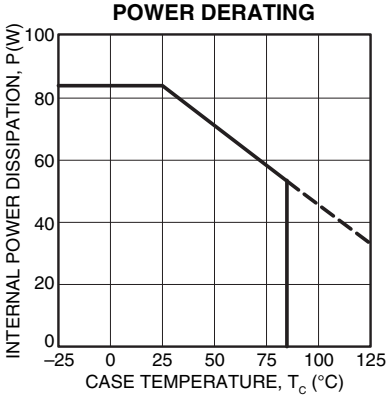
PARAMETER	TEST CONDITIONS[2]	PB51 MIN	PB51 TYP	PB51 MAX	PB51A MIN	PB51A TYP	PB51A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			±.75	±1.75		*	±1.0	V
OFFSET VOLTAGE, vs. temperature	Full temperature range[3]		–4.5	–7		*	*	mV/°C
INPUT IMPEDANCE, DC		25	50		*	*		k
INPUT CAPACITANCE			3			*		pF
CLOSED LOOP GAIN RANGE		3	10	25	*	*	*	V/V
GAIN ACCURACY, internal Rg, Rf	AV = 3		±10	±15		*	*	%
GAIN ACCURACY, external Rf	AV = 10		±15	±25		*	*	%
PHASE SHIFT	f = 10kHz, AVC_L = 10, CC = 22pF		10			*		°
	f = 200kHz, AVC_L = 10, CC = 22pF		60			*		°
OUTPUT								
VOLTAGE SWING	Io = 1.5A (PB58), 2A (PB58A)	VS–11	VS–8		VS–15	VS–11		V
VOLTAGE SWING	Io = 1A	VS–10	VS–7		*	*		V
VOLTAGE SWING	Io = .1A	VS–8	VS–5		*	*		V
CURRENT, continuous		1.5			2.0			A
SLEW RATE	Full temperature range	50	100		75	*		V/µs
CAPACITIVE LOAD	Full temperature range		2200			*		pF
SETTLING TIME to .1%	RL = 100, 2V step		2			*		µs
POWER BANDWIDTH	VC = 100 Vpp	160	320		240	*		kHz
SMALL SIGNAL BANDWIDTH	CC = 22pF, AV = 25, Vcc = ±100		100			*		kHz
SMALL SIGNAL BANDWIDTH	CC = 22pF, AV = 3, Vcc = ±30		1			*		MHz
POWER SUPPLY								
VOLTAGE, ±VS[4]	Full temperature range	±15[6]	±60	±150	*	*	*	V
CURRENT, quiescent	VS = ±15		11			*		mA
	VS = ±60		12			*		mA
	VS = ±150		14	18		*	*	mA
THERMAL								
RESISTANCE, AC junction to case5	Full temp. range, f > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	*	*	*	°C

NOTES: * The specification of PB51A is identical to the specification for PB51 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, T_C = 25°C unless otherwise noted.
3. Guaranteed by design but not tested.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. $+V_S/-V_S$ must be at least 15V above/below COM.

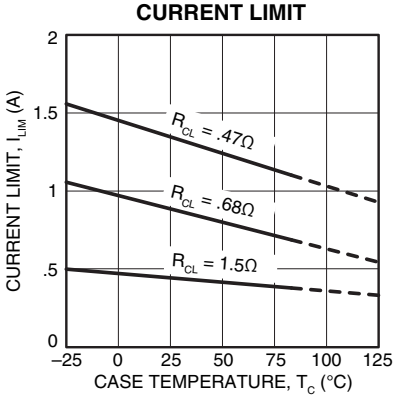
CAUTION The PB51 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

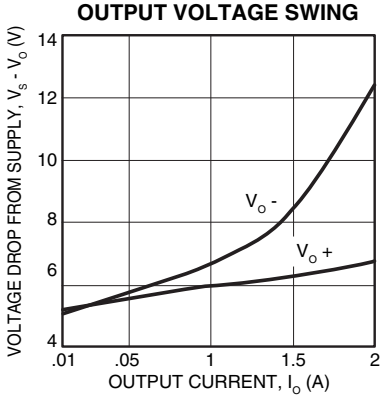
POWER DERATING



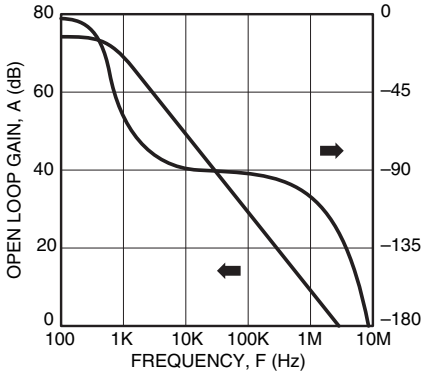
CURRENT LIMIT



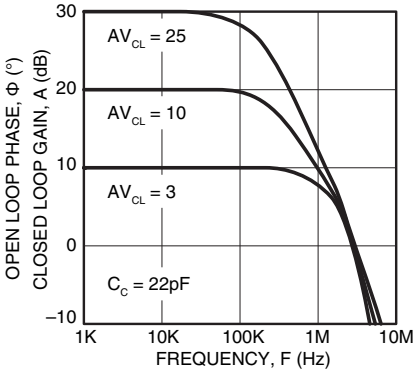
OUTPUT VOLTAGE SWING



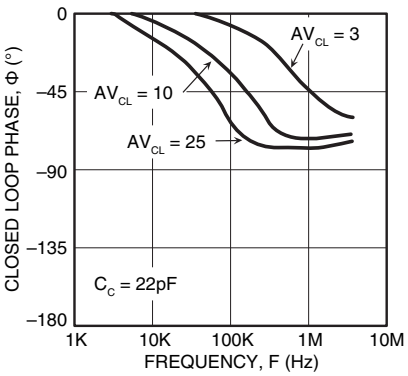
SMALL SIGNAL RESPONSE



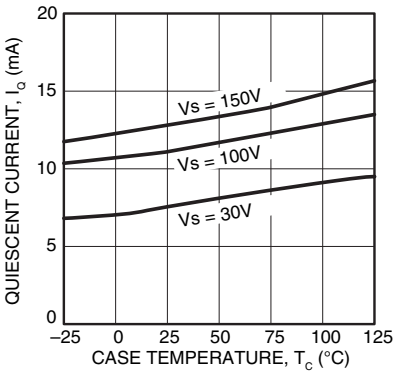
SMALL SIGNAL RESPONSE



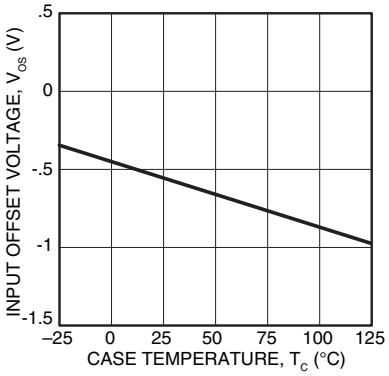
SMALL SIGNAL RESPONSE



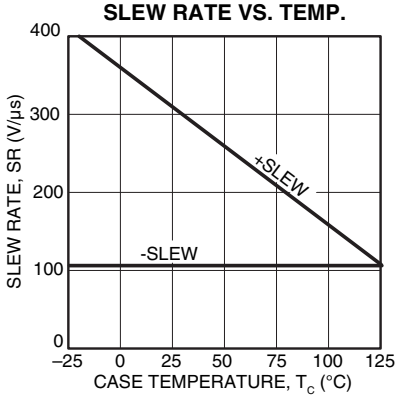
QUIESCENT CURRENT



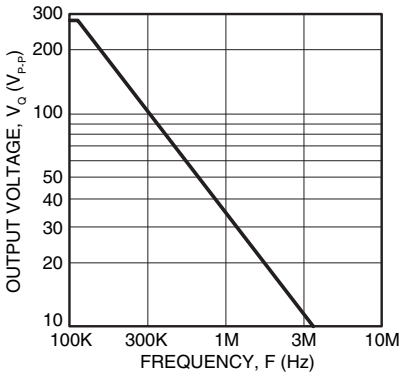
INPUT OFFSET VOLTAGE



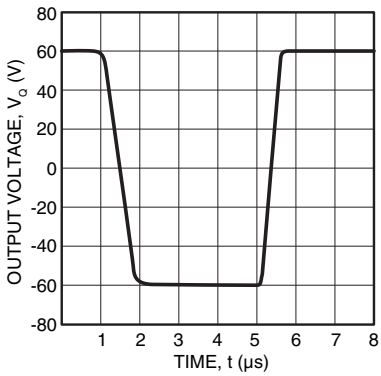
SLEW RATE VS. TEMP.



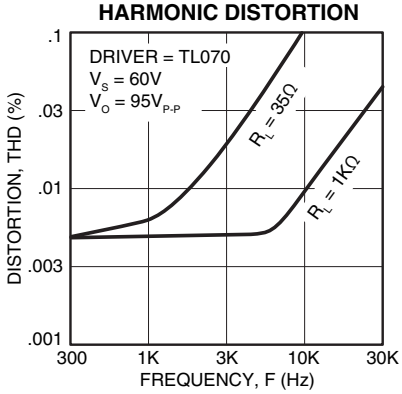
POWER RESPONSE



PULSE RESPONSE



HARMONIC DISTORTION



GENERAL

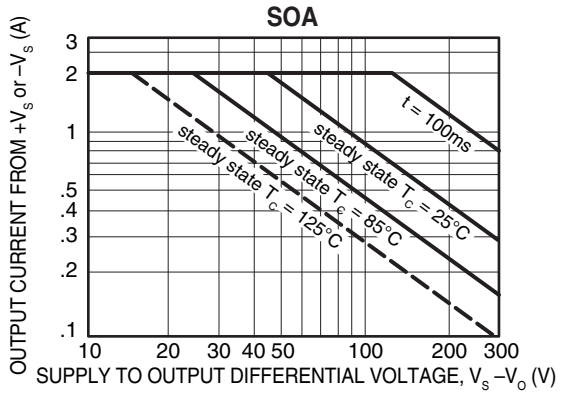
Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.33 with a maximum practical value of 47. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows:

$+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.

SAFE OPERATING AREA



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [(Av\text{-}1) \bullet 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with
R i = 2K, R f = 60K, R g = 0 :
Av (booster) = (6.2K/3.1K) + 1 = 3
Av (composite) = 60K/2K = – 30
Av (driver) = – 30/3 = –10

STABILITY

Stability can be maximized by observing the following guidelines:

1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60
For: R_F = 33K, R_I = 3.3K, R_G = 22K					

TABLE 1.TYPICAL VALUES FOR CASE WHERE OP AMP EFFECTIVE GAIN = 1.

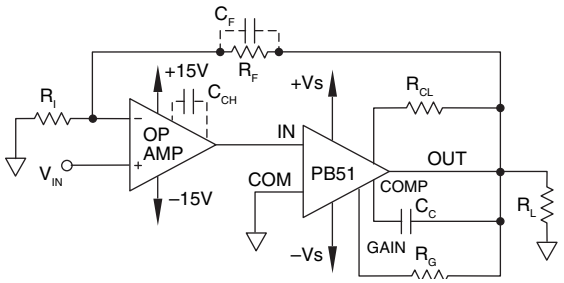


FIGURE 2. NON-INVERTING COMPOSITE AMPLIFIER.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

This data sheet has been carefully checked and is believed to be reliable, however, no responsibility is assumed for possible inaccuracies or omissions. All specifications are subject to change without notice.

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