

## General Description

This planar stripe MOSFET has better characteristics, such as fast switching time, fast reverse recovery time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for active power factor correction and switching mode power supplies.

## FEATURES

- $V_{DSS}=500V$ ,  $I_D=10A$
- Drain-Source ON Resistance :  
 $R_{DS(ON)}(Max)=0.65 \Omega$  @  $V_{GS}=10V$
- $Qg(typ.)= 19.5nC$
- $t_{rr}(typ) = 170ns$

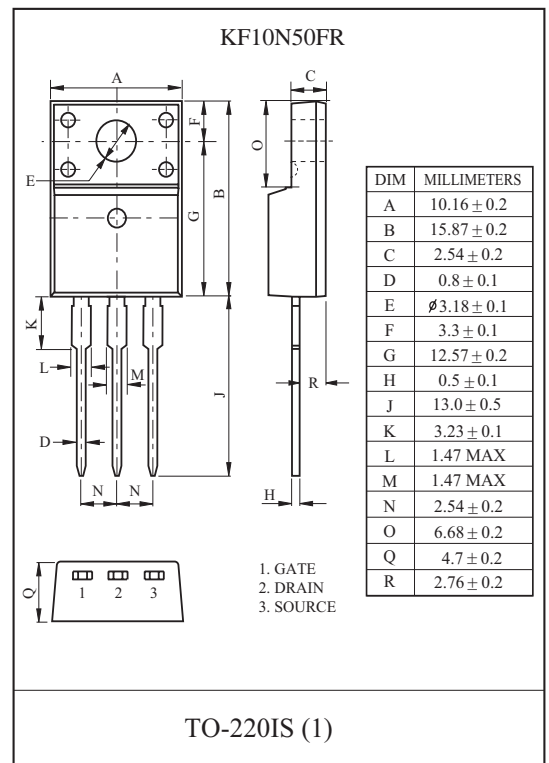
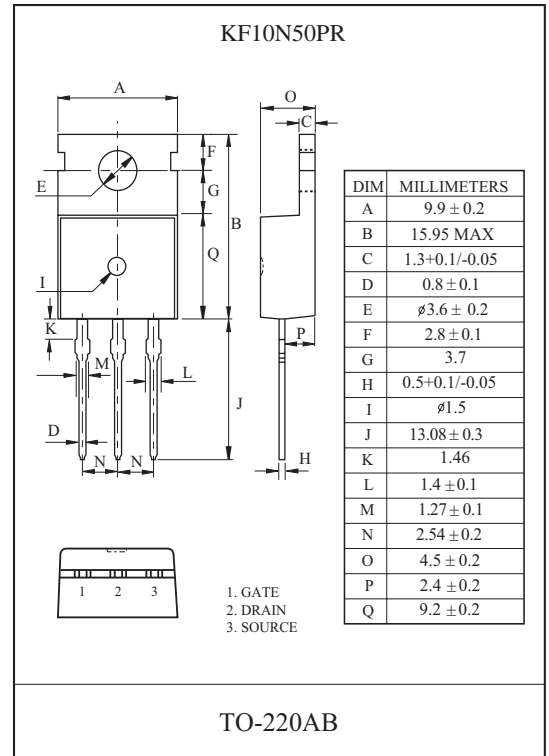
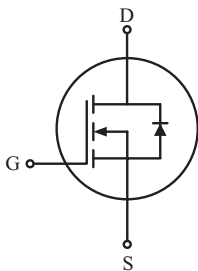
## MAXIMUM RATING (Tc=25 °C)

CHARACTERISTIC	SYMBOL	RATING		UNIT	
		KF10N50PR	KF10N50FR		
Drain-Source Voltage	$V_{DSS}$	500		V	
Gate-Source Voltage	$V_{GSS}$	±30		V	
Drain Current	@T <sub>C</sub> =25 °C	$I_D$	10	10*	A
	@T <sub>C</sub> =100 °C		5	5*	
	Pulsed (Note1)	$I_{DP}$	25	25*	
Single Pulsed Avalanche Energy (Note 2)	$E_{AS}$	300		mJ	
Repetitive Avalanche Energy (Note 1)	$E_{AR}$	14.7		mJ	
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5		V/ns	
Drain Power Dissipation	T <sub>C</sub> =25 °C	$P_D$	130	41.5	W
	Derate above 25 °C		1.04	0.33	W/ °C
Maximum Junction Temperature	$T_j$	150		°C	
Storage Temperature Range	$T_{stg}$	-55 ~ 150		°C	
<b>Thermal Characteristics</b>					
Thermal Resistance, Junction-to-Case	$R_{thJC}$	0.96	3.0	°C/W	
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	62.5	62.5	°C/W	

\* : Drain current limited by maximum junction temperature.

## PIN CONNECTION

(KF10N50PR, KF10N50FR)



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## ELECTRICAL CHARACTERISTICS (Tc=25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$I_D=250\mu A, V_{GS}=0V$	500	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_j$	$I_D=250\mu A$ , Referenced to 25 °C	-	0.6	-	V/ °C
Drain Cut-off Current	$I_{DSS}$	$V_{DS}=500V, V_{GS}=0V$	-	-	10	$\mu A$
Gate Threshold Voltage	$V_{th}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
Gate Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	$\pm 100$	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=5A$	-	0.54	0.65	$\Omega$
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=400V, I_D=10A$ $V_{GS}=10V$ (Note4,5)	-	19.5	-	nC
Gate-Source Charge	$Q_{gs}$		-	4.5	-	
Gate-Drain Charge	$Q_{gd}$		-	8.7	-	
Turn-on Delay time	$t_{d(on)}$	$V_{DD}=250V$ $I_D=10A$ $R_G=25\Omega$ (Note4,5)	-	27	-	ns
Turn-on Rise time	$t_r$		-	35	-	
Turn-off Delay time	$t_{d(off)}$		-	60	-	
Turn-off Fall time	$t_f$		-	29	-	
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$	-	880	-	pF
Reverse Transfer Capacitance	$C_{rss}$		-	12	-	
Output Capacitance	$C_{oss}$		-	133	-	
<b>Source-Drain Diode Ratings</b>						
Continuous Source Current	$I_S$	$V_{GS}<V_{th}$	-	-	10	A
Pulsed Source Current	$I_{SP}$		-	-	40	
Diode Forward Voltage	$V_{SD}$	$I_S=10A, V_{GS}=0V$	-	-	1.4	V
Reverse Recovery Time	$t_{rr}$	$I_S=10A, V_{GS}=0V,$ $dI_S/dt=100A/\mu s$	-	176	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	0.7	-	$\mu C$

Note 1) Repetivity rating : Pulse width limited by junction temperature.

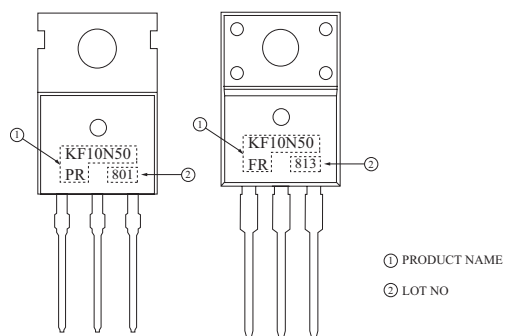
Note 2)  $L=5.5mH, I_S=10A, V_{DD}=50V, R_G=25\Omega$ , Starting  $T_j=25\text{ }^\circ C$ .

Note 3)  $I_S \leq 10A, dI/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$ , Starting  $T_j=25\text{ }^\circ C$ .

Note 4) Pulse Test : Pulse width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .

Note 5) Essentially independent of operating temperature.

## Marking



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Fig1.  $I_D - V_{DS}$

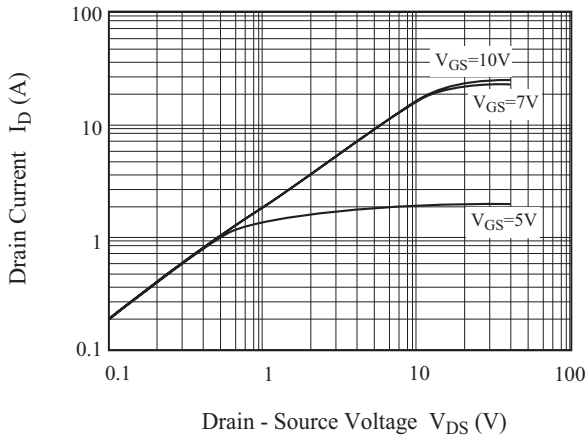


Fig2.  $I_D - V_{GS}$

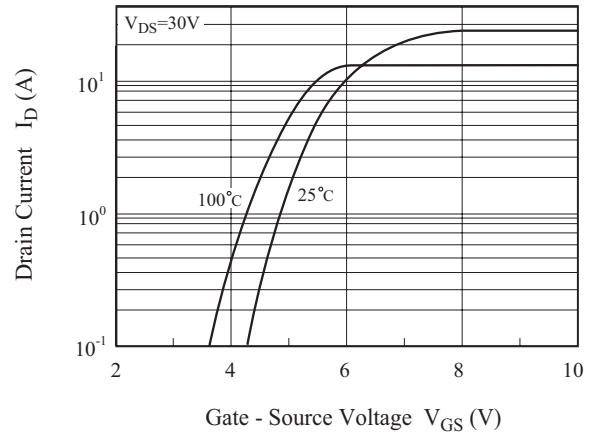


Fig3.  $BV_{DSS} - T_j$

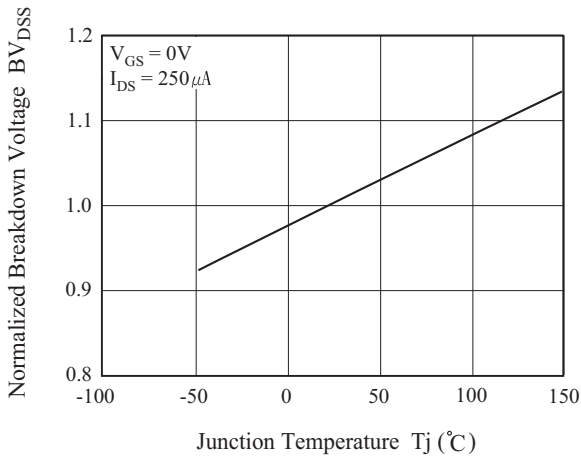


Fig4.  $R_{DS(ON)} - I_D$

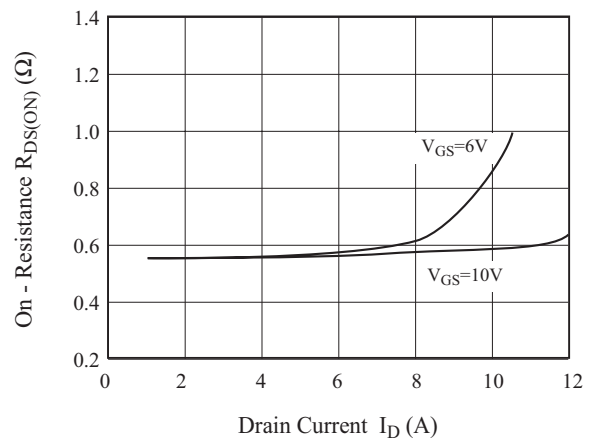


Fig5.  $I_S - V_{SD}$

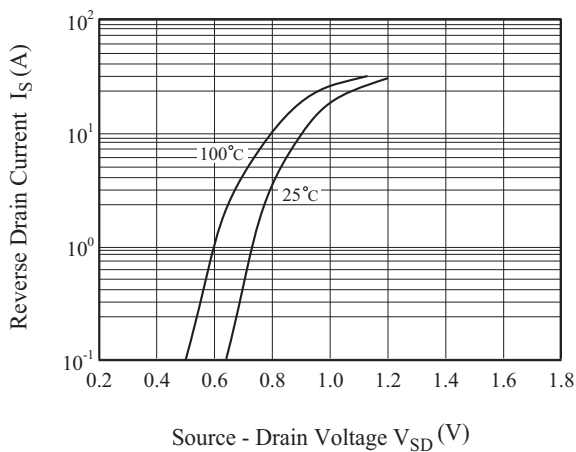
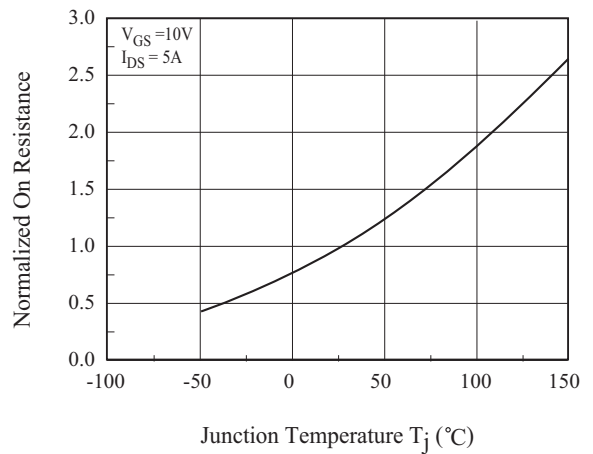


Fig6.  $R_{DS(ON)} - T_j$



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Fig 7. C - V<sub>DS</sub>

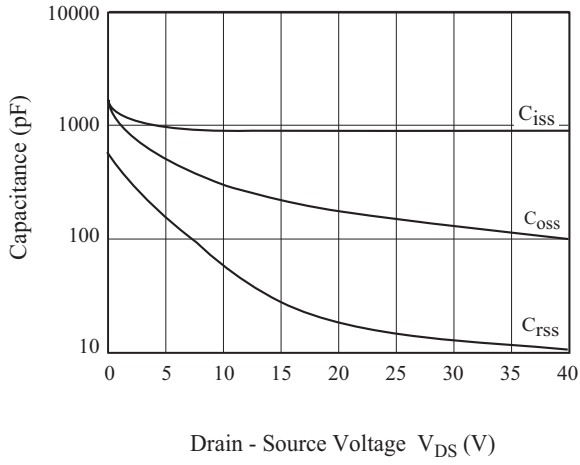


Fig8. Q<sub>g</sub>- V<sub>GS</sub>

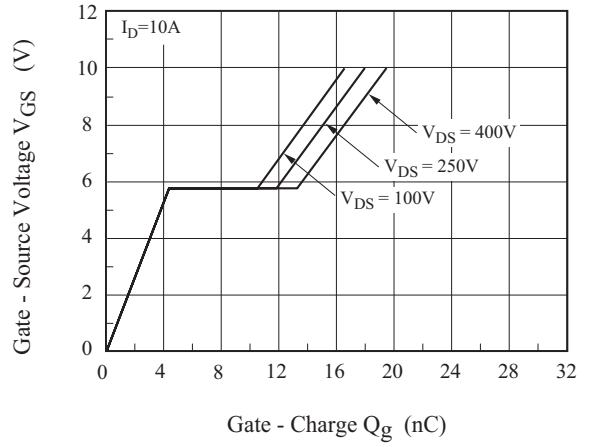


Fig9. Safe Operation Area

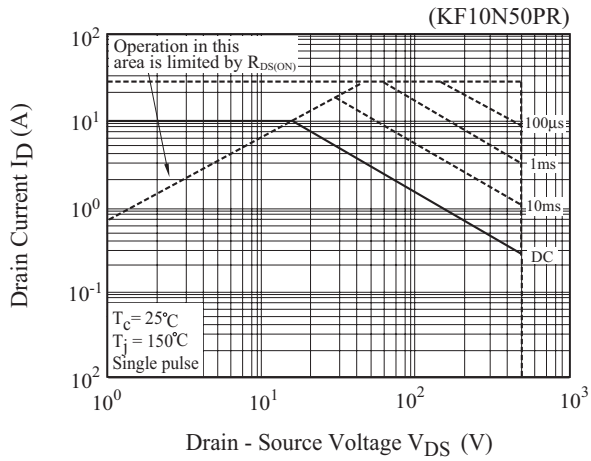


Fig10. Safe Operation Area

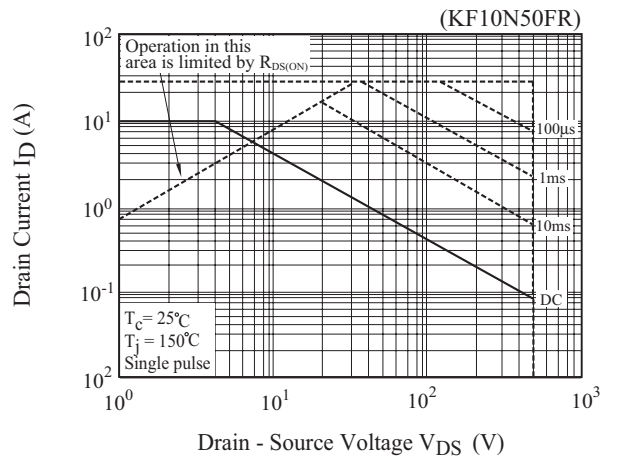
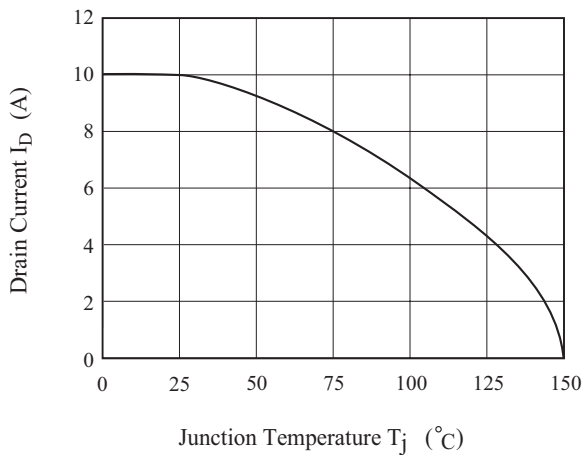


Fig11. I<sub>D</sub> - T<sub>j</sub>



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Fig12. Transient Thermal Response Curve

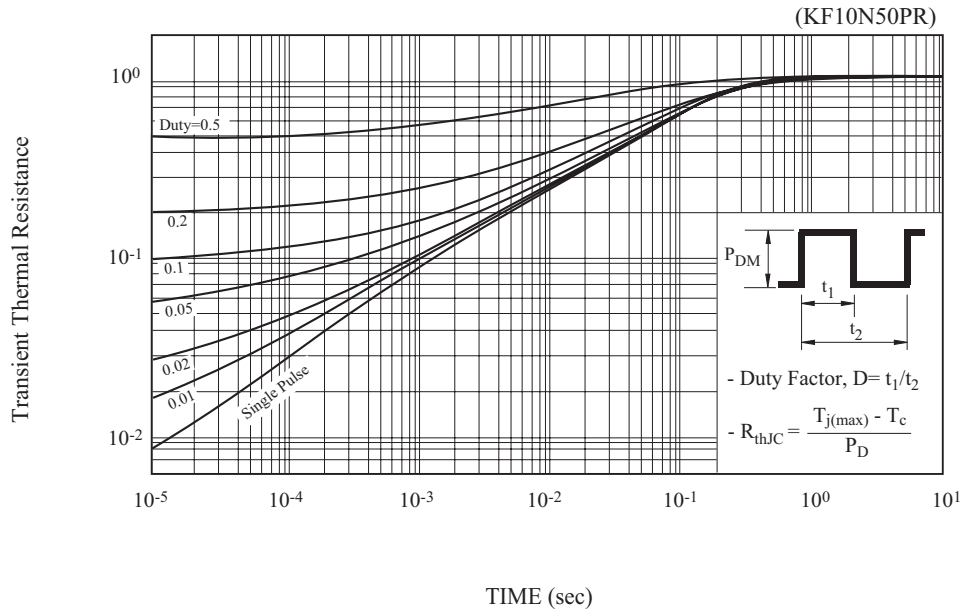
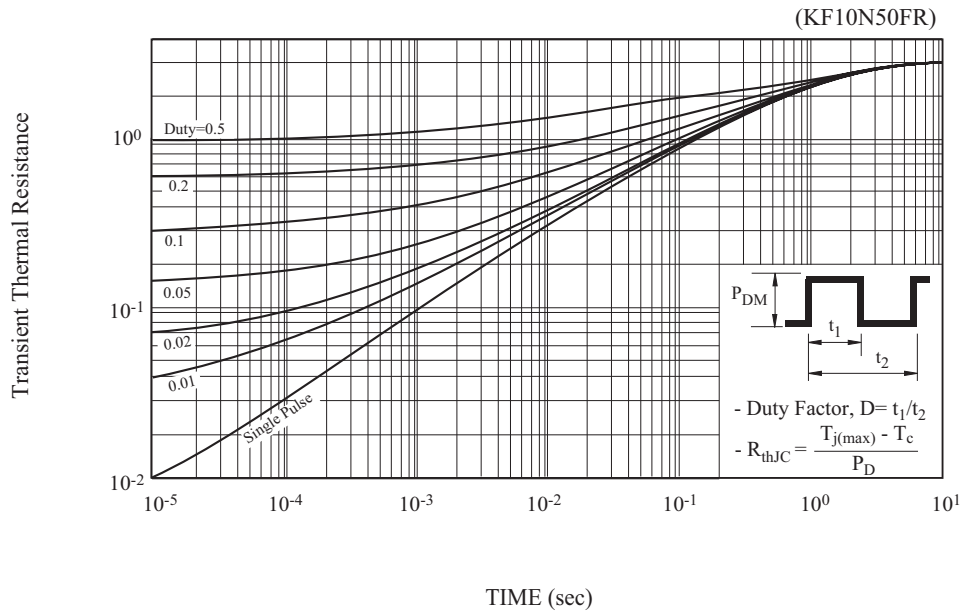


Fig13. Transient Thermal Response Curve



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Fig14. Gate Charge

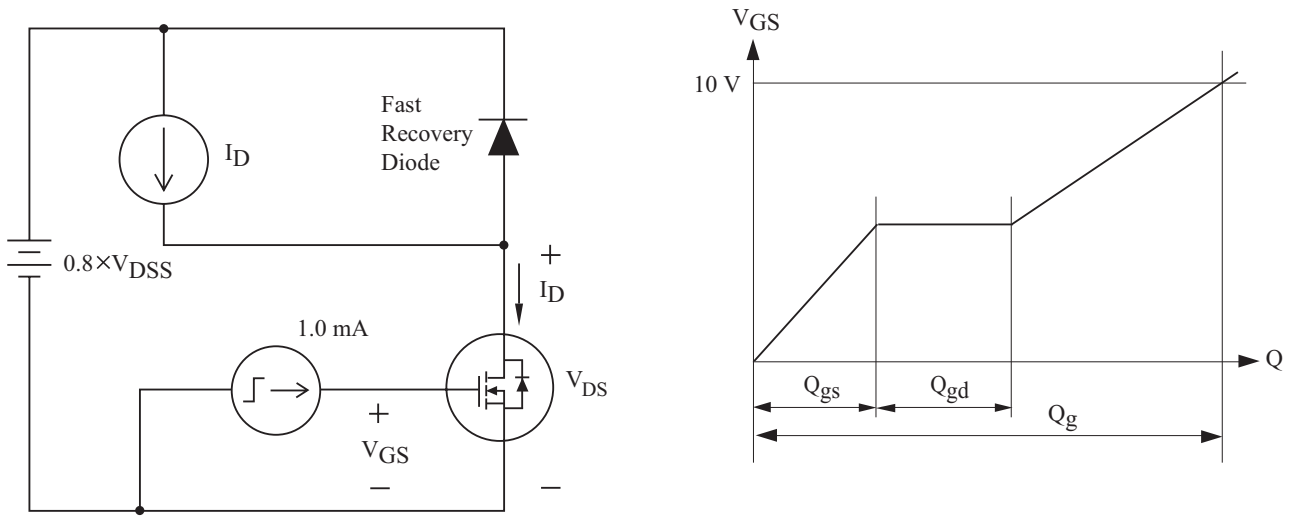


Fig15. Single Pulsed Avalanche Energy

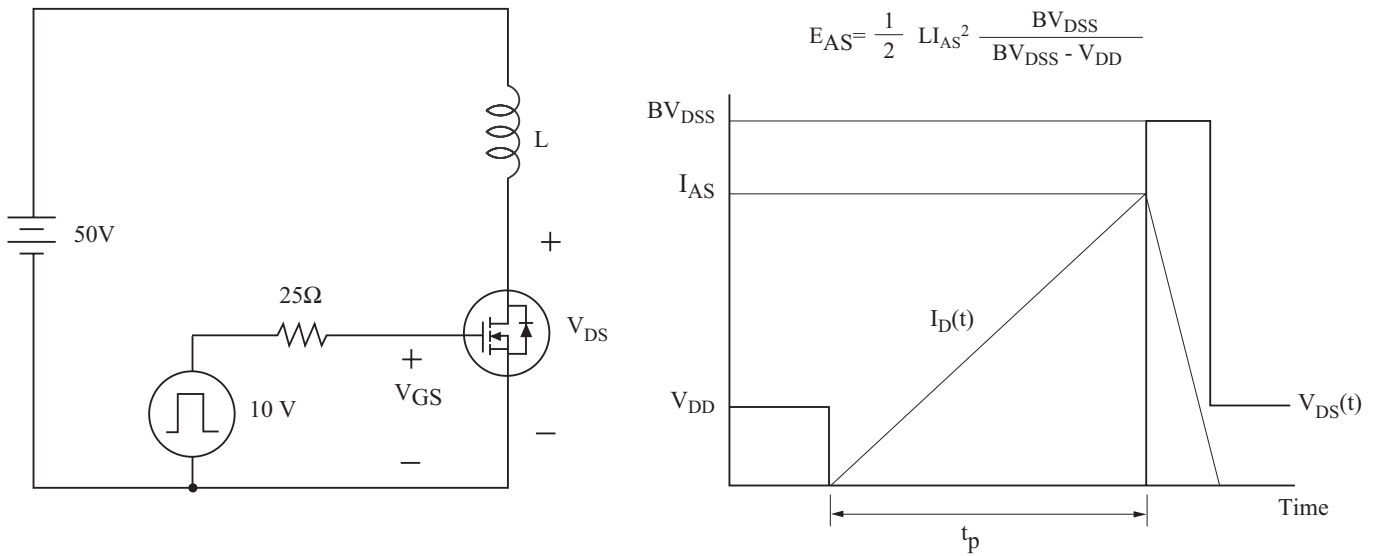
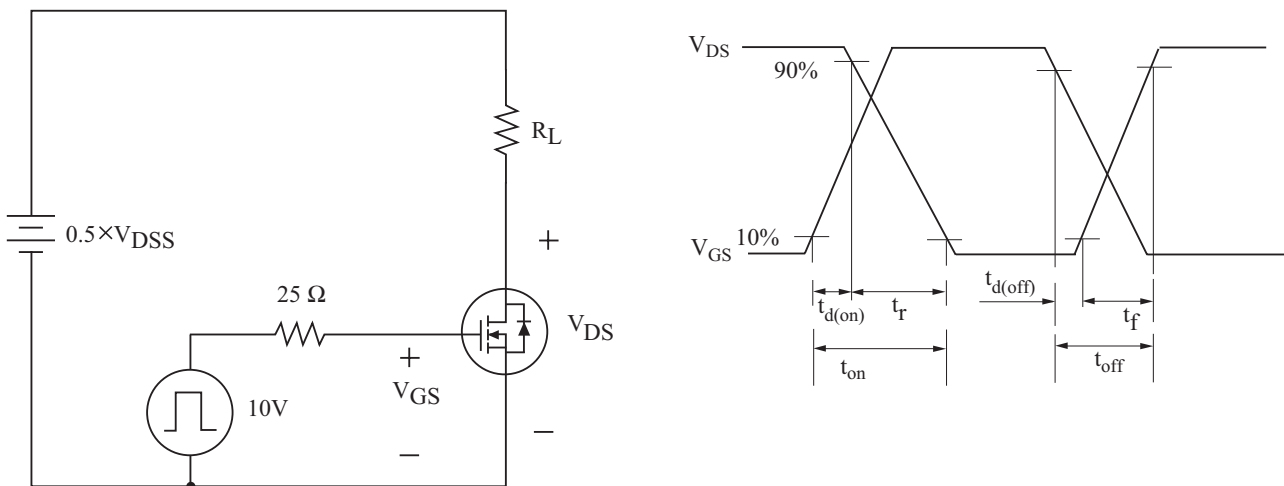


Fig16. Resistive Load Switching



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Fig17. Source - Drain Diode Reverse Recovery and  $dv/dt$

