TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7W74F,TC7W74FU,TC7W74FK

D-Type Flip Flop with Preset and Clear

The TC7W74 is a high speed C2MOS D Flip Flop fabricated with silicon gate C2MOS technology.

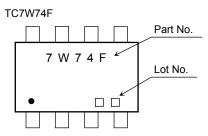
It achieves the high speed operation similar to equivalent LSTTL while maintaining the C<sup>2</sup>MOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse CLEAR and PRESET are independent of the CLOCK and are accomplished by setting the appropriate input to an "L" level Input is equipped with protection circuits against static discharge or transient excess voltage.

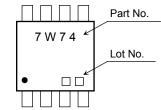
# Features

- High speed:  $f_{max} = 77 \text{ MHz}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 2 \ \mu A \ (max)$  at  $Ta = 25^{\circ}C$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: |IOH| = IOL = 4 mA (min)
- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range:  $V_{CC}$  (opr) = 2 to 6 V

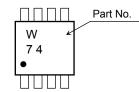
# Marking

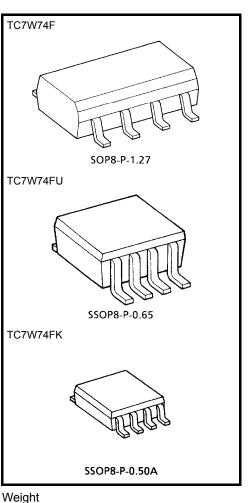


TC7W74FU



#### TC7W74FK





Weight SOP8-P-1.27: 0.05 g (typ.) SSOP8-P-0.65: 0.02 g (typ.) SSOP8-P-0.50A: 0.01 g (typ.)

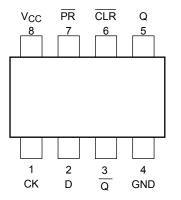
# Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	–0.5 to 7	V
DC input voltage	V <sub>IN</sub>	$-0.5$ to $V_{CC}$ + 0.5	V
DC output voltage	V <sub>OUT</sub>	$-0.5$ to $V_{CC}$ + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	IOK	±20	mA
DC output current	IOUT	±25	mA
DC V <sub>CC</sub> /ground current	ICC	±25	mA
Power discinction	PD	300 (FM8, SM8)	mW
Power dissipation	FD	200 (US8)	IIIVV
Storage temperature range	T <sub>stg</sub>	-65 to 150	°C
Lead temperature (10 s)	ΤL	260	°C

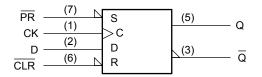
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

# Pin Configuration (top view)



# Logic Diagram



# **TOSHIBA**

# **Truth Table**

	Inp	uts	Out	Function		
	PR	D	СК	Q	IQ	T UNCLION
L	Н	Х	Х	L	Н	Clear
Н	L	Х	Х	Н	L	Preset
L	L	Х	Х	Н	Н	—
н	Н	L		L	Н	—
н	н	Н		Н	L	_
н	Н	х	$\rightarrow$	Qn	Qn	No Change

# **Operating Ranges**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2 to 6	V
Input voltage	V <sub>IN</sub>	0 to V <sub>CC</sub>	V
Output voltage	V <sub>I/O</sub>	0 to V <sub>CC</sub>	V
Operating temperature range	T <sub>opr</sub>	-40 to 85	°C
		0 to 1000 (V <sub>CC</sub> = 2.0 V)	
Input rise and fall time	t <sub>r</sub> , t <sub>f</sub>	0 to 500 (V <sub>CC</sub> = $4.5$ V)	ns
		0 to 400 ( $V_{CC} = 6.0 \text{ V}$ )	

# **Electrical Characteristics**

# **DC Electrical Characteristics**

Characteristics		Symbol	Test Condition			-	Ta = 25°C	;	Ta = -40 to 85°C		Unit	
		- ,				Min	Тур.	Max	Min	Max		
					2.0	1.5		_	1.5			
н	High level	VIH	—		4.5	3.15	_	_	3.15	_		
Input voltage					6.0	4.2	_	_	4.2	_	V	
input voltage					2.0	_	_	0.5	_	0.5	v	
	Low level	VIL		_	4.5	_	_	1.35	_	1.35		
					6.0	_	_	1.8	_	1.8		
	High level V <sub>OH</sub>	level V <sub>OH</sub>	V <sub>OH</sub> V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	_	1.9	_		
					4.5	4.4	4.5	_	4.4	_		
					6.0	5.9	6.0	_	5.9	_		
				I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	_	4.13	—		
Output				I <sub>OH</sub> = -5.2 mA	6.0	5.68	5.80	_	5.63	_	V	
voltage						2.0	_	0	0.1	_	0.1	v
				$I_{OL} = 20 \ \mu A$	4.5	_	0	0.1	_	0.1		
	Low level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		6.0	_	0	0.1	_	0.1		
				I <sub>OL</sub> = 4 mA	4.5	_	0.17	0.26	_	0.33		
			I <sub>OL</sub> = 5.2 mA	6.0	_	0.18	0.26	_	0.33			
Input leakage of	current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> o	r GND	6.0	_		±0.1		±1.0	μA	
Quiescent sup	ply current	ICC	$V_{IN} = V_{CC} o$	r GND	6.0			2.0		20.0	μA	

#### Timing Requirements (input $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit	
			$V_{CC}(V)$	Тур.	Limit	Limit		
			2.0	_	75	95		
Minimum pulse width (CLOCK)	t₩ (L) t₩ (H)	—	4.5	_	15	19	ns	
. ,	·vv (11)		6.0	_	13	16		
			2.0	_	75	95		
Minimum pulse width ( CLR , PR )	t <sub>W (L)</sub>	—	4.5	_	15	19	ns	
			6.0	_	13	16		
	ts		2.0	_	75	95	ns	
Minimum set-up time			4.5	_	15	19		
			6.0	_	13	16		
			2.0	_	0	0	ns	
Minimum hold time	t <sub>h</sub>		4.5	_	0	0		
			6.0	_	0	0		
			2.0	_	25	30	ns	
Minimum removal time ( CLR , PR )	t <sub>rem</sub>	—	4.5	_	5	6		
			6.0	_	4	5		
Clock frequency		_	2.0	_	6	5	MHz	
	f		4.5	_	31	25		
				_	36	29		

# AC Characteristics ( $C_L = 15 \text{ pF}, V_{CC} = 5 \text{ V}, \text{ Ta} = 25^{\circ}\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Output transition time	tтlн tтнL	_	_	6	12	ns
Propagation delay time (CLOCK-Q, Q)	t <sub>pLH</sub> t <sub>pHL</sub>	_	_	13	26	ns
Propagation delay time ( CLR , PR -Q, Q)	t <sub>pLH</sub> t <sub>pHL</sub>	_		14	26	ns
Maximum clock frequency	f <sub>max</sub>	_	36	77		MHz

Characteristics	Symbol	ymbol Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit								
	-,		V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max									
			2.0	_	30	75		95									
Output transition time	t <sub>TLH</sub> t <sub>THL</sub>	—	4.5	_	8	15	_	19	ns								
	STILL.		6.0	_	7	13	_	16									
			2.0	_	48	150	_	190									
Propagation delay time (CLOCK-Q, $\overline{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>	—	4.5	_	16	30	_	38	ns								
	чрпс		6.0	_	13	26	_	32									
Propagation delay time			2.0	_	51	150	_	190									
$(\overline{\text{CLR}}, \overline{\text{PR}}, \overline{\text{Q}})$	t <sub>pLH</sub> t <sub>pHL</sub>	—	4.5	_	17	30	_	38	ns								
	γHL	φnL	spine	-biir	-hi Ir	spire	pric	spine	ΨПС		6.0	_	15	26	_	32	
			2.0	6	21	_	5	—									
Maximum clock frequency	f <sub>max</sub>	—	4.5	31	63	_	25	—	MHz								
			6.0	36	67	_	29	_									
Input capacitance	C <sub>IN</sub>	_			5	10		10	pF								
Power dissipation capacitance	C <sub>PD</sub>		(Note)	_	34	_	_	_	pF								

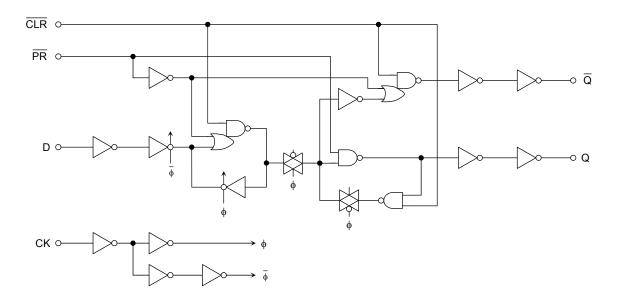
#### AC Electrical Characteristics ( $C_L = 50 \text{ pF}$ , input $t_r = t_f = 6 \text{ ns}$ )

Note: C<sub>PD</sub> is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$ 

#### System Diagram

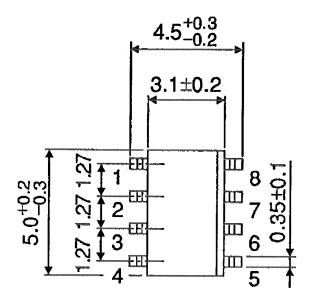


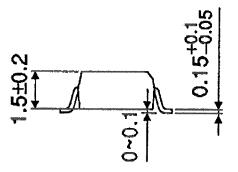
# **TOSHIBA**

#### **Package Dimensions**

SOP8-P-1.27

Unit : mm





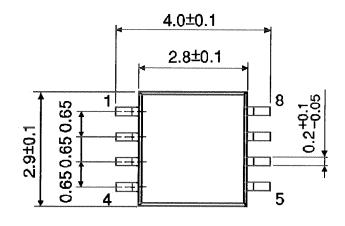
Weight: 0.05 g (typ.)

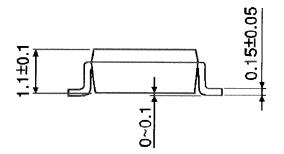
# **TOSHIBA**

# **Package Dimensions**

#### SSOP8-P-0.65

Unit : mm



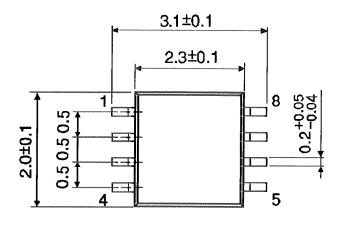


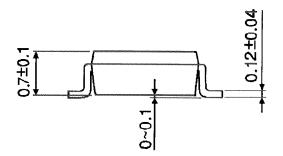
Weight: 0.02 g (typ.)

#### **Package Dimensions**

SSOP8-P-0.50A

Unit : mm





Weight: 0.01 g (typ.)

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