

## AON5810

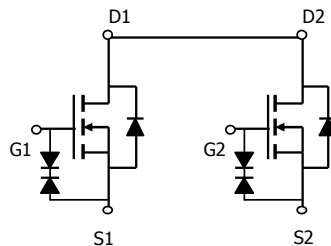
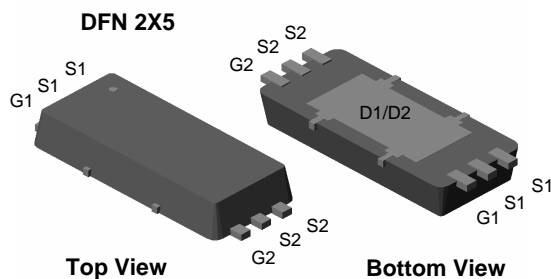
### Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

#### General Description

The AON5810 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 1.8V while retaining a 12V  $V_{GS(MAX)}$  rating. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration. *Standard Product AON5810 is Pb-free (meets ROHS & Sony 259 specifications). AON5810L is a Green Product ordering option. AON5810 and AON5810L are electrically identical.*

#### Features

$V_{DS} (V) = 20V$   
 $I_D = 7.7 A (V_{GS} = 4.5V)$   
 $R_{DS(ON)} < 18 m\Omega (V_{GS} = 4.5V)$   
 $R_{DS(ON)} < 19 m\Omega (V_{GS} = 4.0V)$   
 $R_{DS(ON)} < 21 m\Omega (V_{GS} = 3.1V)$   
 $R_{DS(ON)} < 25 m\Omega (V_{GS} = 2.5V)$   
 $R_{DS(ON)} < 40 m\Omega (V_{GS} = 1.8V)$   
 ESD Rating: 2000V HBM



#### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	
Continuous Drain Current $R_{\theta JA}=75^\circ C/W$	$I_D$	$T_A=25^\circ C$	7.7
		$T_A=70^\circ C$	6.1
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	30	A
Power Dissipation <sup>A</sup> $R_{\theta JA}=75^\circ C/W$	$P_{DSM}$	$T_A=25^\circ C$	1.6
		$T_A=70^\circ C$	1.0
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup> $t \leq 10s$	$R_{\theta JA}$	30	40	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A</sup> Steady-State		61	75	$^\circ C/W$
Maximum Junction-to-Case <sup>B</sup> Steady-State	$R_{\theta JC}$	4.5	6	$^\circ C/W$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±10V			10	μA
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	V <sub>DS</sub> =0V, I <sub>G</sub> =±250μA	±12			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.5	0.73	1	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V	30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =4.5V, I <sub>D</sub> =7.7A T <sub>J</sub> =125°C	11 16	14 21	18 26	mΩ
		V <sub>GS</sub> =4.0V, I <sub>D</sub> =6A	11	14.5	19	
		V <sub>GS</sub> =3.1V, I <sub>D</sub> =6A	13	16.7	21	
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =5A	15	20	25	
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =4A	25	32	40	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =7.7A		28		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V	0.5	0.74	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =10V, f=1MHz		1360		pF
C <sub>oss</sub>	Output Capacitance			200		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			178		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		1.5		Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (4.5V)	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =10V, I <sub>D</sub> =7.7A		13.1		nC
Q <sub>gs</sub>	Gate Source Charge			2		nC
Q <sub>gd</sub>	Gate Drain Charge			3.9		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =5V, V <sub>DS</sub> =10V, R <sub>L</sub> =1.4Ω, R <sub>GEN</sub> =3Ω		6.2		ns
t <sub>r</sub>	Turn-On Rise Time			11		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			40.5		ns
t <sub>f</sub>	Turn-Off Fall Time			10		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =7.7A, dI/dt=100A/μs		18.8		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =7.7A, dI/dt=100A/μs		8.1		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t<sub>10s</sub> thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

Rev 1: Sep. 2007

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

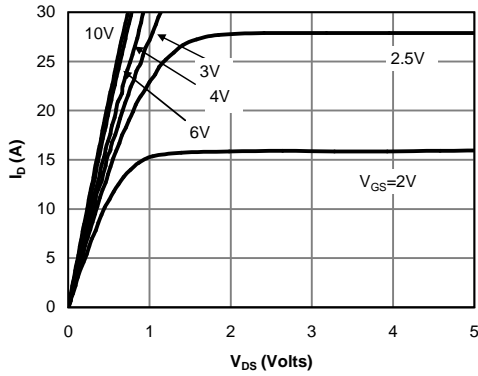


Fig 1: On-Region Characteristics

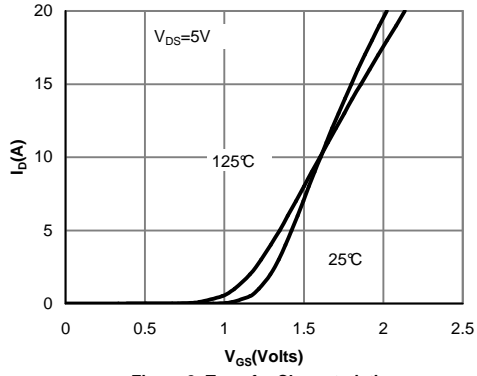


Figure 2: Transfer Characteristics

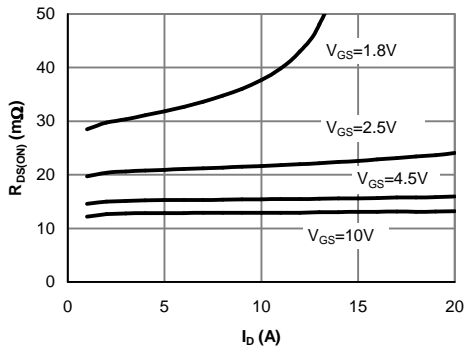


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

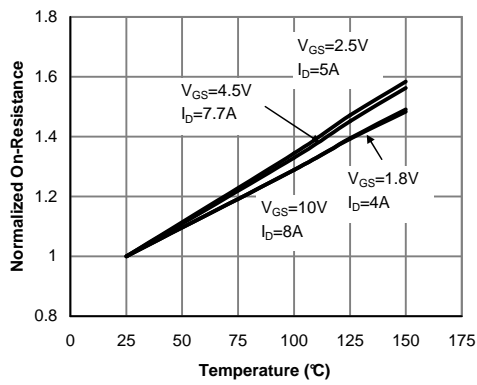


Figure 4: On-Resistance vs. Junction Temperature

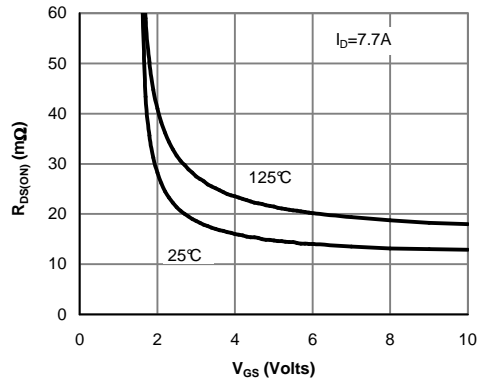


Figure 5: On-Resistance vs. Gate-Source Voltage

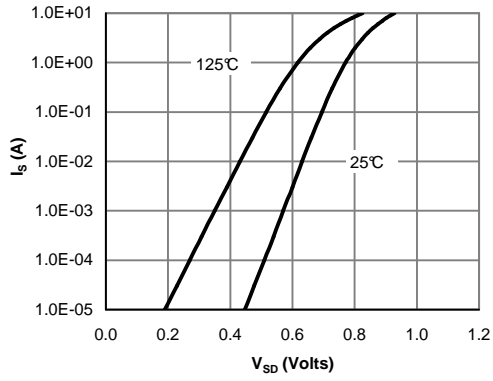


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

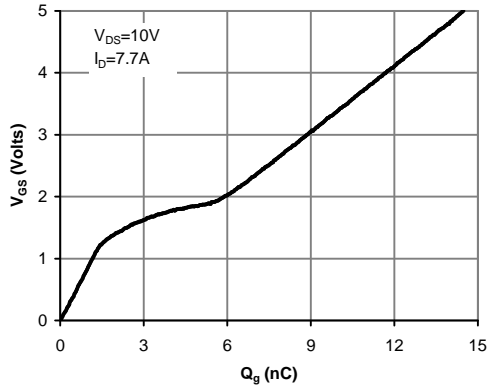


Figure 7: Gate-Charge Characteristics

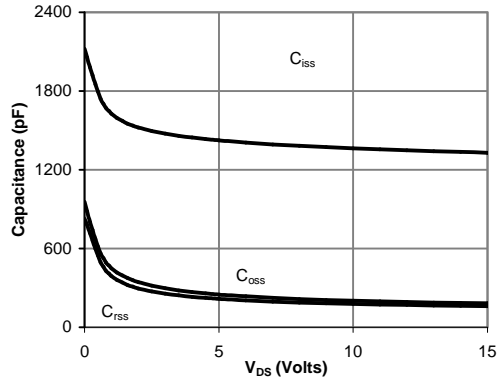


Figure 8: Capacitance Characteristics

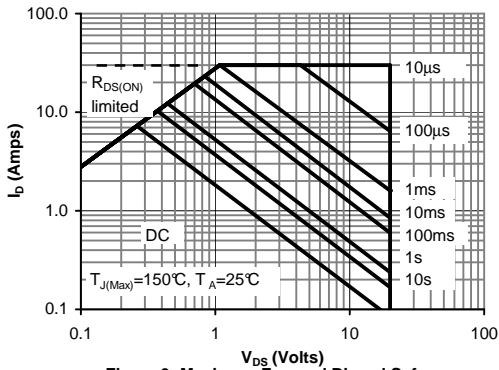


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

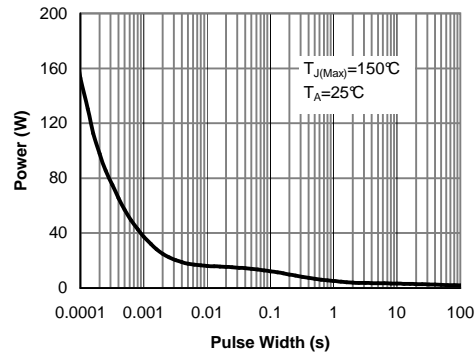


Figure 10: Single Pulse Power Rating Junction-to-Case (Note E)

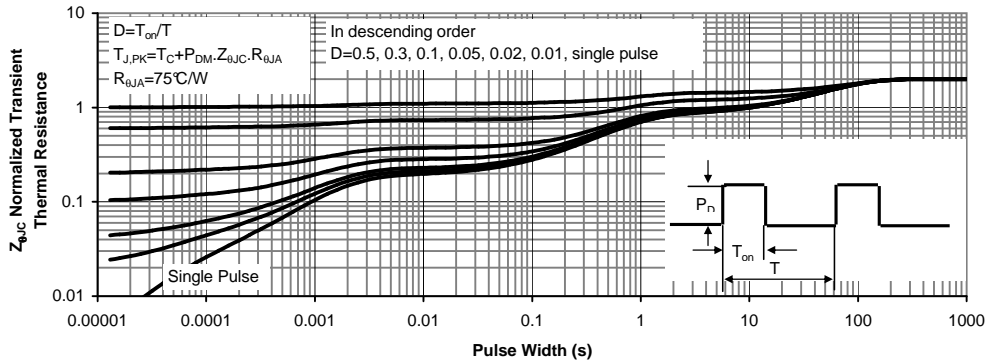


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)