

RoHS Compliant Product
A suffix of "-C" specifies halogen free

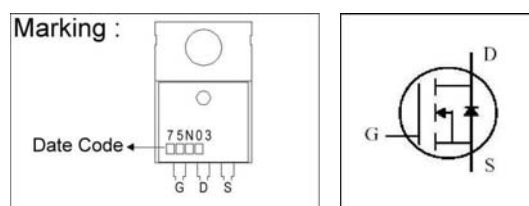
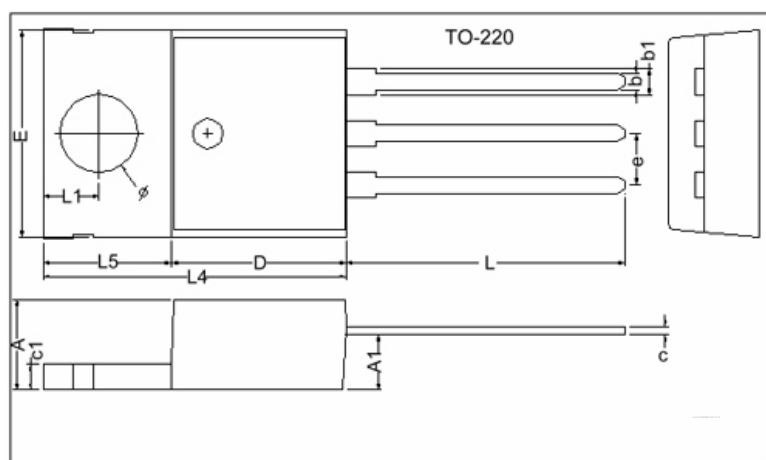
DESCRIPTION

The SSE75N03 used advanced design and process to achieve low gate charge, low on-resistance and fast switching performance. The through-hole version (TO-220) is available for low-profile applications and suited for low voltage applications such as DC/DC converters.

FEATURES

- Low Gate Charge
- Simple Drive Requirement
- Fast Switching

PACKAGE DIMENSIONS



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.40	4.80	c1	1.25	1.45
b	0.76	1.00	b1	1.17	1.47
c	0.36	0.50	L	13.25	14.25
D	8.60	9.00	e	2.54 REF.	
E	9.80	10.4	L1	2.60	2.89
L4	14.7	15.3	\emptyset	3.71	3.96
L5	6.20	6.60	A1	2.60	2.80

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current, $V_{GS}@ 4.5V$	$I_D @ Ta=25^\circ C$	75	A
Drain Current, $V_{GS}@ 4.5V$	$I_D @ Ta=100^\circ C$	62.5	A
Pulsed Drain Current ¹	I_{DM}	350	A
Total Power Dissipation	$P_D @ Tc=25^\circ C$	96	W
Linear Derating Factor		0.76	W/ $^\circ C$
Single Pulse Avalanche Energy ²	E_{AS}	400	mJ
Single Pulse Avalanche Current	I_{AS}	40	A
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55 ~ +150	$^\circ C$

THERMAL DATA

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-case Max.	$R_{\theta j-case}$	1.3	$^\circ C/W$
Thermal Resistance Junction-ambient Max.	$R_{\theta j-amb}$	62	$^\circ C/W$

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	25	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Breakdown Voltage Temp. Coefficient	$\Delta BV_{DSS}/\Delta T_j$	-	0.02	-	V/ $^\circ\text{C}$	Reference to 25°C , $I_D=1\text{mA}$
Gate Threshold Voltage	$V_{GS(th)}$	1.0	-	3.0	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Forward Transconductance	g_{fs}	-	29	-	S	$V_{DS}=10\text{V}, I_D=30\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20\text{V}$
Drain-Source Leakage Current($T_j=25^\circ\text{C}$)	I_{DSS}	-	-	1	μA	$V_{DS}=25\text{V}, V_{GS}=0$
Drain-Source Leakage Current($T_j=150^\circ\text{C}$)		-	-	25	μA	$V_{DS}=20\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance ³	$R_{DS(ON)}$	-	3.7	4.5	m Ω	$V_{GS}=10\text{V}, I_D=40\text{A}$
		-	6.0	7		$V_{GS}=4.5\text{V}, I_D=30\text{A}$
Total Gate Charge ³	Q_g	-	33	-	nC	$I_D=30\text{A}$ $V_{DS}=20\text{V}$ $V_{GS}=4.5\text{V}$
Gate-Source Charge	Q_{gs}	-	9	-		
Gate-Drain ("Miller") Charge	Q_{gd}	-	15	-		
Turn-on Delay Time ³	$T_{d(on)}$	-	10	-	ns	$V_{DS}=15\text{V}$ $I_D=30\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$ $R_D=0.5\Omega$
Rise Time	T_r	-	80	-		
Turn-off Delay Time	$T_{d(off)}$	-	37	-		
Fall Time	T_f	-	85	-		
Input Capacitance	C_{iss}	-	2070	-	pF	$V_{GS}=0\text{V}$ $V_{DS}=25\text{V}$ $f=1.0\text{MHz}$
Output Capacitance	C_{oss}	-	990	-		
Reverse Transfer Capacitance	C_{rss}	-	300	-		

SOURCE-DRAIN DIODE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V_{SD}	-	-	1.5	V	$I_S=20\text{A}, V_{GS}=0\text{V}$
Reverse Recovery Time ³	T_{RR}	-	50	-	Ns	$I_S=30\text{A}, V_{GS}=0\text{V}$
Reverse Recovery Charge	Q_{RR}	-	51	-	nC	$di/dt=100\text{A}/\mu\text{s}$

- Notes: 1. Pulse width limited by safe operating area.
2. Starting $T_j=25^\circ\text{C}$, $V_{DD}=20\text{V}$, $L=0.1\text{mH}$, $R_G=25\Omega$, $I_{AS}=10\text{A}$.
3. Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

CHARACTERISTIC CURVE

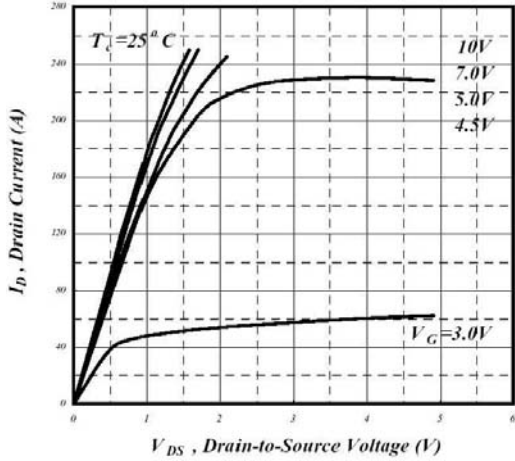


Fig 1. Typical Output Characteristics

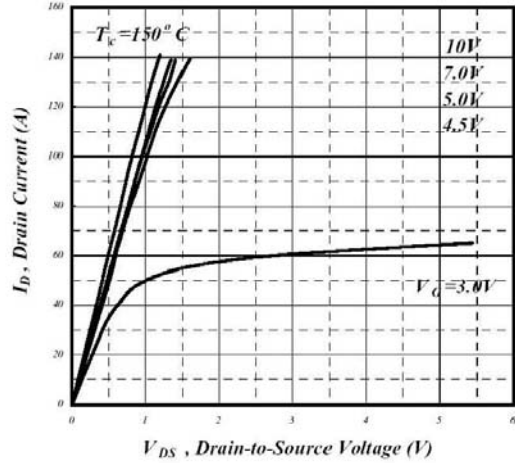


Fig 2. Typical Output Characteristics

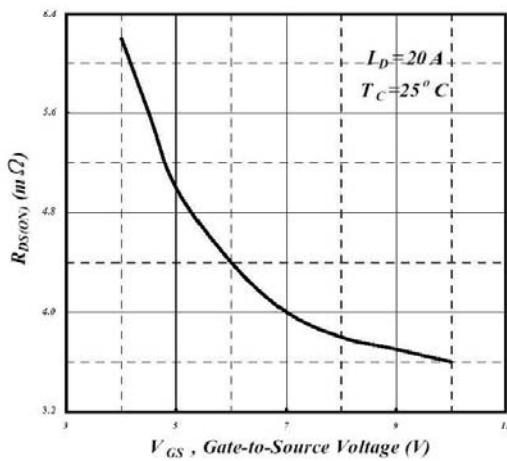


Fig 3. On-Resistance v.s. Gate Voltage

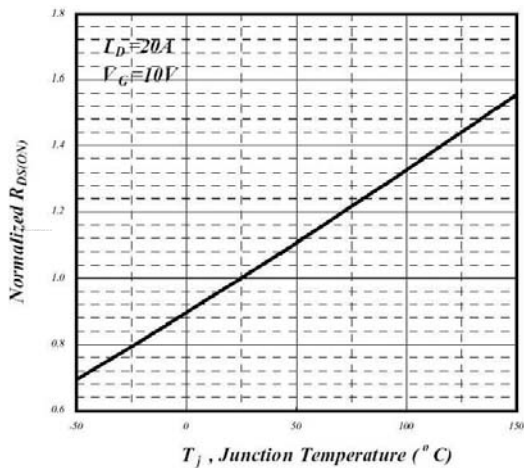


Fig 4. Normalized On-Resistance v.s. Junction Temperature

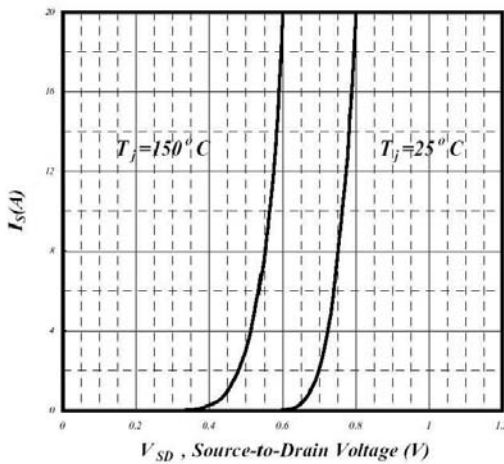


Fig 5. Forward Characteristics of Reverse Diode

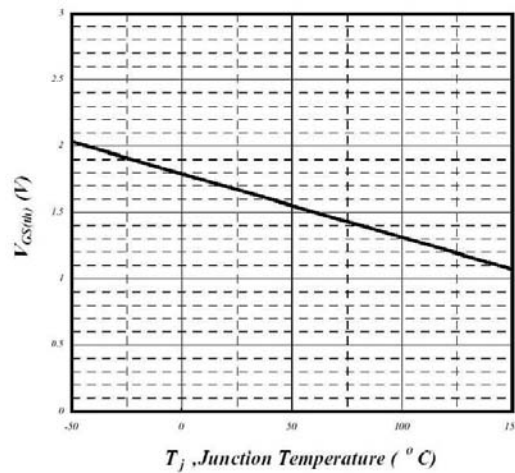


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CHARACTERISTIC CURVE

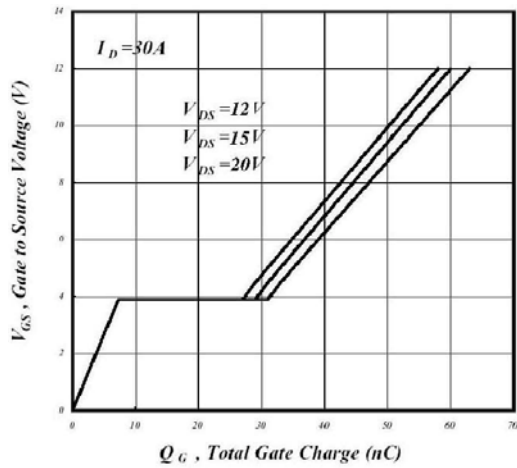


Fig 7. Gate Charge Characteristics

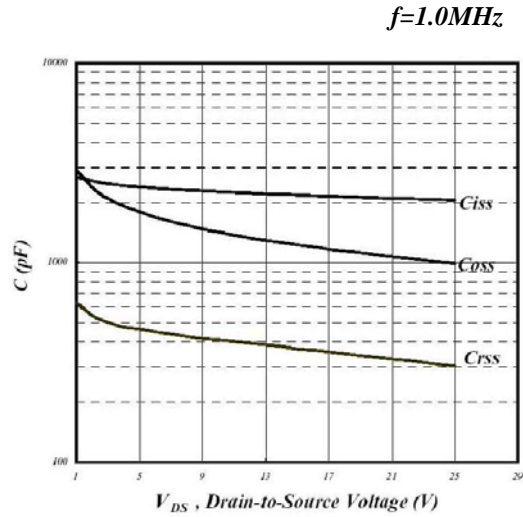


Fig 8. Typical Capacitance Characteristics

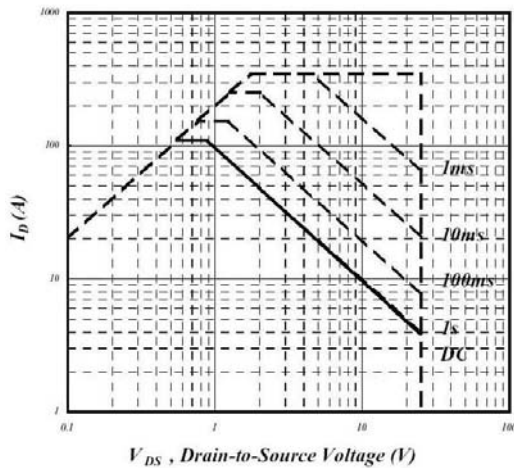


Fig 9. Maximum Safe Operating Area

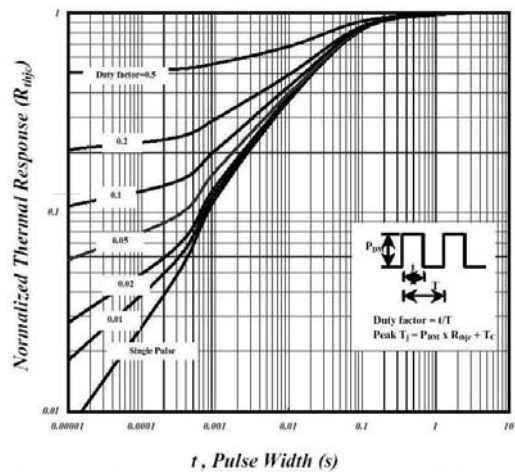


Fig 10. Effective Transient Thermal Impedance

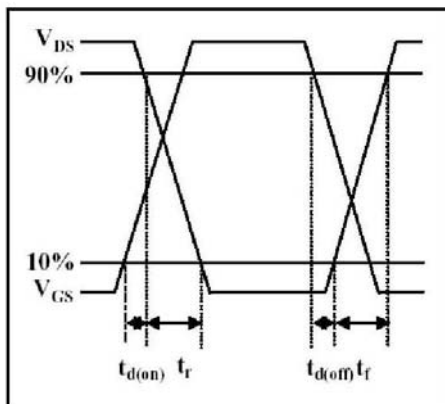


Fig 11. Switching Time Waveform

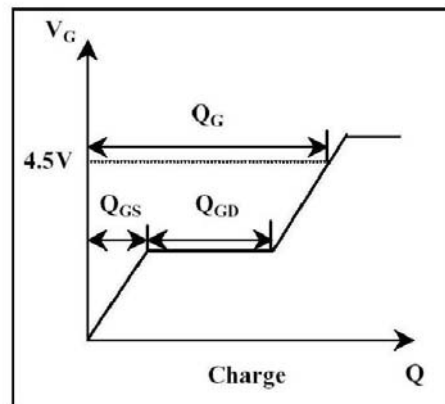


Fig 12. Gate Charge Waveform