FLASH MEMORY

MT28F016S5

5V Only, Dual Supply (Smart 5)

FEATURES

- Thirty-two 64KB erase blocks
- Deep Power-Down Mode:
  10µA MAX
- Smart 5 technology:
  5V ±10% VCC
  5V ±10% VPP application/production programming
  12V VPP tolerant compatibility production programming
- Address access time: 90ns
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence

OPTIONS — MARKING

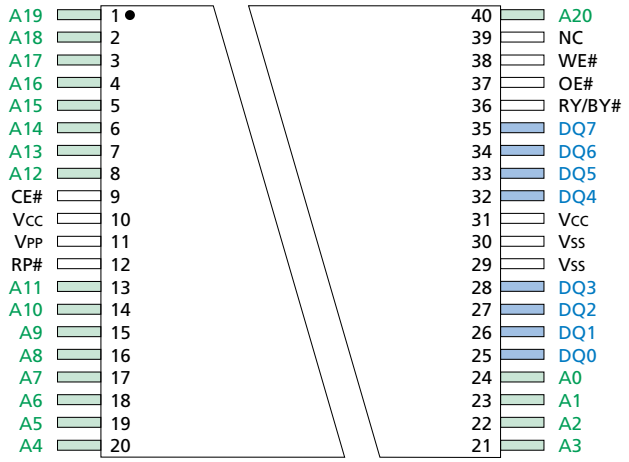
- Timing
  90ns access — -9

- Package
  Plastic 40-pin TSOP Type 1 (10mm x 20mm) VG

Part Number Example:
MT28F016S5VG-9

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I



GENERAL DESCRIPTION

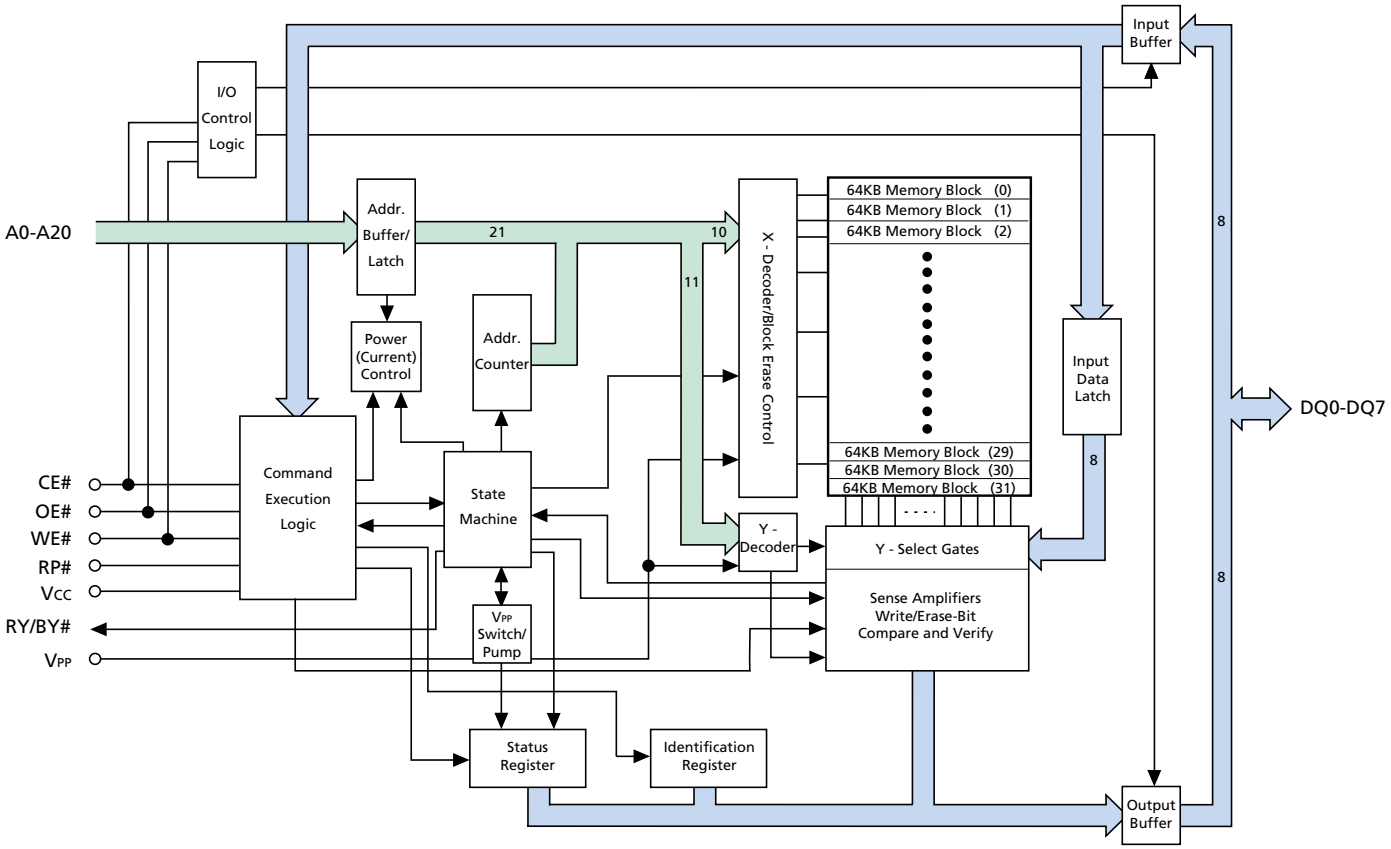
The MT28F016S5 is a nonvolatile, electrically block-erasable (flash), programmable, read-only memory containing 2,097,152 bytes (8 bits). Writing or erasing the device is done with a 5V VPP voltage, while all operations are performed with a 5V VCC. Due to process technology advances, 5V VPP is optimal for application and production programming. For backward compatibility with SmartVoltage technology, 12V VPP is supported for a maximum of 100 cycles and may be connected for up to 100 cumulative hours. The device is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F016S5 is organized into 32 separately erasable blocks. ERASEs may be interrupted to allow other operations with the ERASE SUSPEND command. After the ERASE SUSPEND command is issued, READ operations may be executed.

Operations are executed with commands from an industry-standard command set. In addition to status register polling, the MT28F016S5 provides a ready/busy# (RY/BY#) output to indicate WRITE and ERASE completion.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest data sheet.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
38	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
9	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
12	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# must be held at V_{IH} during all other modes of operation.
37	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 8, 7, 6, 5, 4, 3, 2, 1, 40	A0-A20	Input	Address Inputs: Select a unique, 8-bit byte out of the 2,097,152 available.
25-28, 32-35	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. Used to input commands to the CEL.
36	RY/BY#	Output	Ready/Busy: Indicates the status of the ISM. When RY/BY# = V_{OL}, the ISM is busy processing a command. If RY/BY# = V_{OH}, the ISM is ready to accept a new command. During deep power-down, device configuration read or erase suspend, RY/BY# = V_{OH}. Output is always active.
11	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the operation, V_{PP} must be at V_{PPH} (5V) (V_{PP} • V_{CC}). V_{PP} = "Don't Care" during all other operations.
10, 31	V_{CC}	Supply	Power Supply: +5V ±10%.
29, 30	V_{SS}	Supply	Ground.
39	NC	–	No Connect: This pin may be driven or left unconnected.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	ADDRESS	V_{PP}	DQ0-DQ7	RY/BY#
Standby	H	H	X	X	X	X	High-Z	V_{OH}
Deep Power-Down/Reset	L	X	X	X	X	X	High-Z	V_{OH}
READ								
READ	H	L	L	H	X	X	Data-Out	V_{OH}
Output Disable	H	L	H	H	X	X	High-Z	V_{OH}
WRITE/ERASE [2, 3]								
ERASE SETUP	H	L	H	L	X	X	20H	V_{OH}
ERASE CONFIRM [4]	H	L	H	L	BA	V_{PPH}	D0H	V_{OH} ∅ V_{OL}
WRITE SETUP	H	L	H	L	X	X	10H/40H	V_{OH}
WRITE [5]	H	L	H	L	WA	V_{PPH}	Data-In	V_{OH} ∅ V_{OL}
READ ARRAY [6]	H	L	H	L	X	X	FFH	V_{OH}
DEVICE CONFIGURATION								
Manufacturer Compatibility ID	H	L	L	H	000000H	X	89H	V_{OH}
Device ID	H	L	L	H	000001H	X	A0H	V_{OH}

NOTE: 1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. V_{PPH} = 5V.
3. BA = Block Address; WA = Write Address.
4. Operation must be preceded by ERASE SETUP command.
5. Operation must be preceded by WRITE SETUP command.
6. The READ ARRAY command must be issued before reading the array after writing or erasing.

FUNCTIONAL DESCRIPTION

The MT28F016S5 flash memory incorporates a number of features that make it ideally suited for system firmware or data storage. The memory array is segmented into individual erase blocks. Each block may be erased without affecting data stored in other blocks. These memory blocks are read, written and erased by issuing commands to the command execution logic (CEL). The CEL controls the operation of the internal state machine (ISM), which completely controls all WRITE, BLOCK ERASE and VERIFY operations. The ISM protects each memory location from over-erasure and optimizes each memory location for maximum data retention. In addition, the ISM greatly simplifies the control necessary for writing the device in-system or in an external programmer.

The Functional Description provides detailed information on the operation of the MT28F016S5 and is organized into these sections:

- Overview
- Memory Architecture
- Output (READ) Operations
- Input Operations
- Command Set
- ISM Status Register
- Device Configuration Registers
- Command Execution
- Error Handling
- WRITE/ERASE Cycle Endurance
- Power Usage
- Power-Up

OVERVIEW

SMART 5 TECHNOLOGY

Smart 5 technology allows maximum flexibility for in-system READ, WRITE and ERASE operations. For 5V-only systems, WRITE and ERASE operations may be executed with a V_{PP} voltage of 5V. Due to process technology advances, 5V V_{PP} is optimal for application and production programming. For backward compatibility with SmartVoltage technology, 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 100 cumulative hours. However, no performance increase is realized. For any operation, V_{CC} is at 5V.

THIRTY-TWO INDEPENDENTLY ERASABLE MEMORY BLOCKS

The MT28F016S5 is organized into 32 independently erasable memory blocks that allow portions of the memory to be erased without affecting the rest of the memory data.

INTERNAL STATE MACHINE (ISM)

BLOCK ERASE and WRITE timing are simplified with an ISM that controls all erase and write algorithms in the memory array. The ISM ensures protection against over-erasure and optimizes write margin to each cell.

During WRITE operations, the ISM automatically increments and monitors WRITE attempts, verifies write margin on each memory cell and updates the ISM status register. When a BLOCK ERASE is performed, the ISM automatically overwrites the entire addressed block (eliminates overerasure), increments and monitors ERASE attempts, and sets bits in the ISM status register.

ISM STATUS REGISTER

The ISM status register allows an external processor to monitor the status of the ISM during WRITE and ERASE operations. Two bits of the 8-bit status register are set and cleared entirely by the ISM. These two bits indicate whether the ISM is busy with an ERASE or WRITE task and when an ERASE has been suspended. Additional error information is set in three other bits: V_{PP} status, erase status and write status. These three bits must be cleared by the host system.

READY/BUSY# (RY/BY#) OUTPUT

In addition to status register polling, the MT28F016S5 provides an asynchronous RY/BY# output to indicate the status of the ISM. RY/BY# is V_{OH} when the state machine is inactive and V_{OL} during a WRITE or ERASE operation. This output is always active.

COMMAND EXECUTION LOGIC (CEL)

The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the read path (i.e., memory array, device configuration or status register). Commands may be issued to the CEL while the ISM is active. However, there are restrictions on what commands are allowed in this condition. See the Command Execution section for more detail.

DEEP POWER-DOWN MODE

To allow for maximum power conservation, the MT28F016S5 features a very low current, deep power-down mode. To enter this mode, the RP# pin is taken to V_{SS} ±0.2V. In this mode, the current draw is a maximum of 10µA. Entering deep power-down also clears the status register and sets the ISM to the read array mode.

MEMORY ARCHITECTURE

The MT28F016S5 memory array architecture is designed to allow sectors to be erased without disturbing the rest of the array. The array is divided into 32 addressable blocks that are independently erasable. When blocks rather than the entire array are erased, the total device endurance is enhanced, as is system flexibility. Only the ERASE functions are block-oriented. All READ and WRITE operations are done on a random-access basis. Figure 1 illustrates the memory address map.

OUTPUT (READ) OPERATIONS

The MT28F016S5 features three different types of READs. Depending on the current mode of the device, a READ operation will produce data from the memory array, status register or one of the device configuration registers. In each of these three cases, the WE#, CE# and OE# inputs are controlled in a similar manner. Moving between modes to perform a specific READ will be covered in the Command Execution section.

MEMORY ARRAY

To read the memory array, WE# must be HIGH, and OE# and CE# must be LOW. Valid data will be output on the DQ pins once these conditions have been met and a valid address is given. Valid data will remain on the DQ pins until the address changes, or until OE# or CE# goes HIGH, whichever occurs first. The DQ pins will continue to output new data after each address transition as long as OE# and CE# remain LOW.

Figure 1
Memory Address Map

After power-up or RESET, the device will automatically be in the array read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

STATUS REGISTER

Performing a READ of the status register requires the same input sequencing as a READ of the array except that the address inputs are "Don't Care." Data from the status register is latched on the falling edge of OE# or CE#, whichever occurs last. If the contents of the status register change during a READ of the status register, either OE# or CE# may be toggled while the other is held LOW to update the output.

Following a WRITE or ERASE operation, the device automatically enters the status register read mode. In addition, a READ during a WRITE or ERASE operation will produce the status register contents on DQ0-DQ7. When the device is in ERASE SUSPEND mode, a READ operation will produce the status register contents until another command is issued. While the device is in certain other modes, READ STATUS REGISTER may be given to return to the status register read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

DEVICE CONFIGURATION REGISTERS

Reading any of the device configuration registers requires the same input sequencing as reading the status register except that specific addresses must be issued. WE# must be HIGH, and OE# and CE# must be LOW. To read the manufacturer compatibility ID, addresses must be at 000000H, and to read the device ID, addresses must be at 000001H.

While the device is in certain other modes, READ DEVICE CONFIGURATION may be given to return to the configuration registers read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

INPUT OPERATIONS

The DQ pins are used either to input data to the array or to input a command to the CEL. A command input issues an 8-bit command to the CEL to control the mode of operation of the device. A WRITE is used to input data to the memory array. The following section describes both types of inputs. More information describing how to use the two types of inputs to write or erase the device is provided in the Command Execution section.

COMMANDS

To perform a command input, OE# must be HIGH, and CE# and WE# must be LOW. Addresses are "Don't Care" but must be held stable, except during an ERASE CONFIRM. The 8-bit command is input on DQ0-DQ7 and is latched on the rising edge of CE# (CE#-controlled) or WE# (WE#-controlled), whichever occurs first.

MEMORY ARRAY

A WRITE to the memory array sets the desired bits to logic 0s but cannot change a given bit to a logic 1 from a logic 0. Setting any bits to a logic 1 requires that the entire block be erased. To perform a WRITE, OE# must be HIGH, CE# and WE# must be LOW, and V_{PP} must be set to V_{PPH} (5V). A0-A20 provide the address to be written, while the data to be written to the array is input on the DQ pins. The data and addresses are latched on the rising edge of either CE# (CE#-controlled) or WE# (WE#-controlled), whichever occurs first. A WRITE must be preceded by a WRITE SETUP command. Details on how to input data to the array will be covered in the Write Sequence section.

COMMAND SET

To simplify writing of the memory blocks, the MT28F016S5 incorporates an ISM that controls all internal algorithms for the WRITE and ERASE cycles. An 8-bit command set is used to control the device. Details on how to sequence commands are provided in the Command Execution section. Table 1 lists the valid commands.

ISM STATUS REGISTER

The 8-bit ISM status register (see Table 2) is polled to check for WRITE or ERASE completion or any related errors. During or following a WRITE, ERASE or ERASE SUSPEND, a READ operation will output the status register contents on DQ0-DQ7 without prior command. While the status register contents are read, the outputs will not be updated if there is a change in the ISM status unless OE# or CE# is toggled. If the device is not in the write, erase, erase suspend, status register or read mode, READ STATUS REGISTER (70H) can be issued to view the status register contents.

All of the defined bits are set by the ISM, but only the ISM and erase suspend status bits are reset by the ISM. The erase, write and V_{PP} status bits must be cleared using CLEAR STATUS REGISTER (50H). This allows the user to choose when to poll and clear the status register. For example, the host system may perform multiple WRITE operations before checking the status register instead of checking after each individual WRITE. Asserting the RP# signal or powering down the device will also clear the status register.

DEVICE CONFIGURATION REGISTERS

The device ID and manufacturer compatibility ID can be read by issuing READ DEVICE CONFIGURATION (90H). To read the desired register, a specific address must be asserted. See Table 3 for more details on the various device configuration registers.

Table 1
Command Set

COMMAND	HEX CODE	DESCRIPTION
RESERVED	00H	This command and all unlisted commands are invalid and should not be called. These commands are reserved to allow for future feature enhancements.
READ ARRAY	FFH	Must be issued after any other command cycle before the array can be read. It is not necessary to issue this command after power-up or RESET.
READ DEVICE CONFIGURATION	90H	Allows the device ID and manufacturer ID to be read. Please refer to Table 3 for more information on the various device configuration registers.
READ STATUS REGISTER	70H	Allows the status register to be read. Please refer to Table 2 for more information on the status register bits.
CLEAR STATUS REGISTER	50H	Clears status register bits 3-5, which cannot be cleared by the ISM.
ERASE SETUP	20H	The first command given in the two-cycle ERASE sequence. The ERASE will not be completed unless followed by ERASE CONFIRM.
ERASE CONFIRM	D0H	The second command given in the two-cycle ERASE sequence. Must follow an ERASE SETUP to be valid. Also used during a WRITE/ERASE SUSPEND to resume the WRITE or ERASE.
WRITE SETUP	40H or 10H	The first command given in the two-cycle WRITE sequence. The write data and address are given in the following cycle to complete the WRITE.
ERASE SUSPEND	B0H	Requests a halt of the ERASE and puts the device into the erase suspend mode. When the device is in this mode, only READ STATUS REGISTER, READ ARRAY and ERASE CONFIRM (ERASE RESUME) commands may be executed.

Table 2
Status Register

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	ISM STATUS 1 = Ready 0 = Busy	The ISMS bit displays the active status of the state machine during WRITE or BLOCK ERASE operations. The controlling logic polls this bit to determine when the erase and write status bits are valid.
SR6	ERASE SUSPEND STATUS 1 = ERASE suspended 0 = ERASE in progress/completed	Issuing an ERASE SUSPEND places the ISM in the suspend mode and sets this and the ISMS bit to "1." The ESS bit will remain "1" until an ERASE CONFIRM is issued.
SR5	ERASE STATUS 1 = BLOCK ERASE error 0 = Successful BLOCK ERASE	ES is set to "1" after the maximum number of ERASE cycles is executed by the ISM without a successful verify. ES is only cleared by a CLEAR STATUS REGISTER command or by a RESET.
SR4	WRITE STATUS 1 = WRITE error 0 = Successful WRITE	WS is set to "1" after the maximum number of WRITE cycles is executed by the ISM without a successful verify. WS is only cleared by a CLEAR STATUS REGISTER command or by a RESET.
SR3	V_{PP} STATUS 1 = No V_{PP} voltage detected 0 = V_{PP} present	$V_{PP}S$ detects the presence of a V_{PP} voltage. It does not monitor V_{PP} continuously, nor does it indicate a valid V_{PP} voltage. The V_{PP} pin is sampled for 5V after WRITE or ERASE CONFIRM is given. $V_{PP}S$ must be cleared by CLEAR STATUS REGISTER or by a RESET.
SR0-2	RESERVED	Reserved for future use.

Table 3
Device Configuration

DEVICE CONFIGURATION	ADDRESS	DATA	CONDITION
Manufacturer Compatibility ID	000000H	89H	Manufacturer compatibility ID read
Device ID	000001H	A0H	Device ID read

COMMAND EXECUTION

Commands are issued to bring the device into different operational modes. Each mode allows specific operations to be performed. Several modes require a sequence of commands to be written before they are reached. The following section describes the properties of each mode, and Table 4 lists all command sequences required to perform the desired operation.

READ ARRAY

The array read mode is the initial state of the device upon power-up and is also entered after a RESET. If the device is in any other mode, READ ARRAY (FFH) must be given to return to the array read mode. Unlike the WRITE SETUP command (40H), READ ARRAY does not need to be given before each individual read access.

DEVICE CONFIGURATION

To read the device ID and manufacturer compatibility ID, the READ DEVICE CONFIGURATION (90H) command must be issued. While the device is in this mode, specific addresses must be issued to read the desired information. The manufacturer compatibility ID is read at 000000H, and the device ID is read at 000001H.

WRITE SEQUENCE

Two consecutive cycles are needed to input data to the array. WRITE SETUP (40H or 10H) is given in the first cycle. The next cycle is the WRITE, during which the write address and data are issued and V_{PP} is brought to V_{PPH}. The ISM will now begin to write the byte. V_{PP} must be held at V_{PPH} until the WRITE is completed (SR7 = 1 and RY/BY# = V_{OH}).

While the ISM executes the WRITE, the ISM status bit (SR7) will be at "0" and RY/BY# = V_{OL}, and the device will not respond to any commands. Any READ operation will produce the status register contents on DQ0-DQ7. When the ISM status bit (SR7) is set to a logic 1 and RY/BY# = V_{OH}, the WRITE has been completed, and the device will go into the status register read mode until another command is given.

Table 4
Command Sequences

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE			2ND CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY	1	WRITE	X	FFH				1
READ DEVICE CONFIGURATION	2	WRITE	X	90H	READ	CA	CD	2, 3
READ STATUS REGISTER	2	WRITE	X	70H	READ	X	SRD	4
CLEAR STATUS REGISTER	1	WRITE	X	50H				
ERASE SETUP/CONFIRM	2	WRITE	X	20H	WRITE	BA	D0H	5, 6
ERASE SUSPEND/RESUME	2	WRITE	X	B0H	WRITE	X	D0H	
WRITE SETUP/WRITE	2	WRITE	X	40H	WRITE	WA	WD	6, 7
ALTERNATE WRITE	2	WRITE	X	10H	WRITE	WA	WD	6, 7

NOTE: 1. Must follow WRITE or ERASE CONFIRM commands to the CEL in order to enable flash array READ cycles.
2. CA = Configuration Address: 00000H for manufacturer compatibility ID and 00001H for device ID.
3. CD = Configuration Data.
4. SRD = Status Register Data.
5. BA = Block Address.
6. Addresses are "Don't Care" in first cycle but must be held stable.
7. WA = Address to be written; WD = Data to be written to WA.

ERASE SEQUENCE

Executing an ERASE sequence will set all bits within a block to logic 1. The command sequence necessary to execute an ERASE is similar to that of a WRITE. To provide added security against accidental block erasure, two consecutive command cycles are required to initiate an ERASE of a block. In the first cycle, addresses are "Don't Care," and ERASE SETUP (20H) is given. In the second cycle, V_{PP} is brought to V_{PPH}, an address within the block to be erased is issued, and ERASE CONFIRM (D0H) is given. If a command other than ERASE CONFIRM is given, the write and erase status bits (SR4 and SR5) will be set, and the device will be in the read status mode.

After the ERASE CONFIRM (D0H) is issued, the ISM will start the ERASE of the addressed block. Any READ operation will output the status register contents on DQ0-DQ7. V_{PP} must be held at V_{PPH} until the ERASE is completed (SR7 = 1 and RY/BY# = V_{OH}). Once the ERASE is completed, the device will be in the status register read mode until another command is issued.

ERASE SUSPENSION

The only command that may be issued while an ERASE is in progress is ERASE SUSPEND. This command allows other commands to be executed while pausing the ERASE in progress. Once the device has reached the suspend mode, the erase suspend status bit (SR6) and ISM status bit (SR7) will be set and RY/BY# will transition to V_{OH}. The device may now be given a READ ARRAY, ERASE RESUME or READ STATUS REGISTER command. After READ ARRAY has been issued, any location not within the block being erased may be read. If ERASE RESUME is issued before SR6 has been set, the device will immediately proceed with the ERASE in progress. During an ERASE SUSPEND, V_{PP} and RP# must remain at the same levels used for the ERASE.

ERROR HANDLING

After the ISM status bit (SR7) has been set, V_{PP} (SR3), write (SR4) and erase (SR5) status bits may be checked. If one or a combination of these four bits has been set, an error has occurred. The ISM cannot reset these four bits. To clear these bits, CLEAR STATUS REGISTER (50H) must be given. Table 6 lists the combination of errors.

WRITE/ERASE CYCLE ENDURANCE

The MT28F016S5 is designed and fabricated to meet advanced firmware and data storage requirements. To ensure this level of reliability, V_{PP} must be at 5V ±10% during WRITE or ERASE cycles. For SmartVoltage-compatible production programming, 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 100 cumulative hours. Operation outside these limits may reduce the number of WRITE and ERASE cycles that can be performed on the device.

POWER USAGE

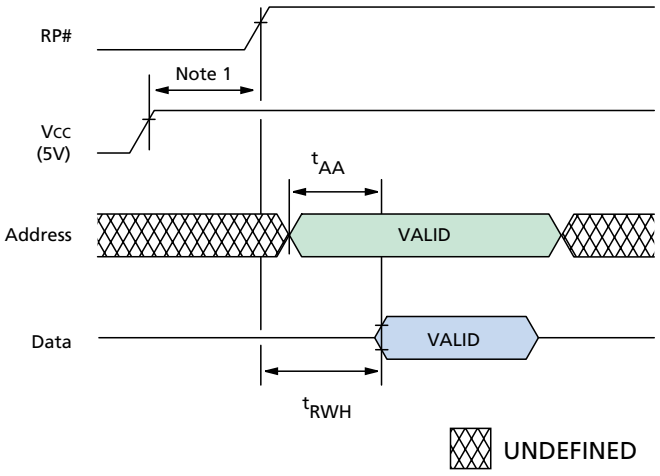
The MT28F016S5 offers several power-saving features that may be utilized in the array read mode to conserve power. Deep power-down mode is enabled by bringing RP# to V_{SS} ±0.2V. Current draw (I_{CC}) in this mode is a maximum of 10µA. When CE# is HIGH, the device will enter standby mode. In this mode, maximum I_{CC} current is 100µA. If CE# is brought HIGH during a WRITE or ERASE, the ISM will continue to operate, and the device will consume the respective active power until the WRITE or ERASE is completed.

POWER-UP

The likelihood of unwanted WRITE or ERASE operations is minimized since two consecutive cycles are required to execute either operation. However, to reset the ISM and to provide additional protection while V_{CC} is ramping, one of the following conditions must be met:

- RP# must be held LOW until V_{CC} is at valid functional level; ***or***
- CE# or WE# may be held HIGH and RP# must be toggled from V_{CC}-GND-V_{CC}.

After a power-up or RESET, the status register is reset, and the device will enter the array read mode.



NOTE: 1. V_{CC} must be within the valid operating range before RP# goes HIGH.

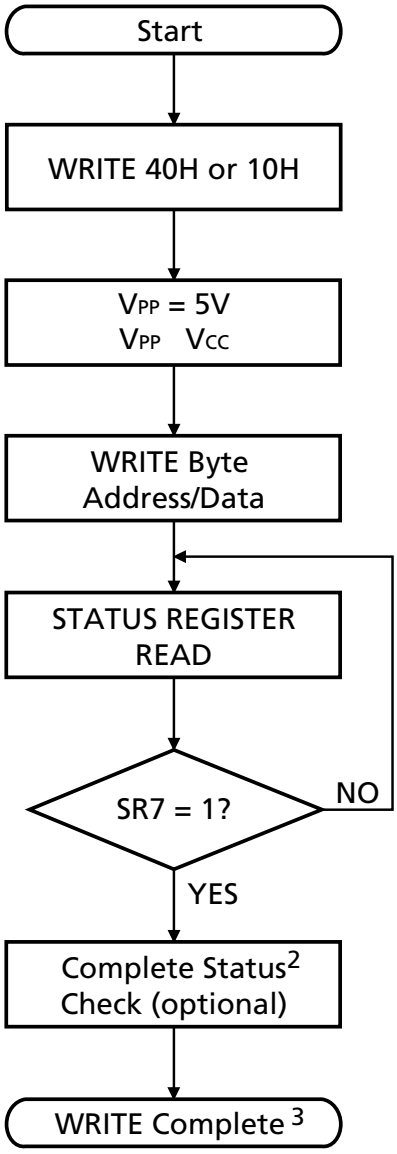
Figure 2
Power-Up/Reset Timing Diagram

Table 6
Status Register Error Decode[1]

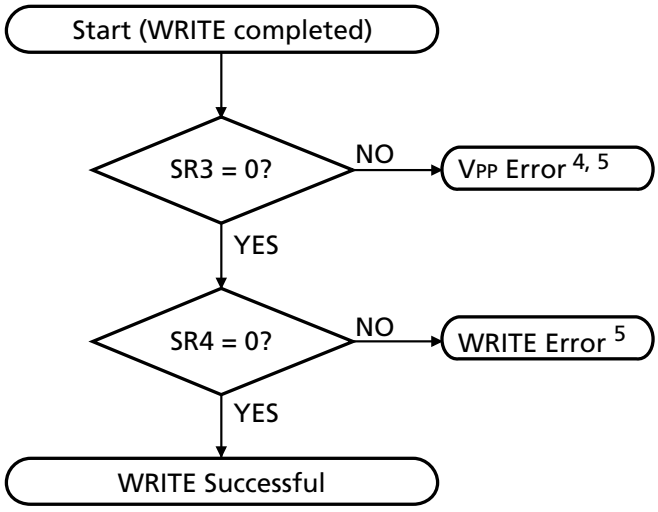
STATUS BITS			
SR5	SR4	SR3	ERROR DESCRIPTION[2]
0	0	0	No errors
0	0	1	V_{PP} voltage error
0	1	0	WRITE error
0	1	1	WRITE error, V_{PP} voltage not valid
1	0	0	ERASE error
1	0	1	ERASE error, V_{PP} voltage not valid
1	1	0	Command sequencing error

NOTE: 1. SR3-SR5 must be cleared using CLEAR STATUS REGISTER.
2. SR3-SR4 reflect noncumulative results.

SELF-TIMED WRITE SEQUENCE[1]

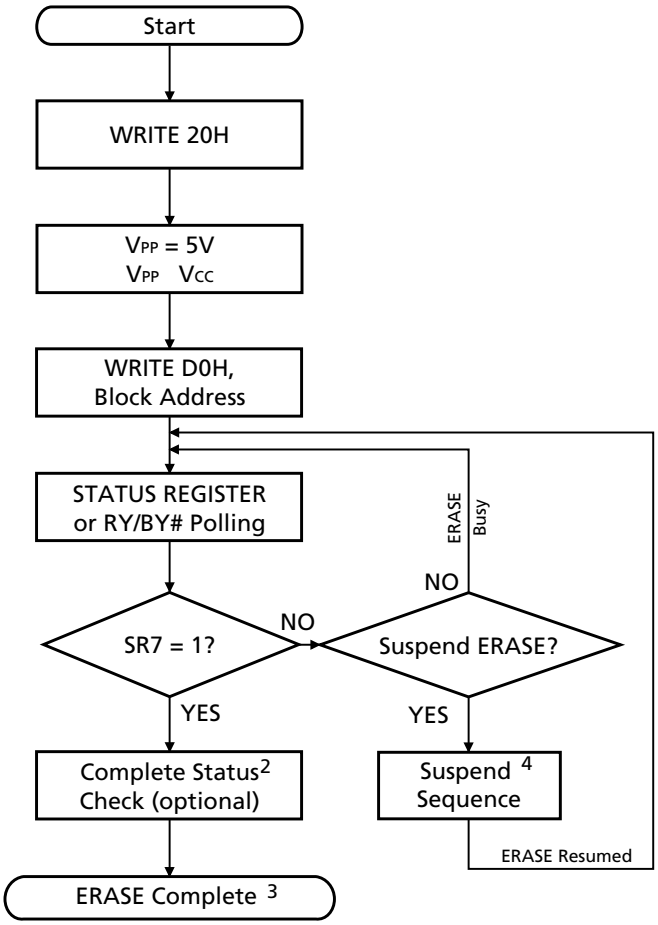


COMPLETE WRITE STATUS-CHECK SEQUENCE

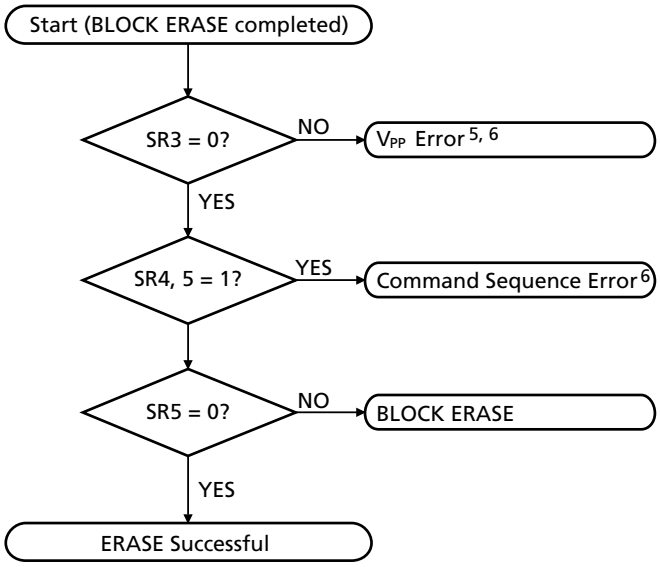


NOTE: 1. Sequence may be repeated for additional WRITEs.
2. Complete status check is not required.
3. Device will be in status register read mode. To return to the array read mode, the FFH command must be issued.
4. If SR3 is set during a WRITE or BLOCK ERASE attempt, CLEAR STATUS REGISTER (50H) should be issued before further WRITE or ERASE operations are attempted.
5. Status register bits 3-5 must be cleared using CLEAR STATUS REGISTER.

SELF-TIMED BLOCK ERASE SEQUENCE[1]

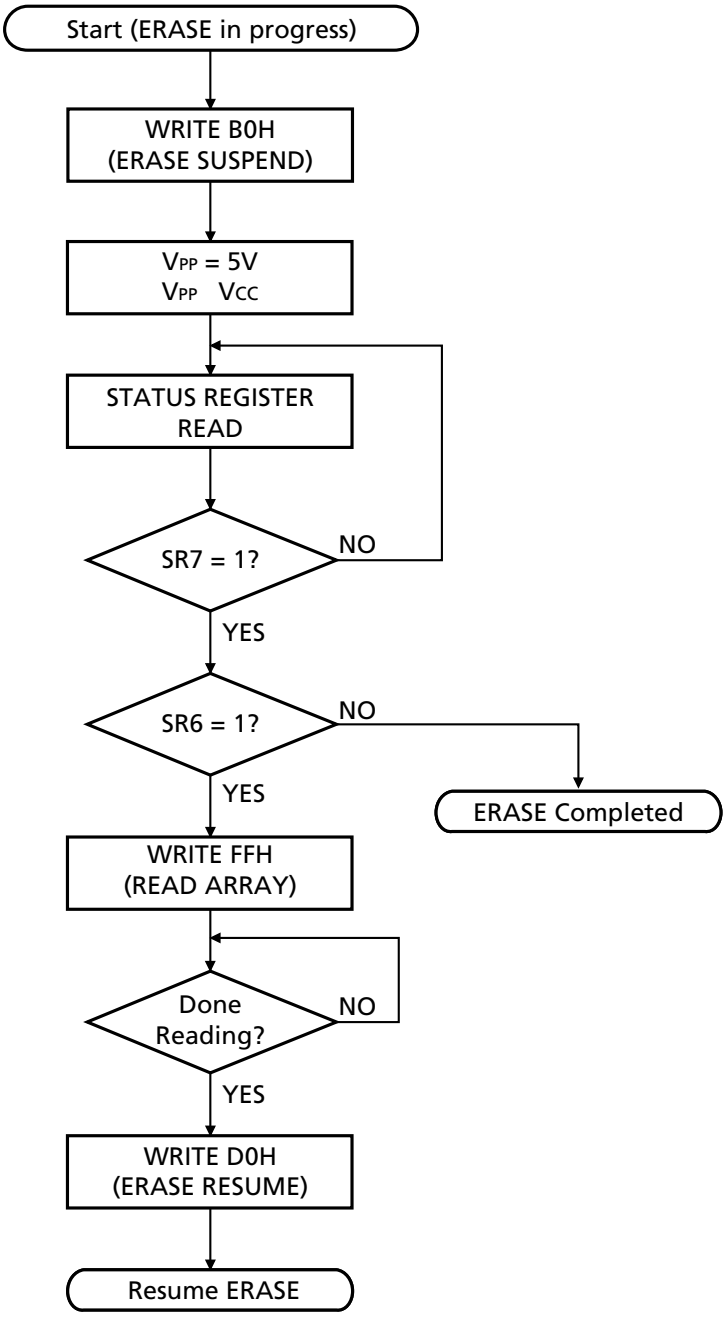


COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



NOTE:
1. Sequence may be repeated to erase additional blocks.
2. Complete status check is not required.
3. To return to the array read mode, the FFH command must be issued.
4. Refer to the ERASE SUSPEND flowchart for more information.
5. If SR3 is set during a WRITE or BLOCK ERASE attempt, CLEAR STATUS REGISTER (50H) should be issued before further WRITE or ERASE operations are attempted.
6. Status register bits 3-5 must be cleared using CLEAR STATUS REGISTER.

ERASE SUSPEND SEQUENCE



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply
Relative to V_{SS} ..... -0.5V to +6V**
Input Voltage Relative to V_{SS} ..... -0.5V to +6V**
V_{PP} Voltage Relative to V_{SS} ..... -0.5V to +12.6V†
Temperature Under Bias ..... -10°C to +80°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**V_{CC}, input and I/O pins may transition to -2V for <20ns and V_{CC} + 2V for <20ns.
†Voltage may pulse to -2V for <20ns and 14V for <20ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC READ OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
5V Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2	V_{CC} + 0.5	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	1

DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS (TTL) Output High Voltage (I_{OH} = -2.5mA)	V_{OH1}	2.4	–	V	1
Output Low Voltage (I_{OL} = 5.8mA)	V_{OL}	–	0.45	V	
OUTPUT VOLTAGE LEVELS (CMOS) Output High Voltage (I_{OH} = -100µA)	V_{OH2}	V_{CC} - 0.4	–	V	1
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); All other pins not under test = 0V	I_L	-1	1	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	

NOTE: 1. All voltages referenced to V_{SS}.

CAPACITANCE

(T_A = +25°C; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_I	8	pF	
Output Capacitance	C_O	12	pF	

READ AND STANDBY CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	TYP	MAX	UNITS	NOTES
READ CURRENT: TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}; f = 8 MHz; Other inputs = V_{IL} or V_{IH}; $\overline{RP}$ = V_{IH})	I_{CC1}	8	50	mA	1, 2
READ CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; $\overline{OE}$ • V_{CC} - 0.2V; f = 8 MHz; Other inputs ≤ 0.2V or • V_{CC} - 0.2V; $\overline{RP}$ = V_{CC} - 0.2V)	I_{CC2}	5	35	mA	1, 2
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RP}$ = V_{IH}; Other inputs = V_{IL} or V_{IH})	I_{CC3}	0.2	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RP}$ = V_{CC} - 0.2V)	I_{CC4}	65	100	µA	
DEEP POWER-DOWN CURRENT: V_{CC} SUPPLY ($\overline{RP}$ = V_{SS} ±0.2V)	I_{CC5}	1	20	µA	
STANDBY OR READ CURRENT: V_{PP} SUPPLY (V_{PP} • V_{CC})	I_{PP1}	±2	±15	µA	
DEEP POWER-DOWN CURRENT: V_{PP} SUPPLY ($\overline{RP}$ = V_{SS} ±0.2V)	I_{PP2}	2	5	µA	

NOTE: 1. I_{CC} is dependent on cycle rates.
2. I_{CC} is dependent on output loading. Specified values are obtained with the outputs open.

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

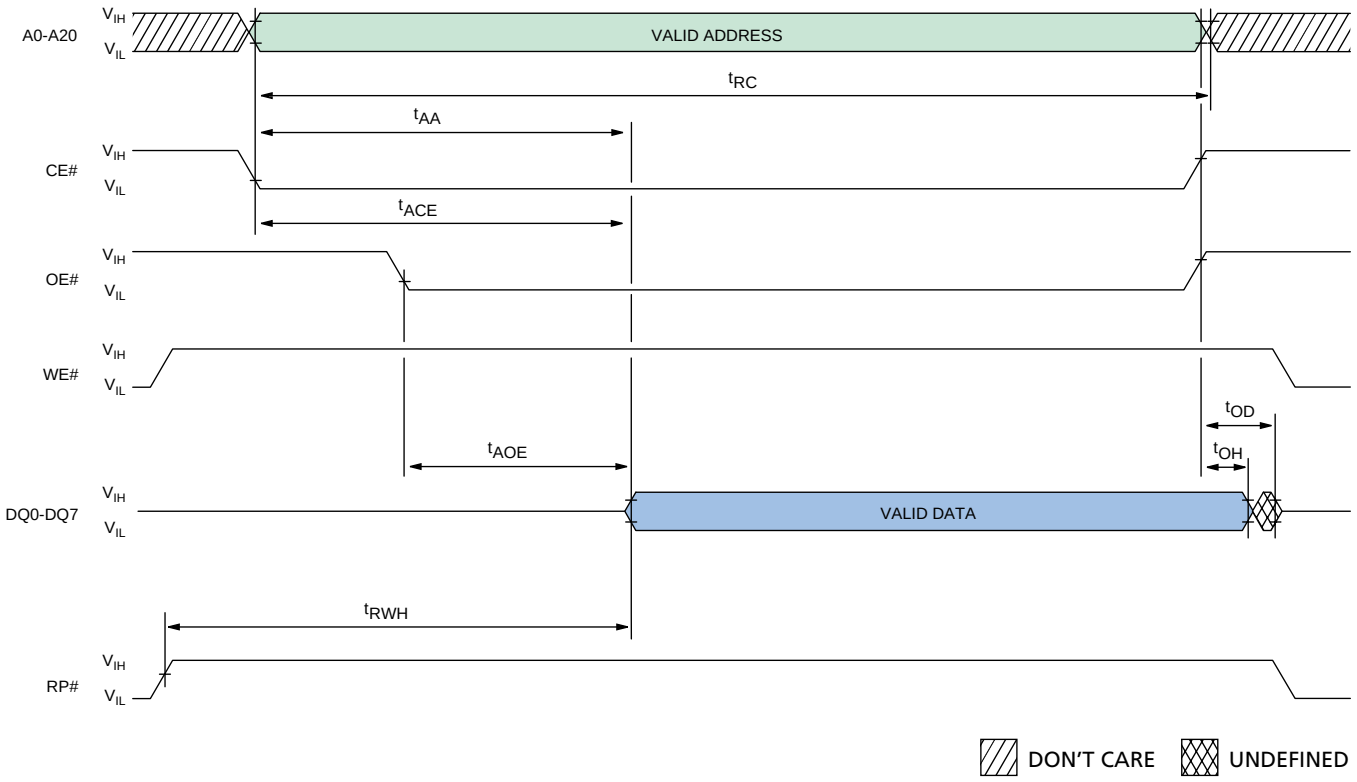
AC CHARACTERISTICS		-9			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ cycle time	^tRC	90		ns	
Access time from CE#	^tACE		90	ns	1
Access time from OE#	^tAOE		45	ns	1
Access time from address	^tAA		90	ns	
RP# HIGH to output valid delay	^tRWH		400	ns	
OE# or CE# HIGH to output in High-Z	^tOD		20	ns	
Output hold time from OE#, CE# or address change	^tOH	0		ns	

NOTE: 1. OE# may be delayed by ^tACE minus ^tAOE after CE# falls before ^tACE is affected.

AC TEST CONDITIONS

Input pulse levels	0.4V to 2.4V
Input rise and fall times	<10ns
Input timing reference level	0.8V and 2V
Output timing reference level	0.8V and 2V
Output load	1 TTL gate and C_L = 100pF

READ CYCLE



TIMING PARAMETERS

SYMBOL	-9 MIN	-9 MAX	UNITS
tRC	90		ns
tACE		90	ns
tAOE		45	ns
tAA		90	ns

SYMBOL	-9 MIN	-9 MAX	UNITS
tRWH		400	ns
tOD		20	ns
tOH	0		ns

RECOMMENDED DC WRITE/ERASE CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
V_{PP} WRITE/ERASE lockout voltage	V_{PPLK}	–	1.5	V	1
V_{PP} voltage during WRITE/ERASE operation	V_{PPH}	4.5	5.5	V	2
V_{CC} WRITE/ERASE lockout voltage	V_{LKO}	2	–	V	

WRITE/ERASE CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%; V_{PP} = +5V ±10% [Note 2])

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
WRITE CURRENT: V_{CC} SUPPLY	I_{CC6}	35	mA	3
WRITE CURRENT: V_{PP} SUPPLY	I_{PP3}	40	mA	3
ERASE CURRENT: V_{CC} SUPPLY	I_{CC7}	30	mA	3
ERASE CURRENT: V_{PP} SUPPLY	I_{PP4}	20	mA	3
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (ERASE suspended)	I_{CC8}	10	mA	3, 4
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (ERASE suspended)	I_{PP5}	200	µA	

NOTE:
1. Absolute WRITE/ERASE protection when $V_{PP} \leq V_{PPLK}$.
2. For SmartVoltage-compatible production programming, 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 100 cumulative hours.
3. Sampled, not tested, 100%.
4. Parameter is specified when device is not accessed. Actual current draw will be I_{CC8} (5V V_{CC}) plus current of operation being executed while the device is in suspend mode.

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: WE# (CE#)-CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-9		
PARAMETER	**SYMBOL**	**MIN**	**UNITS**	**NOTES**
WRITE cycle time	^tWC	90	ns	
WE# (CE#) HIGH pulse width	^tWPH (^tCPH)	25	ns	
WE# (CE#) pulse width	^tWP (^tCP)	50	ns	
Address setup time to WE# (CE#) HIGH	^tAS	40	ns	
Address hold time from WE# (CE#) HIGH	^tAH	5	ns	
Data setup time to WE# (CE#) HIGH	^tDS	40	ns	
Data hold time from WE# (CE#) HIGH	^tDH	5	ns	
CE# (WE#) setup time to WE# (CE#) LOW	^tCS (^tWS)	0	ns	
CE# (WE#) hold time from WE# (CE#) HIGH	^tCH (^tWH)	0	ns	
V_{PP} setup time to WE# (CE#) HIGH	^tVPS	100	ns	
RP# HIGH to WE# (CE#) LOW delay	^tRS	1,000	ns	
WRITE duration	$^tWED1$	6	µs	
BLOCK ERASE duration	$^tWED2$	600	ms	
WRITE recovery to READ	^tWR	0	ns	
V_{PP} hold time from status data valid, RY/BY# HIGH	^tVPH	0	ns	
WE# (CE#) HIGH to RY/BY# LOW	^tRYBY	90	ns	
WE# (CE#) HIGH to busy status (SR7 = 0)	^tWB	200	ns	

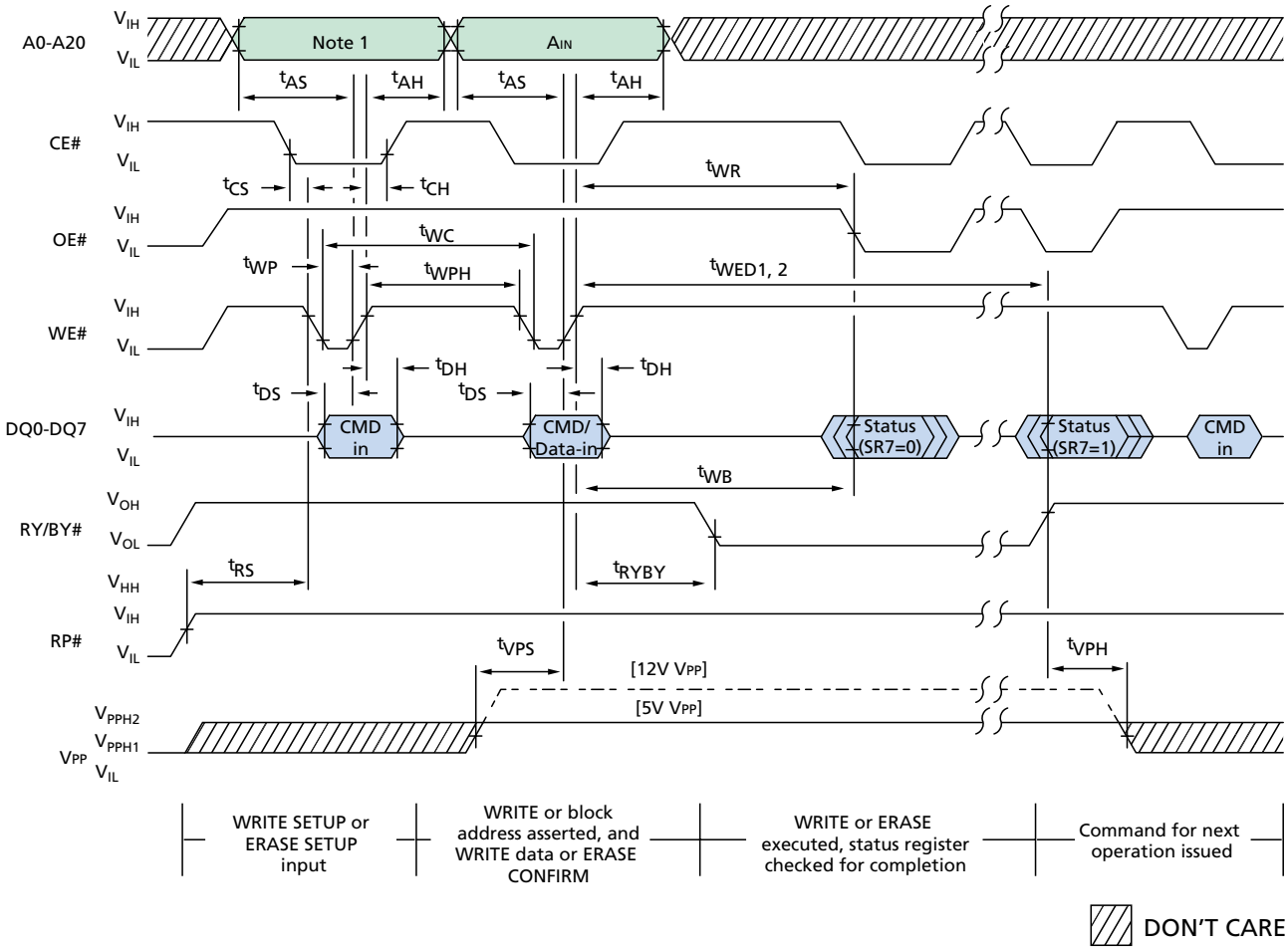
WRITE AND ERASE DURATION CHARACTERISTICS

	5V V_{PP}			
PARAMETER	**TYP**	**MAX**	**UNITS**	**NOTES**
WRITE time	8	TBD	µs	1
BLOCK ERASE time	0.5	TBD	s	1
BLOCK WRITE time	0.5	TBD	s	1, 2, 3
ERASE SUSPEND latency to READ	9	12	µs	1

NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.
3. Typical WRITE times use checkerboard data pattern.

WRITE/ERASE CYCLE

WE#-CONTROLLED WRITE/ERASE



TIMING PARAMETERS

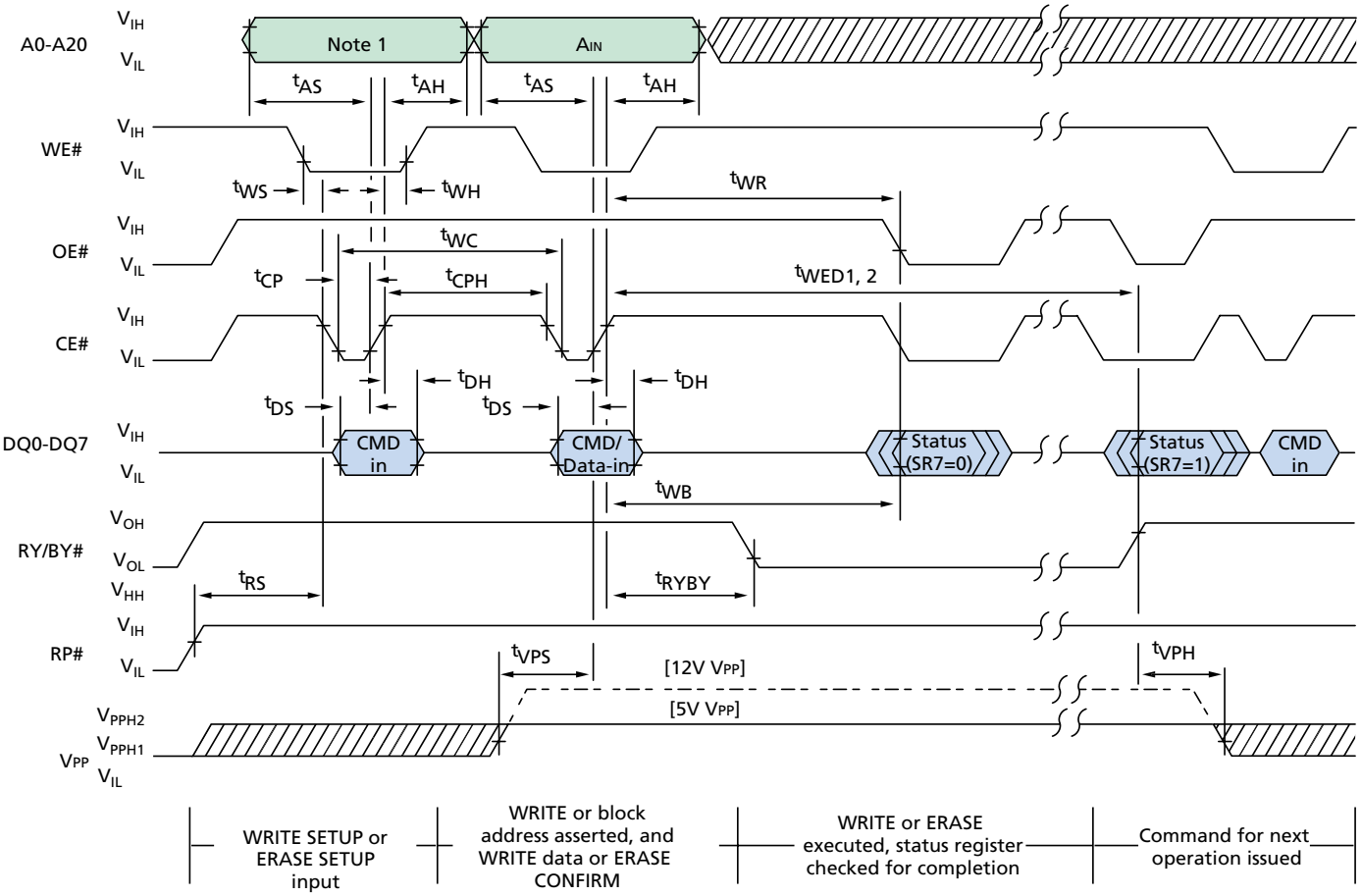
SYMBOL	-9 MIN	UNITS
tWC	90	ns
tWPH	25	ns
tWP	50	ns
tAS	40	ns
tAH	5	ns
tDS	40	ns
tDH	5	ns
tCS	0	ns
tCH	0	ns

SYMBOL	-9 MIN	UNITS
tVPS[2]	100	ns
tRS	1,000	ns
tVPH[2]	0	ns
tRYBY	90	ns
tWB	200	ns
tWED1	6	µs
tWED2	600	ms
tWR	0	ns

NOTE: 1. Address inputs are "Don't Care" but must be held stable.
2. Measured with $V_{PP} = V_{PPH} = 5V$.

WRITE/ERASE CYCLE

CE#-CONTROLLED WRITE/ERASE



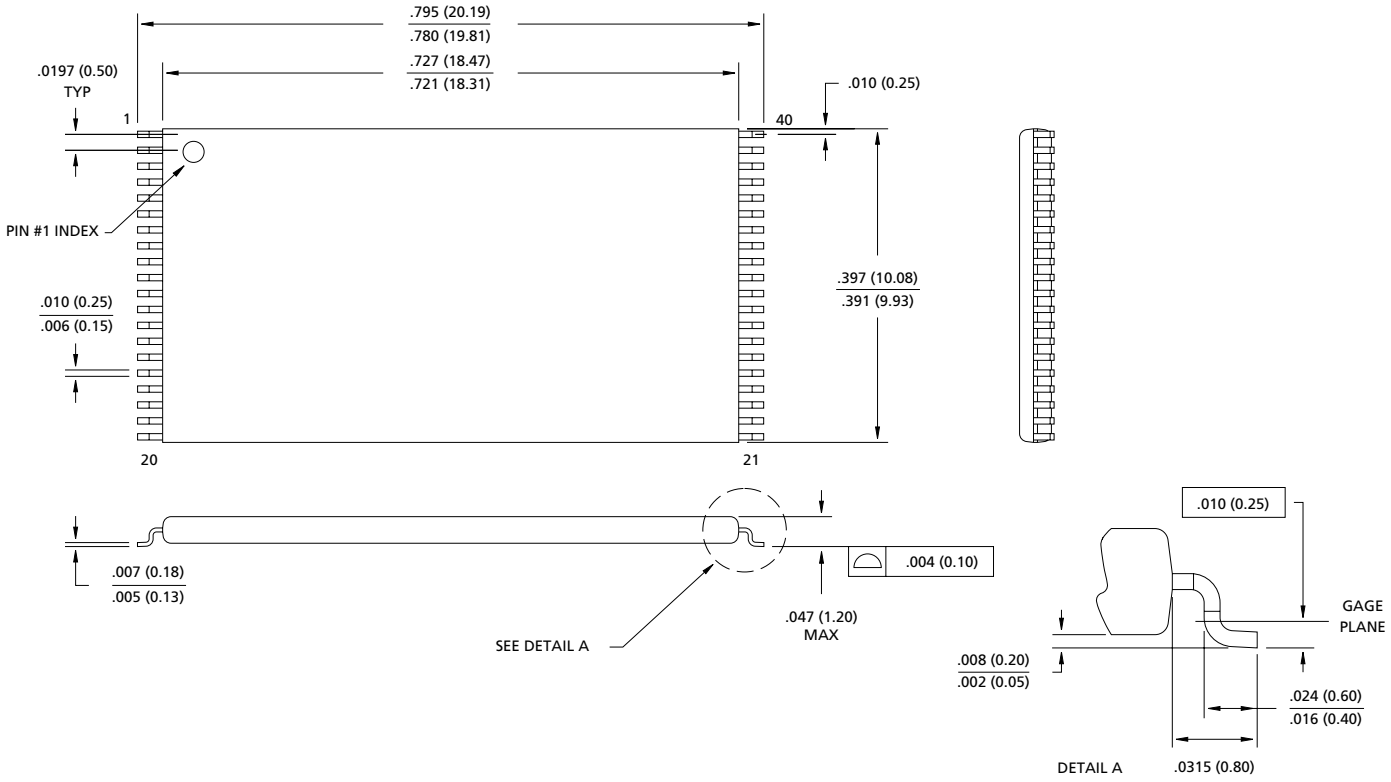
TIMING PARAMETERS

SYMBOL	-9 MIN	UNITS
tWC	90	ns
tCPH	25	ns
tCP	50	ns
tAS	40	ns
tAH	5	ns
tDS	40	ns
tDH	5	ns
tWS	0	ns
tWH	0	ns

SYMBOL	-9 MIN	UNITS
tVPS[2]	100	ns
tRS	1,000	ns
tVPH[2]	0	ns
tRYBY	90	ns
tWB	90	ns
tWED1	6	µs
tWED2	600	ms
tWR	0	ns

NOTE: 1. Address inputs are "Don't Care" but must be held stable.
2. Measured with $V_{PP} = V_{PPH} = 5V$.

40-PIN PLASTIC TSOP I
(10mm x 20mm)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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