# TRI-STATE® 64-Bit Random Access Memories

## General Description

The DM76L99/DM86L99 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory, the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 75 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance state while the one selected memory exhibits the normal totem-pole, low impedance output characteristics of TTL.

## Features

- Same pin-out as SN5489/SN7489, 3101, MM5501
- Organized as 16, 4-bit words
- Expandable to 1200, 4-bit words without additional resistors
- Typical access from chip enable       50 ns
- Typical access time       80 ns
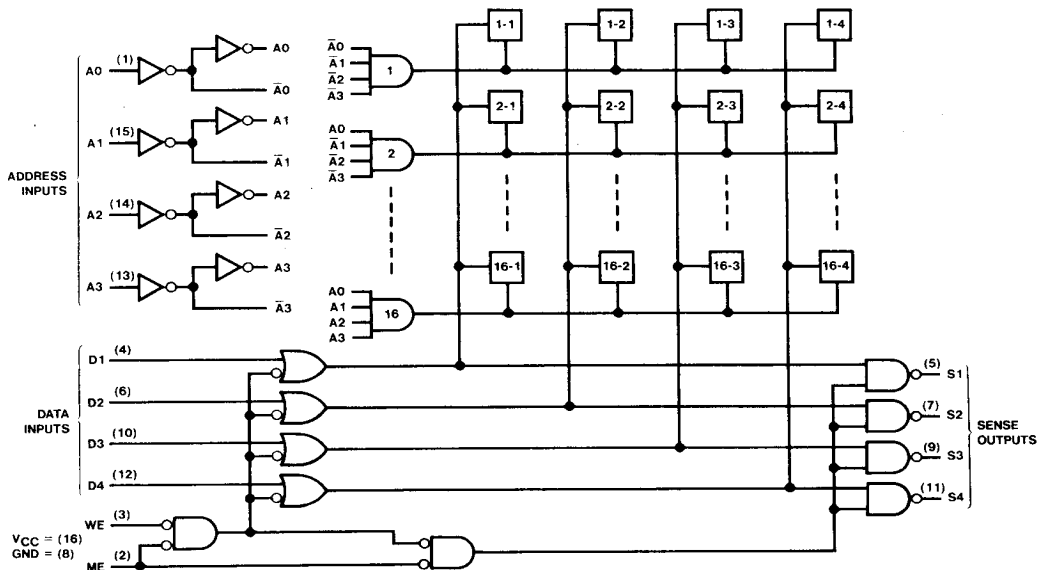- Typical power dissipation       75 mW

## Connection Diagram
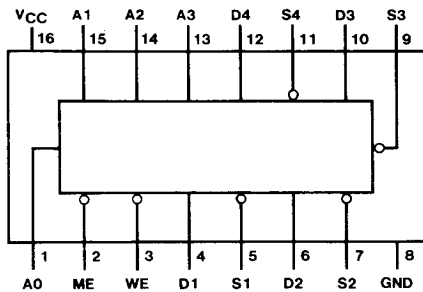


76L99 (J,W); 86L99 (N)

## Truth Table

| Memory Enable | Write Enable | Operation | Outputs |
|---|---|---|---|
| L | L | Write | Hi-Z |
| L | H | Read | Complement of Data Stored in Memory |
| H | X | Hold | Hi-Z |

## Logic Diagram

## Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

| Parameter | | Conditions | | DM76/86 L99 | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ (1) | Max | |
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = Min | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = Min | | | | 0.7 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $I_{OH}$ | High Level Output Current | | | | | −1.0 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = −1.0 mA | | 2.4 | | | V |
| $I_{OL}$ | Low Level Output Current | | DM76L | | | 2.0 | mA |
| | | | DM86L | | | 3.6 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min $I_{OL}$ = Max | DM76L | | | 0.3 | V |
| | | | DM86L | | | 0.4 | |
| $I_{O(OFF)}$ | Off State (High Impedance State) Output Current | $V_{CC}$ = Max | $V_O$ = 0.3 V | | | −40 | μA |
| | | | $V_O$ = 2.4 V | | | 40 | |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5 V | | | | 100 | μA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4 V | | | | 10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.3 V | | | | −180 | μA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (2) | | −6 | | −30 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max | | | 15 | 19 | mA |

**Note 1:** All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
**Note 2:** Not more than one output should be shorted at a time.

## Switching Characteristics $V_{CC}$ = 5 V, $T_A$ = 25°C

| Parameter | | | From | To | Conditions | DM76/86 L99 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ (1) | Max | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | | Address | Output | $C_L$ = 50 pF, $R_L$ = 4 kΩ | | 51 | 120 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | | Address | Output | | | 77 | 150 | ns |
| $t_{EN}$ | Output Disable Time from Write Enable | | WE | Output | | | 73 | 110 | ns |
| $t_{SR}$ | Sense Recovery Time from Write Enable | | WE | Output | | | 110 | 165 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | ME | Output | | | 30 | 50 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | ME | Output | | | 29 | 43 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | ME | Output | $C_L$ = 5 pF, $R_L$ = 4 kΩ | | 18 | 27 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | | ME | Output | | | 37 | 56 | ns |
| $t_{SETUP}$ | Setup Time | Data | | | | 0 | | | ns |
| | | Address | | | | 0 | | | |
| | | ME | | | | 0 | | | |
| $t_{HOLD}$ | Hold Time | Data | | | | 0 | | | ns |
| | | Address | | | | 0 | | | |
| | | ME | | | | 0 | | | |
| $t_{WP}$ | Write Enable Pulse Width | | | | | 50 | 30 | | ns |

## AC Test Circuit
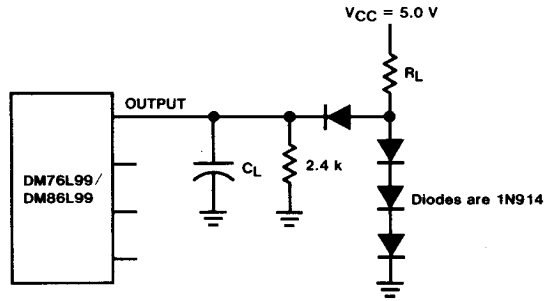


## Switching Time Waveforms
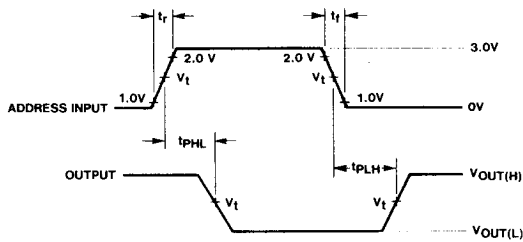


**WRITE CYCLE**

**MEMORY ENABLE**

$t_{LZ}$ & $t_{HZ}$
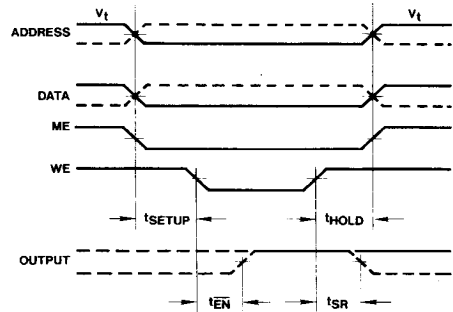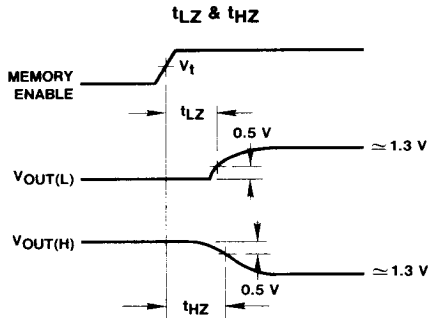
$t_{ZL}$ & $t_{ZH}$
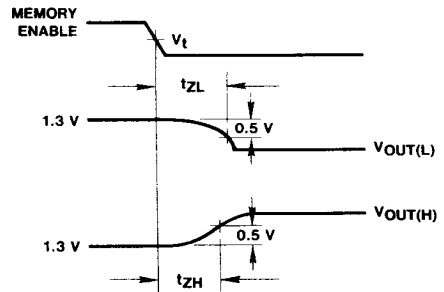
Note: The pulse generator has the following characteristics: $V = 3.0$ V, $t_r = 15$ ns, $t_f = 5.0$ ns, $f = 500$ kHz, duty cycle = 50%, $Z_{OUT} = 50 \Omega$, $V_t = 1.3$ V @ 25°C.

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