

# FT8010

## Reset Timer with Configurable Delay Time

### Features

- Long Delay Configurable to 7.5 or 11.25 Seconds
- Primary and Secondary Input Reset Pins
- Push-Pull and Open-Drain Output Pins
- 1.8 V to 5.0 V Operation ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- 1.7 V to 5.0 V Operation ( $T_A = -25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- 1.65 V to 5.0 V Operation ( $T_A = 0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Packaged in 10-Lead UMLP (1.4 mm x 1.8 mm) and 8-Lead MLP (2.0 mm x 2.0 mm) Packages

### Description

The FT8010 is a timer for resetting a mobile device where long reset times are needed. The long time delay helps avoid unintended resets caused by accidental key presses. Two delays can be selected by hard-wiring the DSR pin:  $7.5 \pm 20\%$  seconds or  $11.25 \pm 20\%$  seconds.

The FT8010 has two identical inputs for single or dual switch resetting capability. The device has two outputs: a push-pull output with 0.5 mA drive and an open-drain output with 0.5 mA pull-down drive.

FT8010 draws minimal  $I_{CC}$  current when inactive and functions over a wide 1.65 V to 5.0 V power supply range.

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FT8010UMX	-40°C to +85°C	10-Lead, Ultrathin MLP, 1.4 x 1.8 x 0.55 mm Package, 0.40 mm Pitch	5000 Units Tape and Reel
FT8010MPX	-40°C to +85°C	8-Lead, MLP 2.0 x 2.0 x 0.8 mm Package, 0.5 mm Pitch	3000 Units Tape and Reel

### Block Diagram

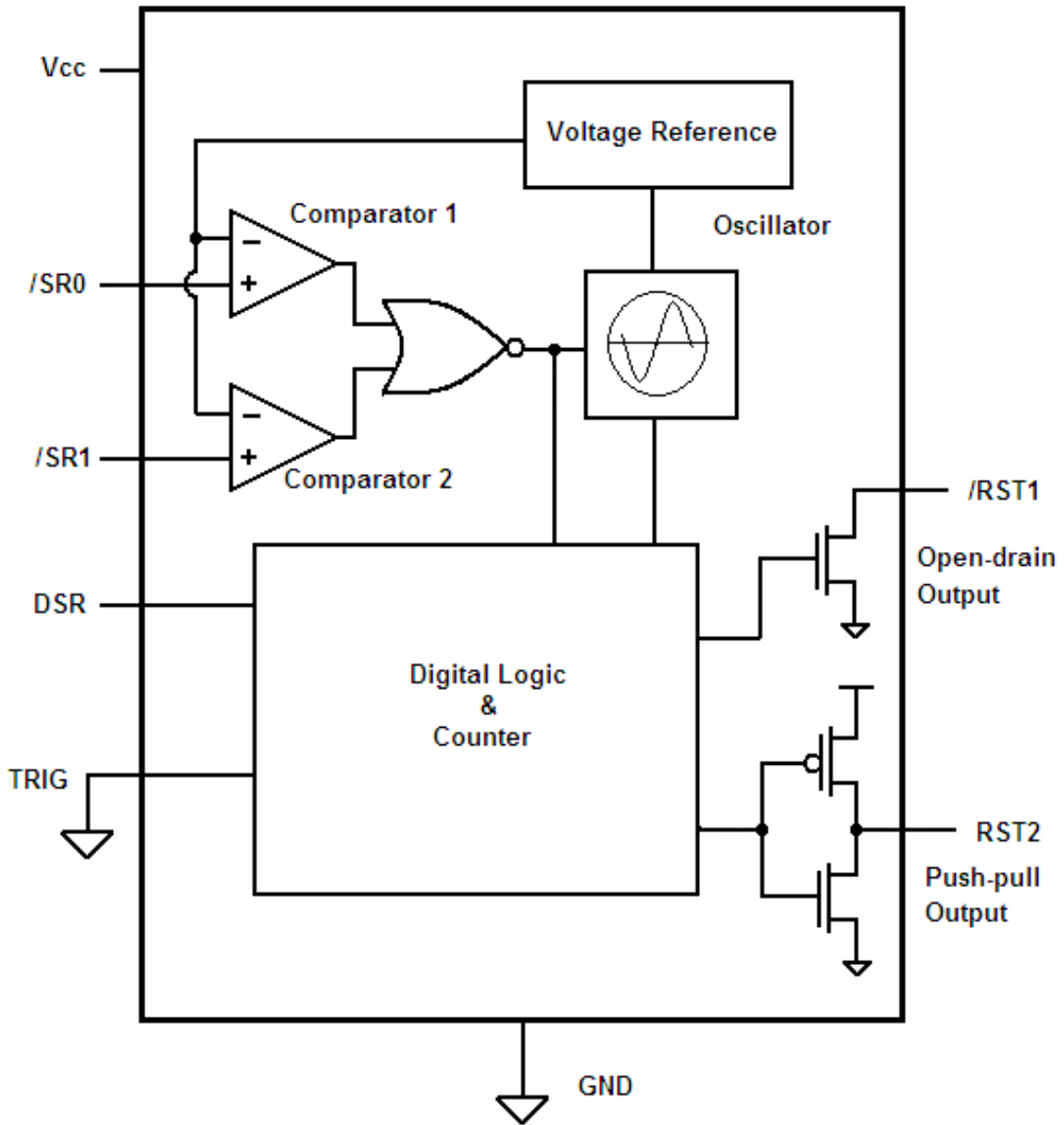


Figure 1. Block Diagram



## Pin Configuration

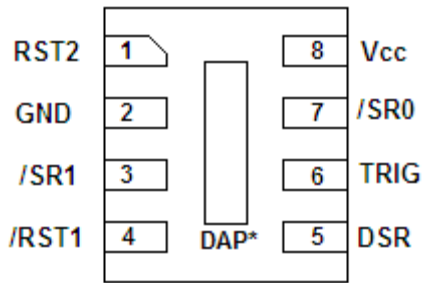


Figure 2. MLP Pin Configuration<sup>(1)</sup>  
(Top Through View)

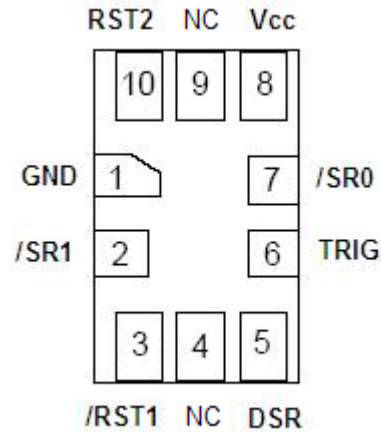


Figure 3. UMLP Pin Configuration<sup>(2)</sup>  
(Top Through View)

**Note:**

1. The DAP may be a no connect or it may be tied to ground.
2. NC = No connect

## Pin Definitions

MLP Pin #	UMLP Pin #	Name	Description
1	10	RST2	Push-Pull Output, Active HIGH
2	1	GND	Ground
3	2	/SR1	Secondary Reset Input, Active LOW
4	3	/RST1	Open-Drain Output, Active LOW
5	5	DSR	Delay Selection Input (Must be tied directly to GND or V <sub>CC</sub> ; do not use pull-up or pull-down resistors.)
6	6	TRIG	Test Pin, Tied to GND in Normal Use
7	7	/SR0	Primary Reset Input, Active LOW
8	8	V <sub>CC</sub>	Power Supply
	4, 9,	NC	No Connect

## Functional Description

The FT8010 reset timer uses an internal oscillator and a two-stage, 21-bit counter to determine when the output pins switch. Time N is set by the hard-wired logic level of the DSR pin. N is either 7.5 ±20% seconds for DSR=LOW or 11.25 ±20% seconds for DSR=HIGH.

**Table 1. FT8010 Truth Table**

DSR	Reset Timer ( +-20% )
0	7.50s
1	11.25s

The two input pins, /SR0 and /SR1, drive voltage comparators that compare the voltage on the input with the voltage set by the reference block. A low input signal on both /SR0 and /SR1 starts the oscillator. The oscillator sends data pulses to the digital core, which includes the counter. There are two scenarios for counting, as described below: short duration and long duration. In the short-duration scenario, outputs /RST1 and RST2 are not affected. In the long duration scenario, the outputs change state after time N. The outputs return to their original states when a HIGH input signal occurs on either /SR0 or /SR1.

The /RST1 output is an open-drain driver. When the count time exceeds time N, the /RST1 output drives LOW. The RST2 output is a push-pull driver. When the count time exceeds time N, the RST2 output drives HIGH.



The TRIG pin should be tied GND or LOW during normal operation. The TRIG pin is a test mode pin used for SCAN testing.

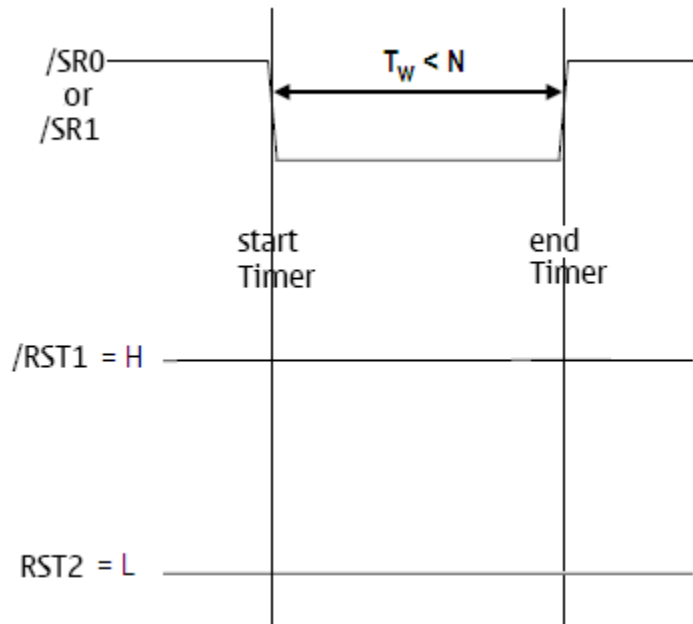
### Application Note

**IMPORTANT:** The DSR pin must be tied to V<sub>CC</sub> or GND to provide a HIGH or LOW voltage level. The voltage level on the DSR pin determines the length of the configurable delay. It is important that the voltage level on the DSR pin not change during normal operation. The DSR pin must be tied directly to V<sub>CC</sub> or GND before SR0 or SR1 buttons go LOW. Do not use pull-up or pull-down resistors on the DSR pin.

### Short Duration ( $t_w < N$ )

In this case, both input /SR0 and /SR1 are LOW for a duration  $t_w$  which is shorter than time N. When an input goes LOW, the internal timer starts counting. The input goes HIGH before time N. The timer stops counting and resets and no changes occur on the outputs (see Figure 4).

/SR0	/SR1	/RST1	/RST2	Description
	L	H	L	The timer starts counting when both inputs go LOW. The timer stops counting and resets when either input goes HIGH. No changes occur on the outputs, Both /SR0 and /SR1 need to be LOW to activate (start) the timer.
L		H	L	



**Figure 4. Short Duration Waveform**

### Long Duration ( $t_w > N$ )

In this case, inputs /SR0 and /SR1 are LOW for a duration,  $t_w$ , which is longer than time N. When an input goes LOW, the internal timer starts counting. After time N, the outputs switch and the timer stops counting. The input goes HIGH sometime after N

seconds. When the input goes HIGH, the timer resets and the outputs switch back to their original state after a propagation delay (see Figure 5).

/SR0	/SR1	/RST1	RST2	Description
	L			The timer starts counting when both inputs go LOW. After time N, the outputs switch. When either input goes HIGH, the timer resets and the outputs switch back to their original state. Both /SR0 and /SR1 need to be LOW to activate (start) the timer.
L				

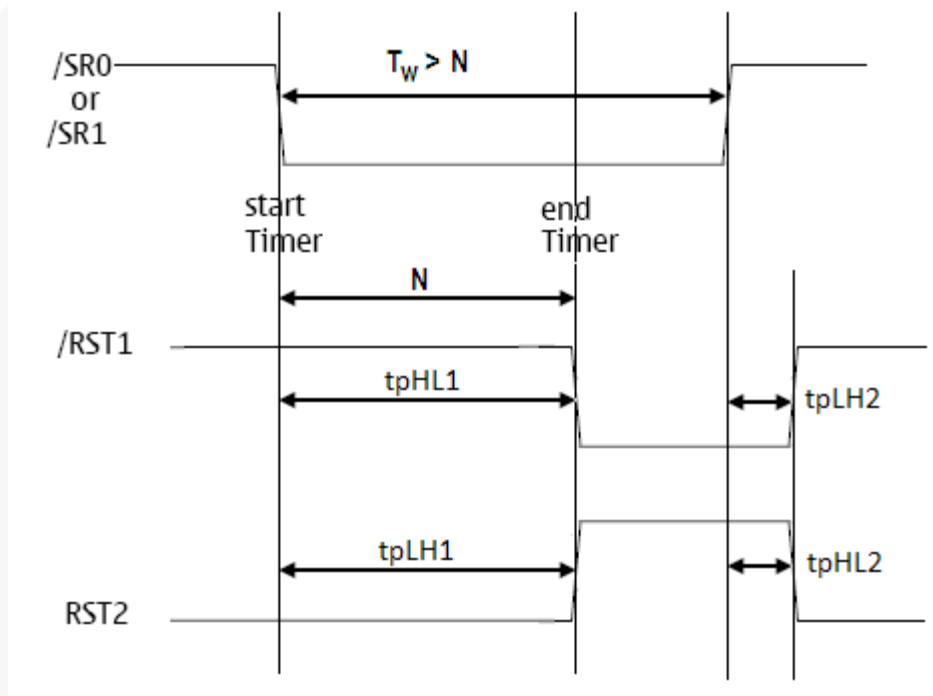


Figure 5. Long Duration Waveform

**Note:**

- Waveforms not drawn to scale ( $tp_{HL1}, tp_{LH1} \gg tp_{HL2}, tp_{LH2}$ ).



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
$V_{CC}$	Supply Voltage		-0.5	7	V
$V_{IN}$	DC Input Voltage	/SR0, /SR1, TRIG, DSR	-0.5	7	V
$V_{OUT}$	Output Voltage <sup>(4)</sup>	/RST1 HIGH or LOW	-0.5	7	V
		RST2 HIGH or LOW	-0.5	$V_{CC}+0.5$	
		/RST1, RST2, $V_{CC}=0$	-0.5	7	
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0$ V		-50	mA
$I_{OK}$	DC Output Diode Current	$V_{OUT} < 0$ V		-50	mA
		$V_{OUT} > V_{CC}$		+50	
$I_{OH}/I_{OL}$	DC Output Source/Sink Current		-50	+50	mA
$I_{CC}$	DC $V_{CC}$ or Ground Current per Supply Pin			$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		-65	+150	°C
$T_J$	Junction Temperature under Bias			+150	°C
$T_L$	Junction Lead Temperature, Soldering 10 Seconds			+260	°C
$P_D$	Power Dissipation			5	mW
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4	kV
		Charged Device Model, JESD22-C101		2	

**Note:**

- $I_O$  absolute maximum rating must be observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	-40°C to +85°C	1.8	5.0	V
		-25°C to +85°C	1.7	5.0	
		0°C to +85°C	1.65	5.00	
t <sub>RFC</sub>	V <sub>CC</sub> Recovery Time After Power Down	V <sub>CC</sub> =0 V After Power Down, Rising to 0.5 V	5		ms
V <sub>IN</sub>	Input Voltage	/SR0, /SR1	0	5	V
V <sub>OUT</sub>	Output Voltage	/RST1 HIGH or LOW	0	5	V
		RST2 HIGH or LOW	0	V <sub>CC</sub>	
		/RST1, RST2, V <sub>CC</sub> =0 V	0	5	
I <sub>OH</sub>	DC Output Source Current	RST2, 1.8 V ≤ V <sub>CC</sub> ≤ 3.0 V	-0.1		mA
		RST2, 3.0 V ≤ V <sub>CC</sub> ≤ 5.0 V	-0.5		
I <sub>OL</sub>	DC Output Sink Current	/RST1, RST2, V <sub>CC</sub> =1.8 V to 5.0 V	+0.5		
T <sub>A</sub>	Free Air Operating Temperature		-40	+85	°C
Θ <sub>JA</sub>	Thermal Resistance	MLP-8		245	°C/W
		UMLP-10		200	

### Note:

5. All unused inputs must be held at V<sub>CC</sub> or GND.

## DC Electrical Characteristics

Unless otherwise specified, conditions of T<sub>A</sub>=-40 to 80°C with V<sub>CC</sub>=1.8 - 5.0V OR T<sub>A</sub>=-25 to 85°C with V<sub>CC</sub>=1.7 - 5V OR T<sub>A</sub>=0 to 85°C with V<sub>CC</sub>=1.65 - 5V produce the performance characteristics below.

Symbol	Parameter	Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	/SR0, /SR1	1.2		V
		DSR	0.65 x V <sub>CC</sub>		
V <sub>IL</sub>	Input Low Voltage	/SR0, /SR1		0.32	V
		DSR		0.25 x V <sub>CC</sub>	
V <sub>OH</sub>	High Level Output Voltage	RST2, I <sub>OH</sub> =-100 μA	0.8 x V <sub>CC</sub>		V
		RST2, I <sub>OH</sub> =-500 μA V <sub>CC</sub> =3.0 to 5.0 V	0.8 x V <sub>CC</sub>		
V <sub>OL</sub>	Low Level Output Voltage	RST2, I <sub>OL</sub> =500 μA		0.3	V
		/RST1, I <sub>OL</sub> =500 μA		0.3	
I <sub>IN</sub>	Input Leakage Current	0 V ≤ V <sub>IN</sub> ≤ 5.0 V		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current (Timer Inactive)	/SR0 or /SR1=V <sub>CC</sub>		20	μA
	Dynamic Supply Current (Timer Active)	/SR0=/SR1=0 V		100	

## AC Electrical Characteristics

Unless otherwise specified, conditions of  $T_A = -40$  to  $80^\circ\text{C}$  with  $V_{CC} = 1.8 - 5.0\text{V}$  OR  $T_A = -25$  to  $85^\circ\text{C}$  with  $V_{CC} = 1.7 - 5\text{V}$  OR  $T_A = 0$  to  $85^\circ\text{C}$  with  $V_{CC} = 1.65 - 5\text{V}$  produce the performance characteristics below.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{PHL1}$	Timer Delay, /SRn to /RST1, (DSR=0)	$C_L = 5\text{ pF}$ , $R_L = 5\text{ k}\Omega$ See Figure 6	6.0	7.5	9.0	s
	Timer Delay, /SRn to /RST1, (DSR=1)	$C_L = 5\text{ pF}$ , $R_L = 5\text{ k}\Omega$ See Figure 6	9.00	11.25	13.50	s
$t_{PLH2}$	Propagation Delay, /SRn to /RST1, (DSR=0 or 1)	$C_L = 5\text{ pF}$ , $R_L = 5\text{ k}\Omega$ See Figure 6		220	310	ns
$t_{PLH1}$	Timer Delay, /SRn to RST2, (DSR=0)	$C_L = 5\text{ pF}$ , $R_L = 10\text{ k}\Omega$ See Figure 7	6.0	7.5	9.0	s
	Timer Delay, /SRn to RST2, (DSR=1)	$C_L = 5\text{ pF}$ , $R_L = 10\text{ k}\Omega$ See Figure 7	9.00	11.25	13.50	s
$t_{PHL2}$	Propagation Delay, /SRn to RST2, (DSR=0 or 1)	$C_L = 5\text{ pF}$ , $R_L = 10\text{ k}\Omega$ See Figure 7		210	300	ns

## Capacitance Specifications

$T_A = +25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = \text{GND}$	4.0	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 5.0\text{ V}$	5.0	pF



AC Test Circuit and Waveforms

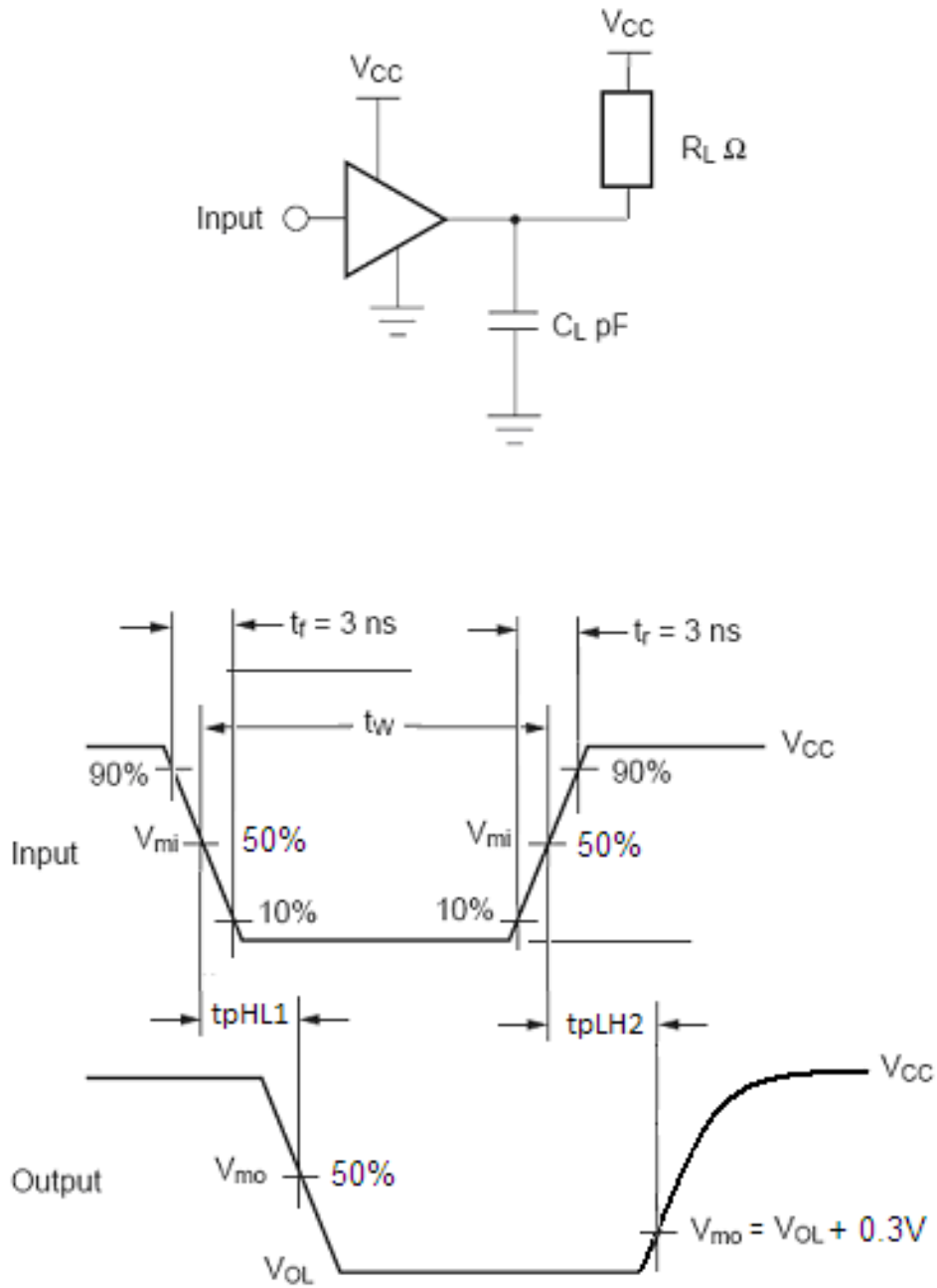


Figure 6. /RST1 Output

AC Test Circuit and Waveforms (Continued)

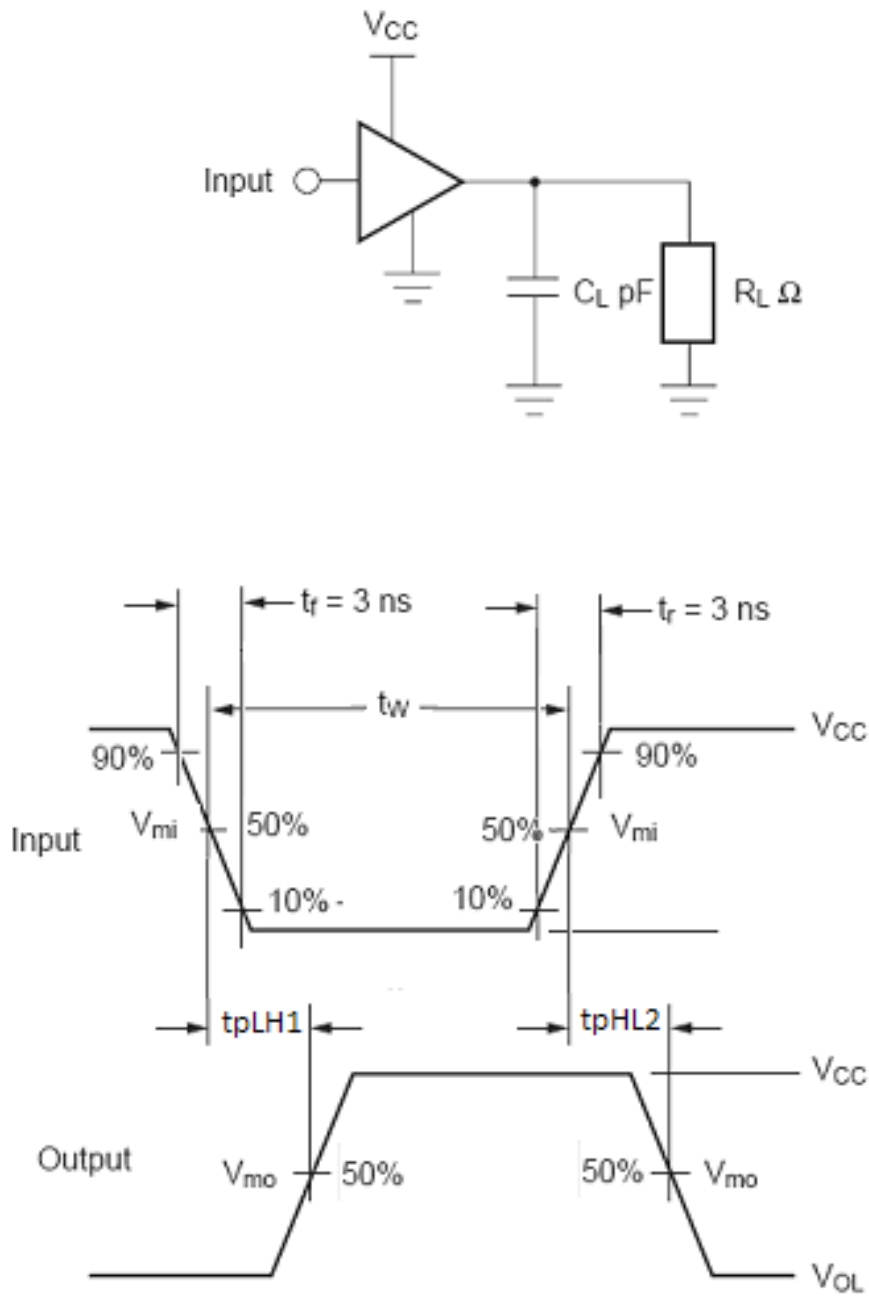


Figure 7. RST2 Output

Physical Dimensions

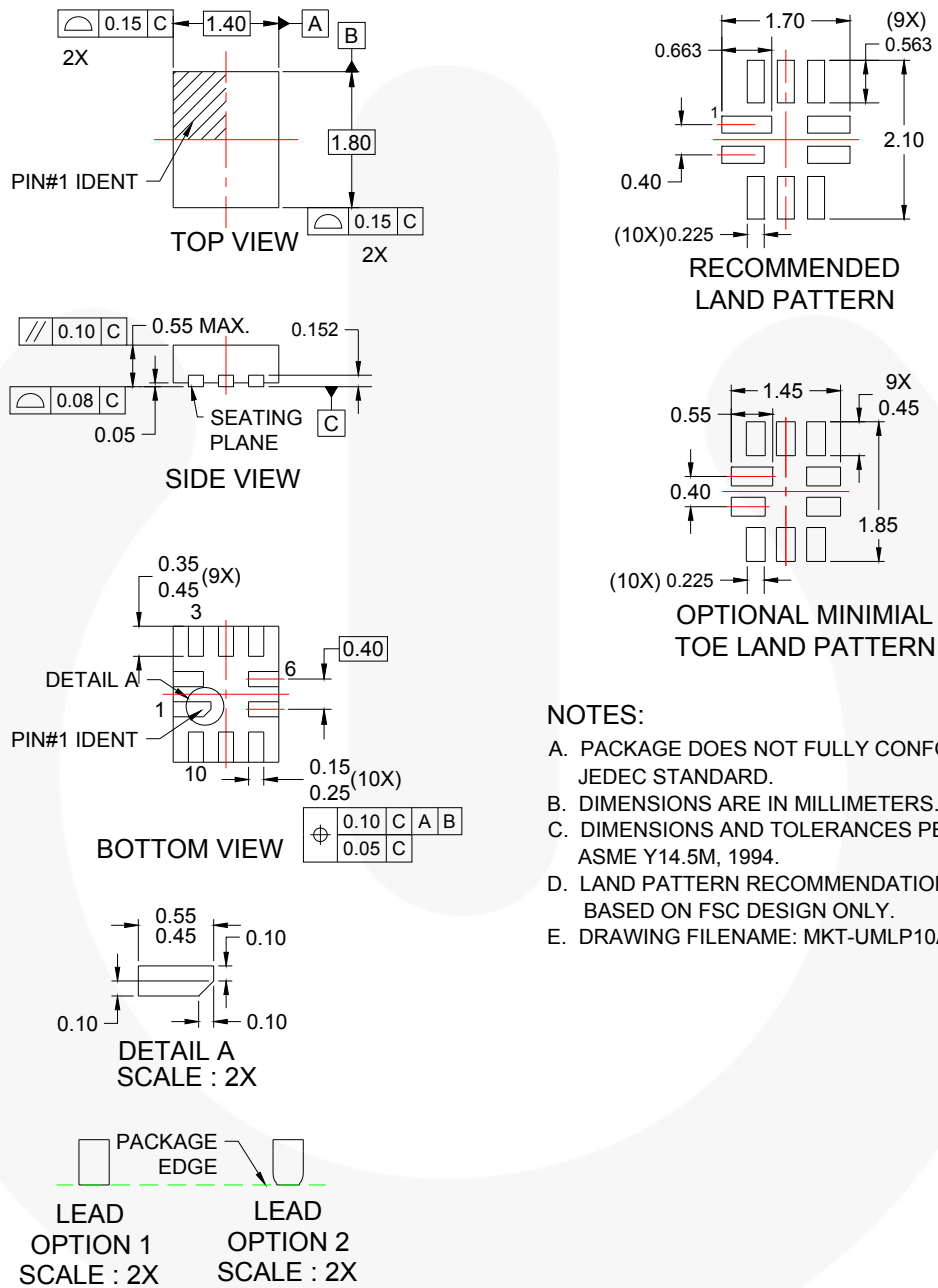
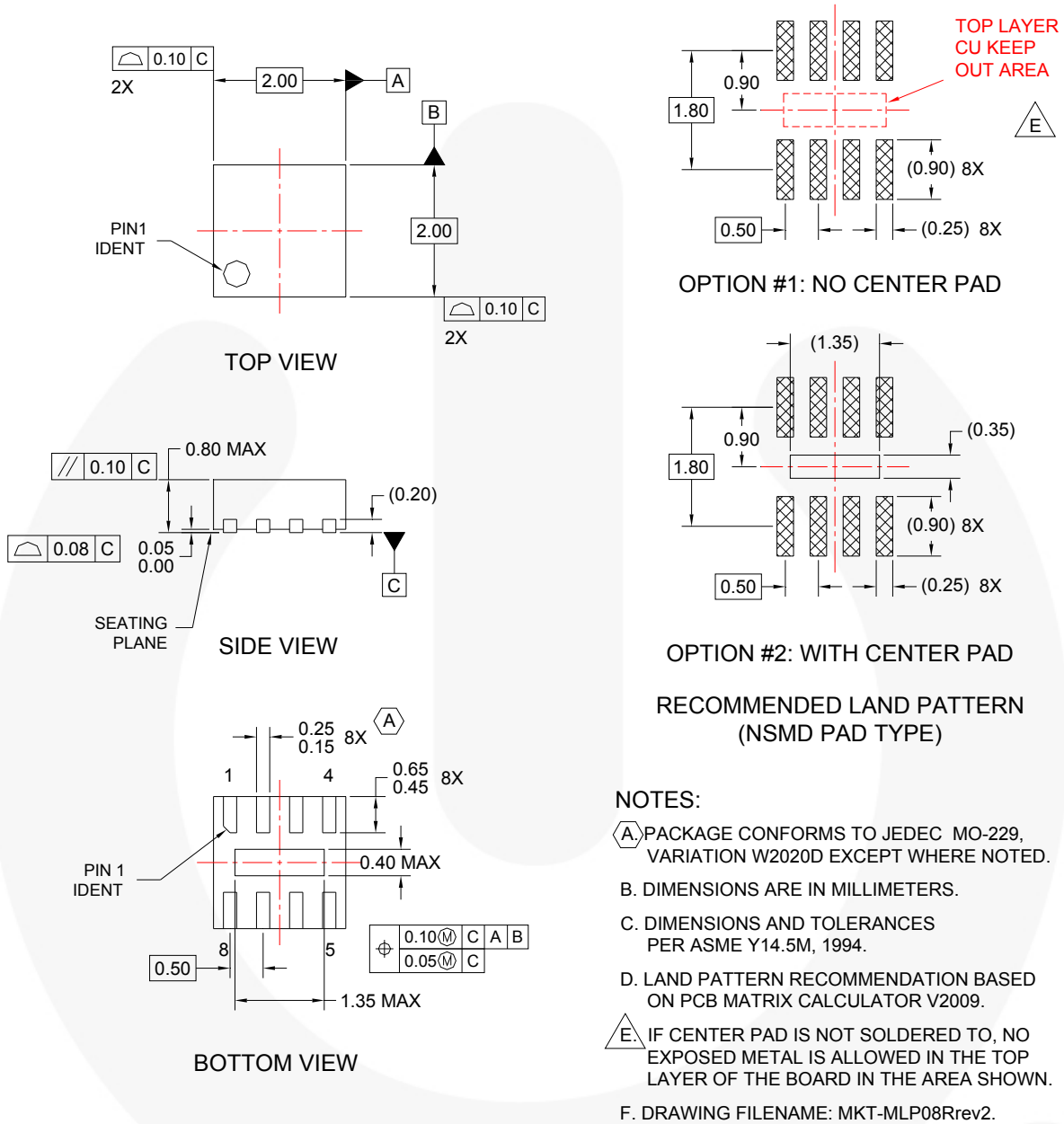


Figure 8. 10-Lead, Ultrathin MLP, 1.4 x 1.8 x 0.55 mm Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>

**Physical Dimensions (Continued)**



**Figure 9. 8-Lead, Molded Leadless Package (MLP), 2.0 x 2.0 x 0.8 mm**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>.



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |  |   |   |   |
|--|---|---|---|
| 2Cool™   | F-PFS™  | PowerTrench®  | The Power Franchise®  |
| AccuPower™   | FRFET®  | PowerXS™  | <b>the power franchise</b>  |
| AX-CAP™*   | Global Power Resource™  | Programmable Active Droop™  | TinyBoost™  |
| BitSiC™  | GreenBridge™  | QFET®   | TinyBuck™   |
| Build it Now™  | Green FPS™  | QS™   | TinyCalc™   |
| CorePLUS™  | Green FPS™ e-Series™  | Quiet Series™   | TinyLogic®  |
| CorePOWER™   | Gmax™   | RapidConfigure™   | TINYOPTO™   |
| CROSSVOLT™   | GTO™  |  ™ | TinyPower™  |
| CTL™   | IntelliMAX™   | Saving our world, 1mW/W/kW at a time™   | TinyPWM™  |
| Current Transfer Logic™  | ISOPLANAR™  | SignalWise™   | TinyWire™   |
| DEUXPEED®  | Making Small Speakers Sound Louder and Better™                                    | SmartMax™   | TransiC™  |
| Dual Cool™   | MegaBuck™   | SMART START™  | TriFault Detect™  |
| EcoSPARK®  | MICROCOUPLER™   | Solutions for Your Success™   | TRUECURRENT®*   |
| EfficientMax™  | MicroFET™   | SPM®  | µSerDes™  |
| ESBC™  | MicroPak™   | STEALTH™  |  |
|  Fairchild® | MicroPak2™  | SuperFET®   | UHC®  |
| Fairchild Semiconductor®   | MillerDrive™  | SuperSOT™-3   | Ultra FRFET™  |
| FACT Quiet Series™   | MotionMax™  | SuperSOT™-6   | UniFET™   |
| FACT®  | mWSaver™  | SuperSOT™-8   | VCX™  |
| FAST®  | OptoHi™   | SupreMOS®   | VisualMax™  |
| FastvCore™   | OPTOLOGIC®  | SyncFET™  | VoltagePlus™  |
| FETBench™  | OPTOPLANAR®   | Sync-Lock™  | XS™   |
| FlashWriter®*  |  |    |   |
| FPS™   |   |   |   |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I62