



# AKD4204-A

## AK4204 Evaluation Board Rev.0

### GENERAL DESCRIPTION

The AKD4204-A is an evaluation board for a fast evaluation of the AK4204, Evaluation requires audio/video analog analyzers/generators and a power supply.

■ **Ordering Guide**

AKD4204-A --- AK4204 Evaluation Board

### FUNCTION

- **RCA jacks for analog audio input/output**
- **RCA jacks for video input/output**

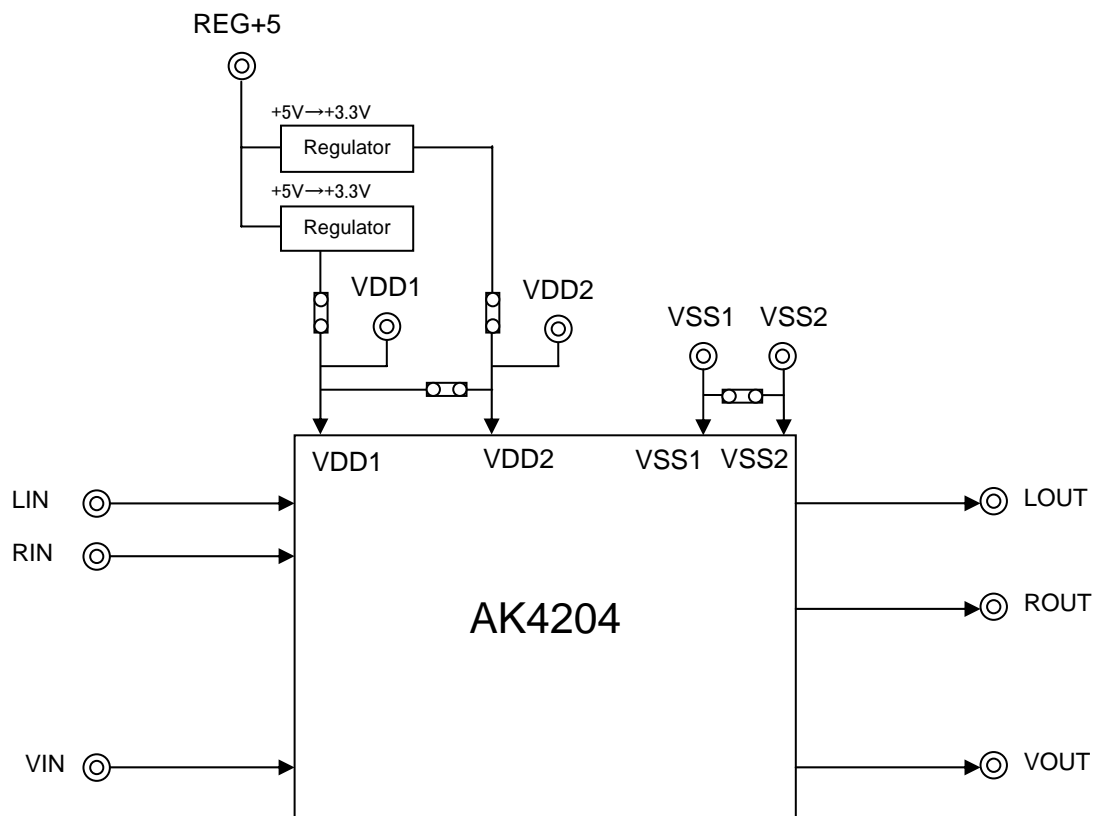


figure 1. AKD4204-A Block Diagram

※Circuit diagram and PCB layout are attached at the end of this manual.

<b>EVALUATION BOARD MANUAL</b>
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## ■ Operation Sequence

### 1) Set up the power supply lines.

Name of Jack	Color of Jack	Voltage	Used for	Comment and attention	Default of Jack
REG+5V	Yellow	+4.8~+5.2V	input Regulator	Connect only when using regulator.	open
VDD1	Red	+3.0~+3.6V	AK4204 VDD1	Should be connected when JP7 (VDD1) is set to REG side. Should be open when JP7(VDD1) is set to VDD1 side.	+3.3V
VDD2	Red	+3.0~+3.6V	AK4204 VDD2	Should be connected when JP4 (VDD2) is set to REG side. Should be open when JP4 (VDD2) is set to VDD2 side.	+3.3V
D3.3V	Red	+3.0 ~3.6 V	Logic Power supply	Should be connected when JP5 (D3.3V) is set to REG side. Should be open when JP5 (D3.3V) is set to D3.3V side.	+3.3V
VSS1	Black	0V	Analog Ground	Should always be connected	0V
VSS2	Black	0V	Analog Ground	Should always be connected	0V

Table 1. Power supply lines

Each supply line should be distributed from the power supply unit.

### 2) Set-up jumper pins. (See the followings.)

### 3) Power on.

## ■ Jumper Pins Set Up

[JP4] (VDD2): Regulator (+3.3V) or VDD2 connector

OPEN: The VDD2 pin is supplied via the VDD2 connector. <Default>

SHORT: The VDD2 pin is supplied via the regulator (+3.3V). (The connector "VDD2" must be open.)

[JP5] (D3.3V): Regulator (+3.3V) or D3.3V connector

OPEN: Logic voltage is supplied via the D3.3V connector. <Default>

SHORT: Logic voltage is supplied via the regulator (+3.3V). (The connector "D3.3V" must be open.)

[JP6] (VDD): VDD1 and VDD2

OPEN: Separated<Default>

SHORT: Connected

[JP7] (VDD1): Regulator (+3.3V) or VDD1 connector

OPEN: The VDD1 pin is supplied via the VDD1 connector. <Default>

SHORT: The VDD1 pin is supplied via the regulator (+3.3V). (The connector "VDD1" must be open.)

The regulator can be supplied 3.3V to all circuits by shorting JP4, JP5 and JP7, and supplying +5V to REG+5V Connector.

### ■ Chip Resistance Set Up

[R15] : SGND pin input select

OPEN: Not to use  
SHORT: SGND<Default>

[R16] : APDN pin input select

OPEN: Not to use  
SHORT: APDN<Default>

[R17] : VSS1 and VSS2

OPEN: Separated<Default>  
SHORT: Connected

### ■ The function of the toggle SW

[S1] (VPDN): Power down of The AK4204 video block. Keep “H” during normal operation.

[S2] (APDN): Power down of The AK4204 audio block. Keep “H” during normal operation.

### ■ Analog Input/Output List

		Signal Name	Note
Audio	Input	J3(LIN), J7(RIN)	Max. 1Vrms
	Output	J4 (LOUT), J6 (ROUT)	Max. 2.1Vrms
Video	Input	J1 (VIN)	Max. 1.5Vpp
	Output	J2 (VOUT)	Min. 2.52Vpp

Table 2. Analog Input/Output List

**MEASUREMENT RESULTS**

■ **Audio**

[Measurement condition]

- Measurement unit : Audio Precision SYS-2722
- BW : 20Hz~20kHz
- Power Supply : REG+5V=+5V, VDD1=VDD2=+3.3V (Regulator)
- Interface : Input: RCA, Output: RCA
- Temperature : Room
- Measurement signal line path: LIN/RIN → LOU/ROU

Parameter	Input signal	Measurement filter	Results LOUT [dB]	Results ROU [dB]
THD+N (At 2Vrms Output)	1kHz, 0dBFS	20kLPF	-95.12	-95.19
DR	1kHz, -60dBFS	22kLPF, A-weighted	103.45	103.41
S/N	“no-input”	22kLPF, A-weighted	103.41	103.53

**Plots**

- Figure 1-1. FFT (1kHz, 0dBFS input) at 2Vrms output
- Figure 1-2. FFT (1kHz, -60dBFS input)
- Figure 1-3. FFT (Noise floor)
- Figure 1-4. THD+N vs. Input Level (fin=1kHz)
- Figure 1-5. THD+N vs. fin (Input Level=0dBFS)
- Figure 1-6. Linearity (fin=1kHz)
- Figure 1-7. Frequency Response (Input Level=0dBFS)
- Figure 1-8. Crosstalk (Input Level=0dBFS)

■ Video

[Measurement condition]

- Signal Generator : Tektronix TG2000
- Measurement unit : Tektronix VM700T
- Power Supply : REG+5V=+5V, VDD1=VDD2=+3.3V (Regulator)
- Interface : Input: RCA, Output: RCA
- Temperature : Room
- Measurement signal line path: S/N: VIN → VOUT  
DG, DP: VIN → VOUT

Parameter	Input Signal	Measurement Filter	Results	Unit
S/N	100% Flat Field	BW=100kHz to 6MHz Filter=Uni-Weighted	82.7	dB
DG	Modulated 5 step		Min: 0.00 Max: 0.16	%
DP	Modulated 5 step		Min: 0.00 Max: 0.73	deg.

Plots

Figure 2-1. DG, DP (Input= Modulated 5 step)

Plots (Audio)

AK4204 LIN/RIN → LOU/ROUT: FFT: fin=1KHz, Input Level=0dB

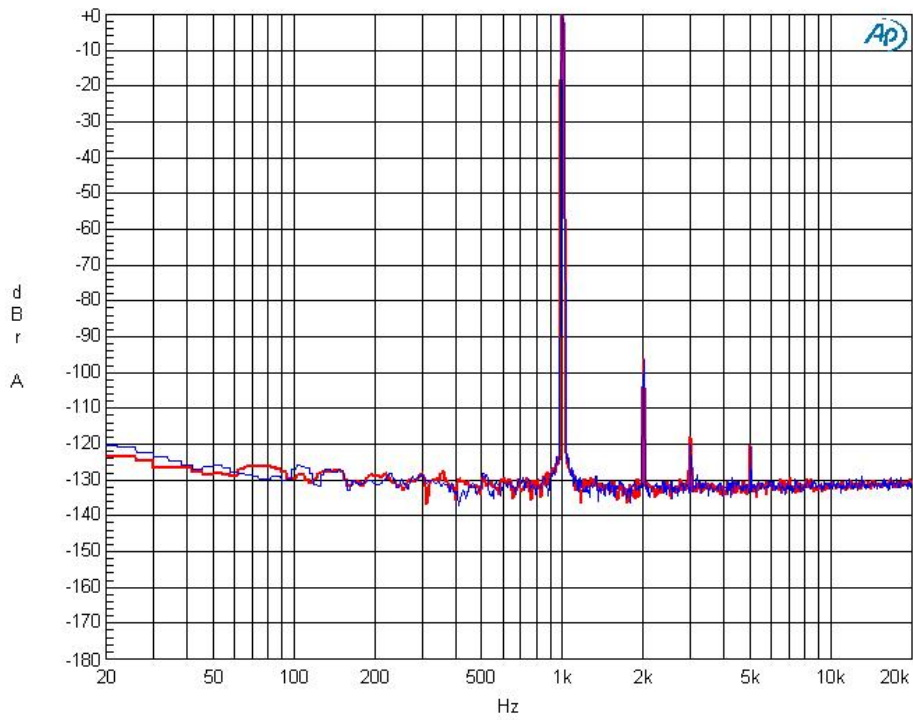


Figure1-1. FFT (fin=1kHz, Input Level=0dB)

AK4204 LIN/RIN → LOU/ROUT: FFT: fin=1KHz, Input Level=-60dB

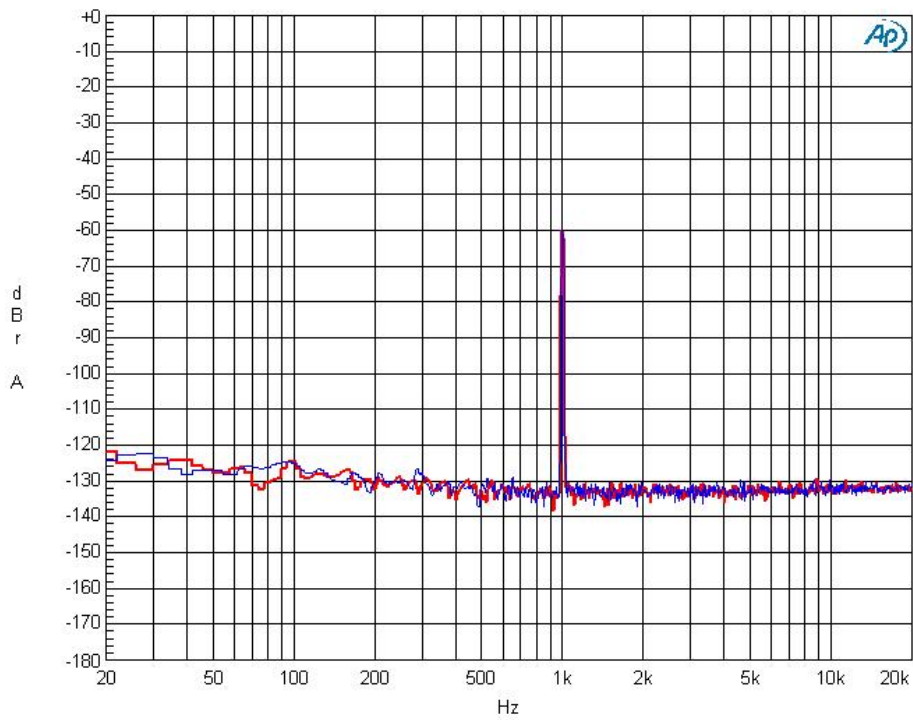


Figure-1-2. FFT (fin=1kHz Input Level=-60dB)

AK4204 LIN/RIN → LOU/ROUT: FFT: No-Input

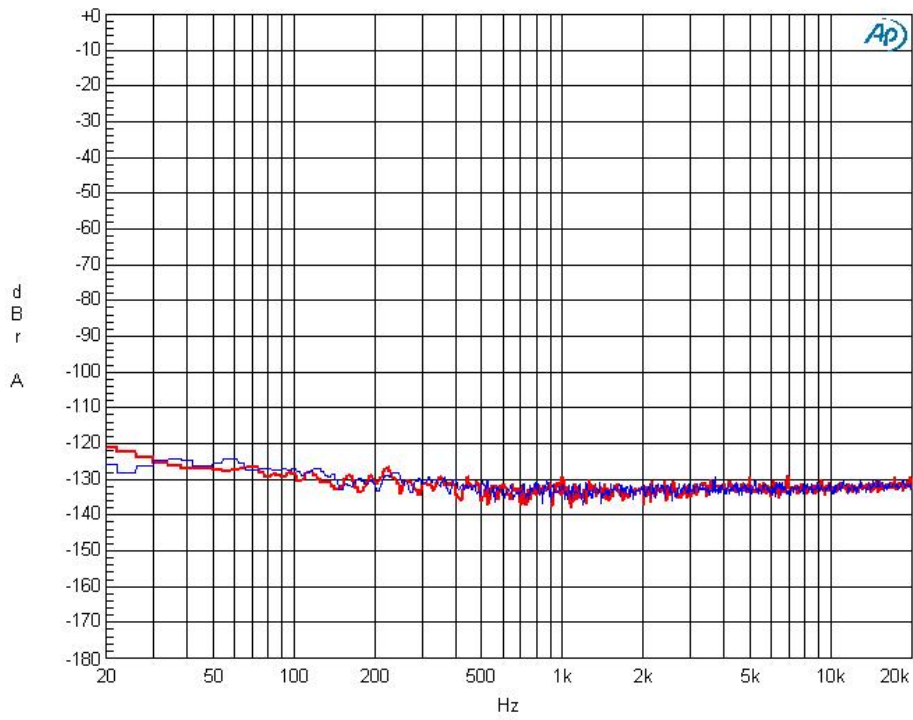


Figure1-3. FFT (Noise Floor)

AK4204 LIN/RIN → LOU/ROUT: THD+N Amplitude vs Input Amplitude: fin=1KHz

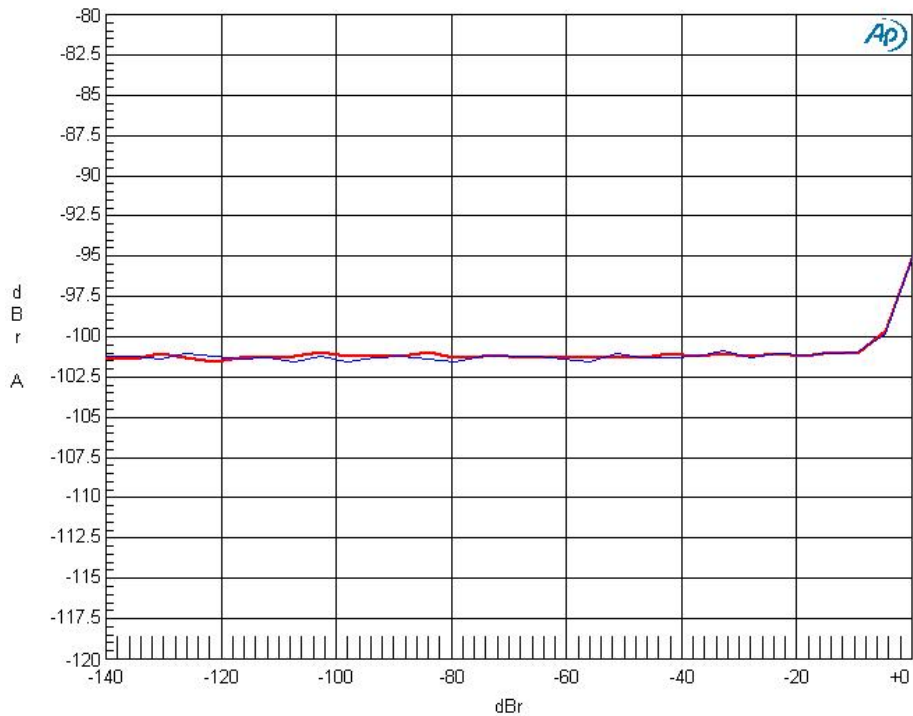


Figure1-4. THD+N vs. Input level (fin=1kHz)

AK4204 LIN/RIN → LOU/ROUT: THD+N Amplitude vs Input Frequency: Input Level=0dB

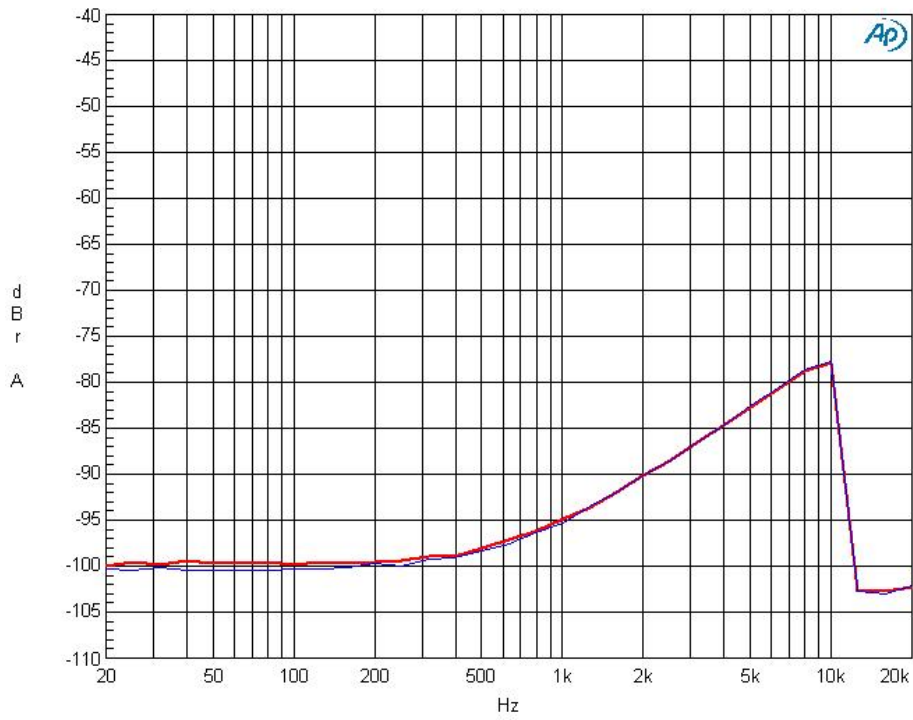


Figure1-5. THD+N vs. Input Frequency (Input level=0dB)

AK4204 LIN/RIN → LOU/ROUT: Linearity: fin=1KHz

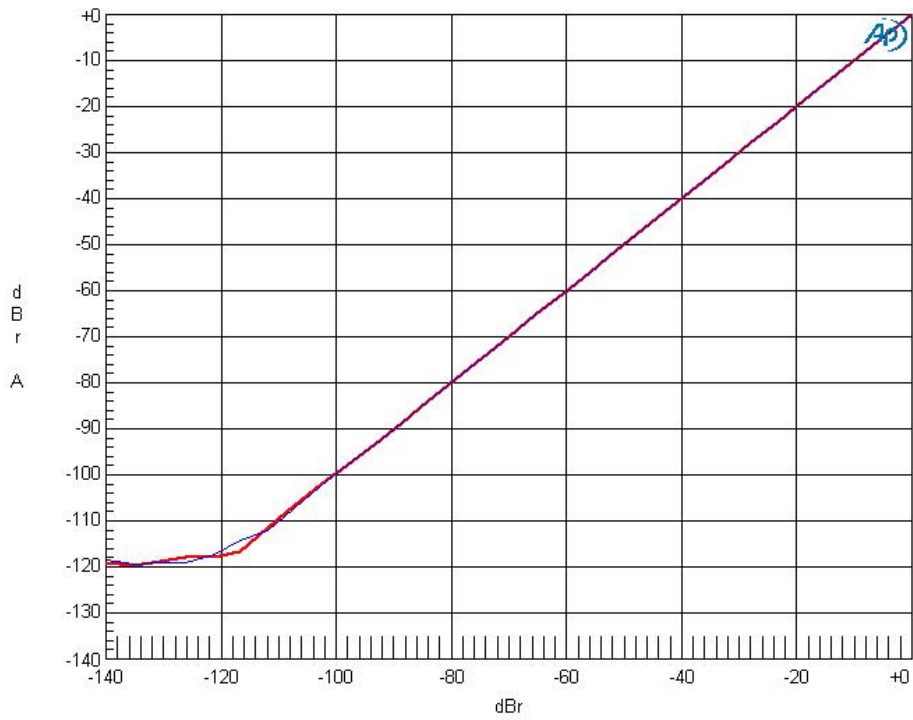


Figure1-6.Linearity (fin=1kHz)



AK4204 LIN/RIN → LOU/ROUT: Frequency Response: Input Level=0dBr

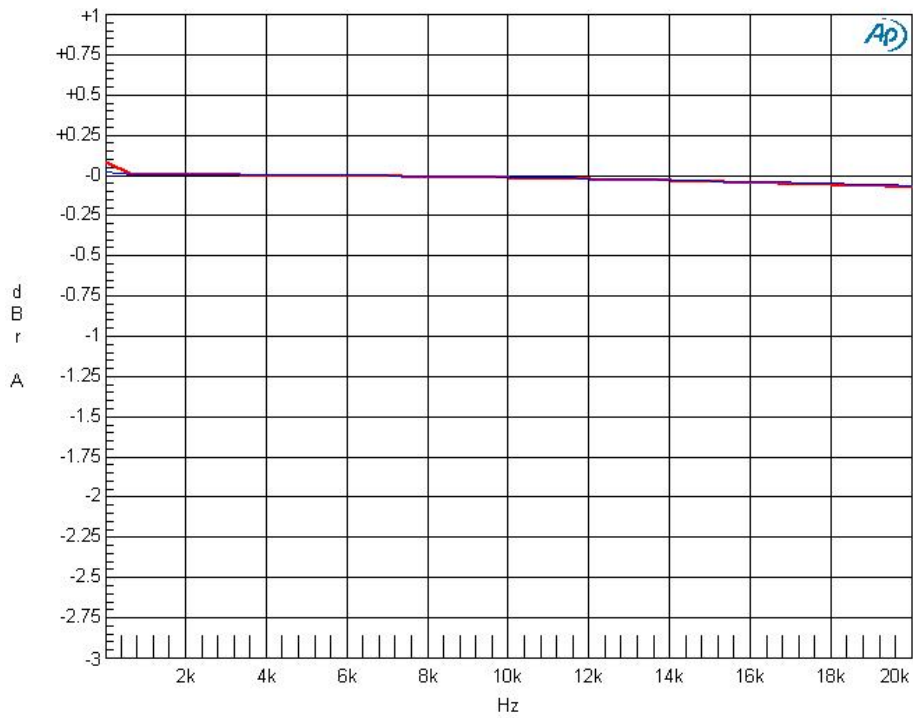


Figure1-7. Frequency Response (Input level=0dB)

AK4204 LIN/RIN → LOU/ROUT: Crosstalk: fin=1KHz, Input Level=0dBr / No-input

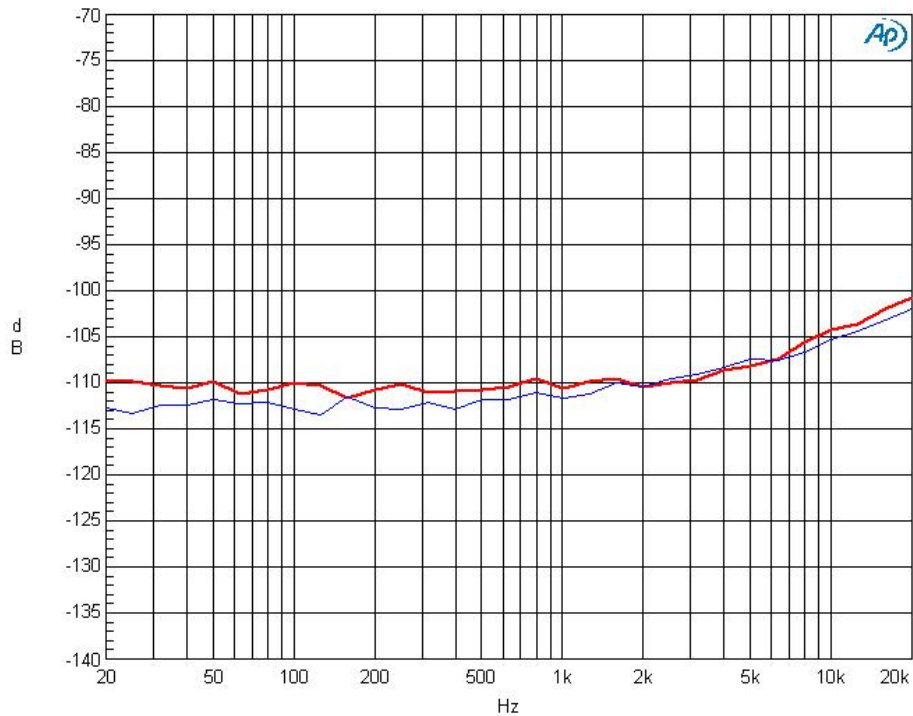


Figure1-8. Crosstalk (Input level=0dB)

Plots(Video)

AK4204 VIN → VOUT: DG, DP: Input Signal=Modulated 5 step

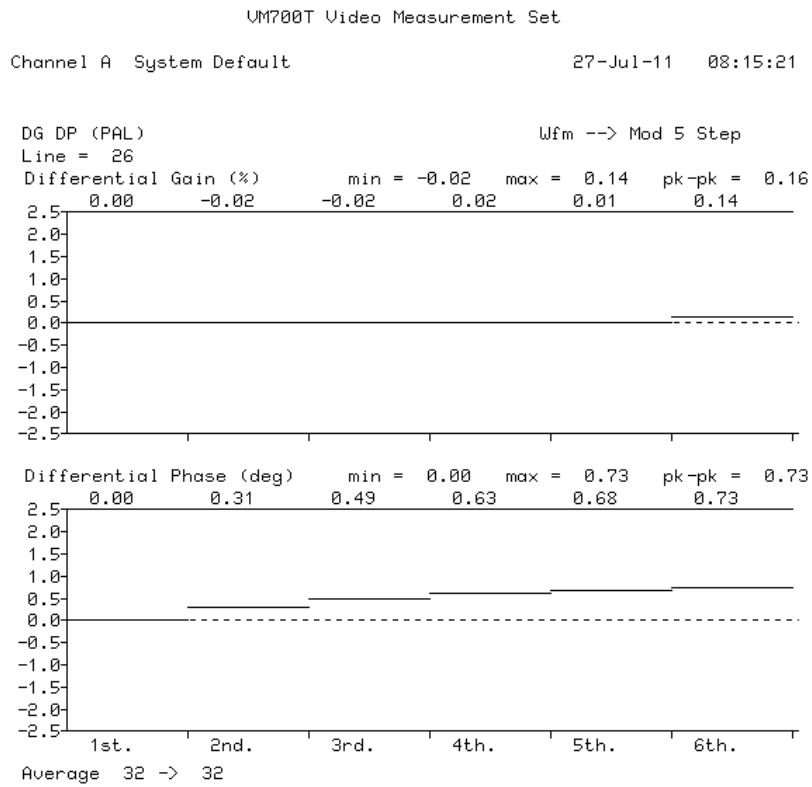


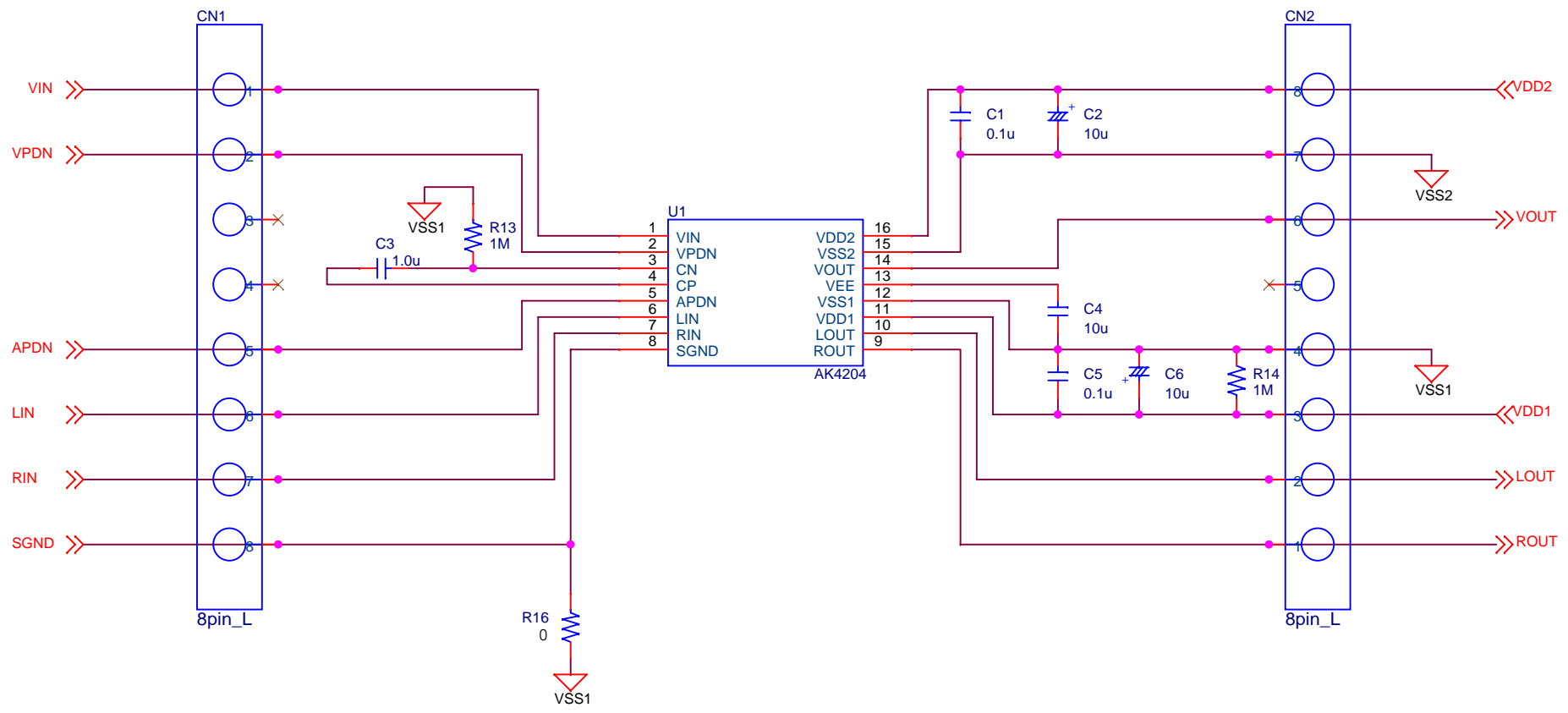
Figure 2-1 DG, DP (Input Signal= Modulated 5 step)

<b>Revision History</b>
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Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
11/08/02	KM108500	0	First Edition		
11/09/06	KM108501	0	Change	5	Measurement Result were changed Video S/N

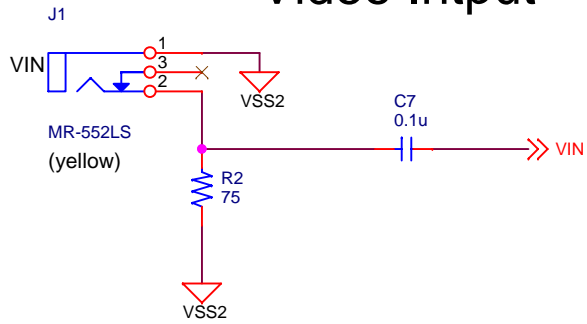
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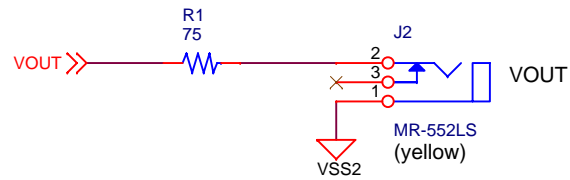


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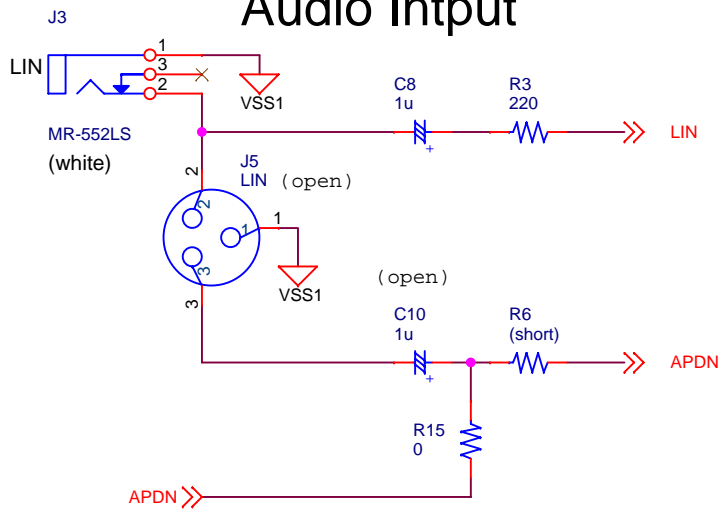
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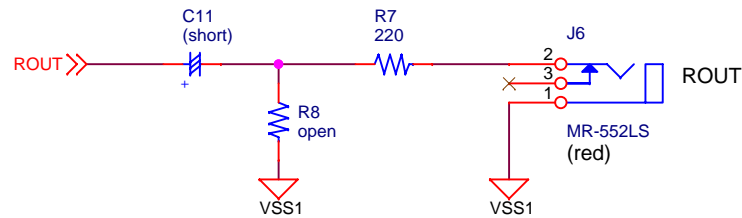
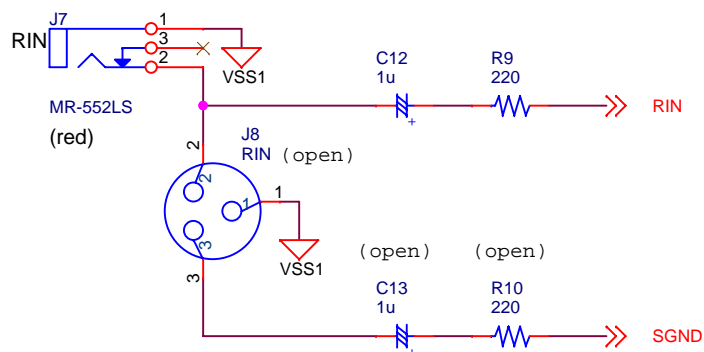
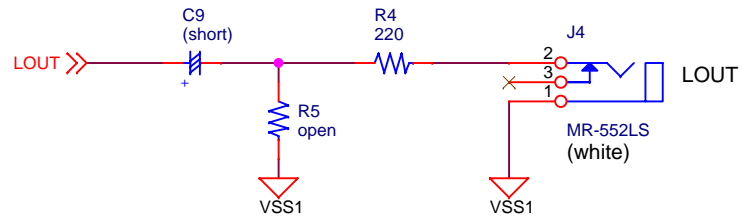
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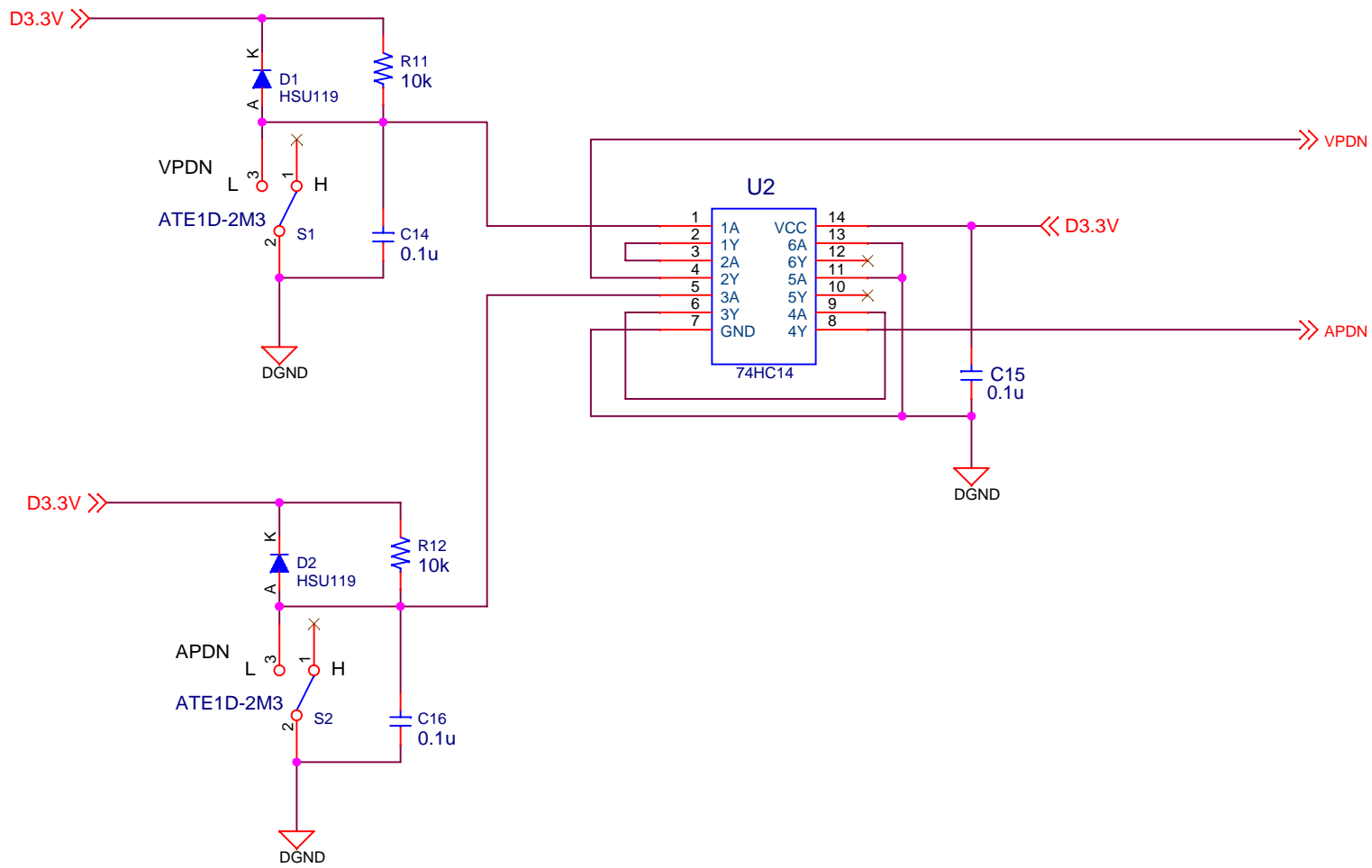
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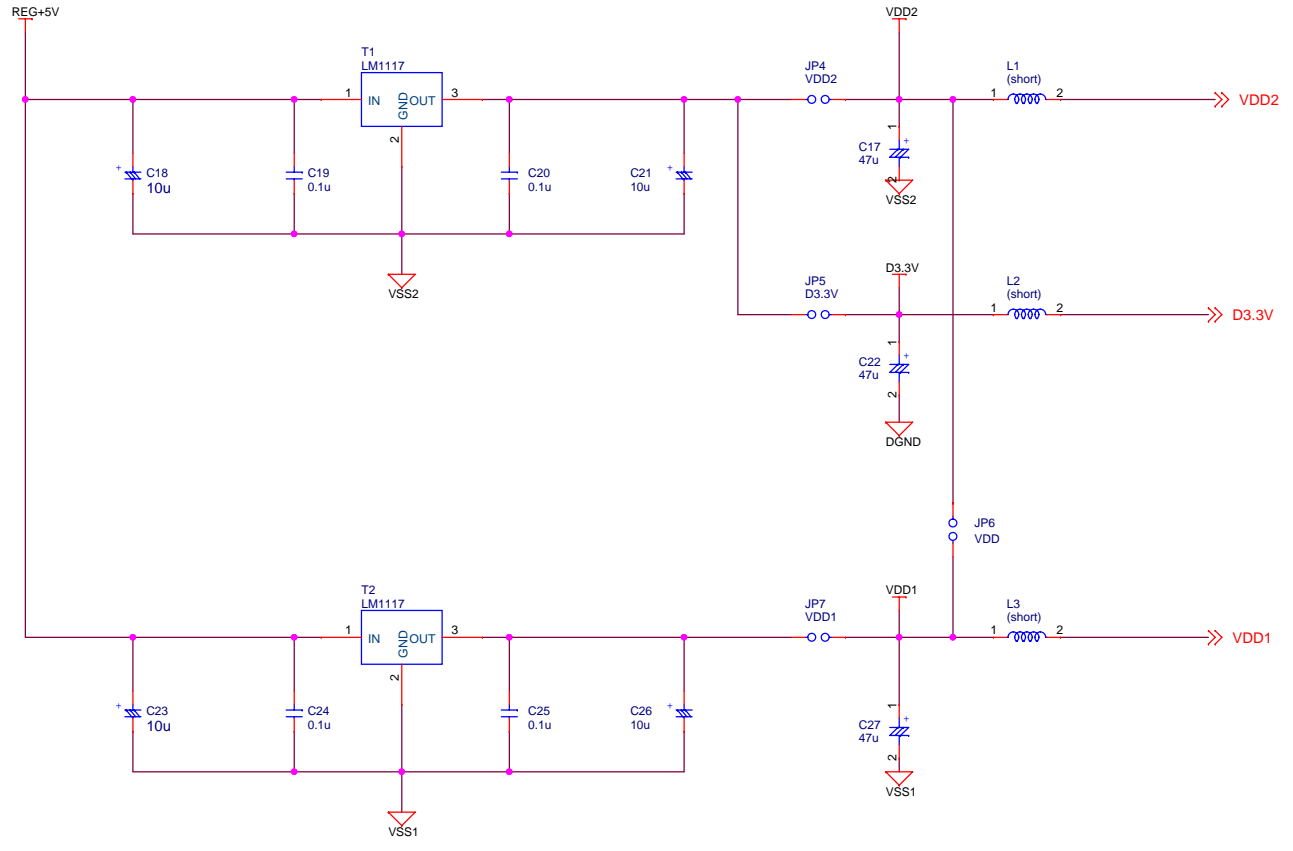
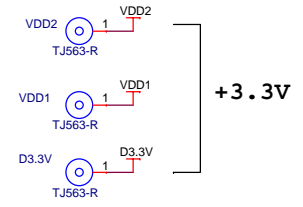
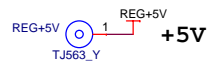
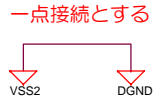
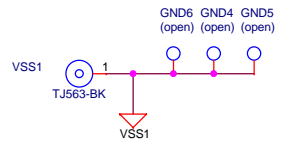
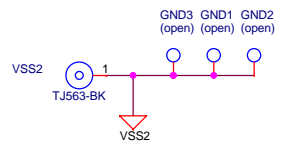
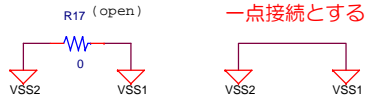
## Audio Output



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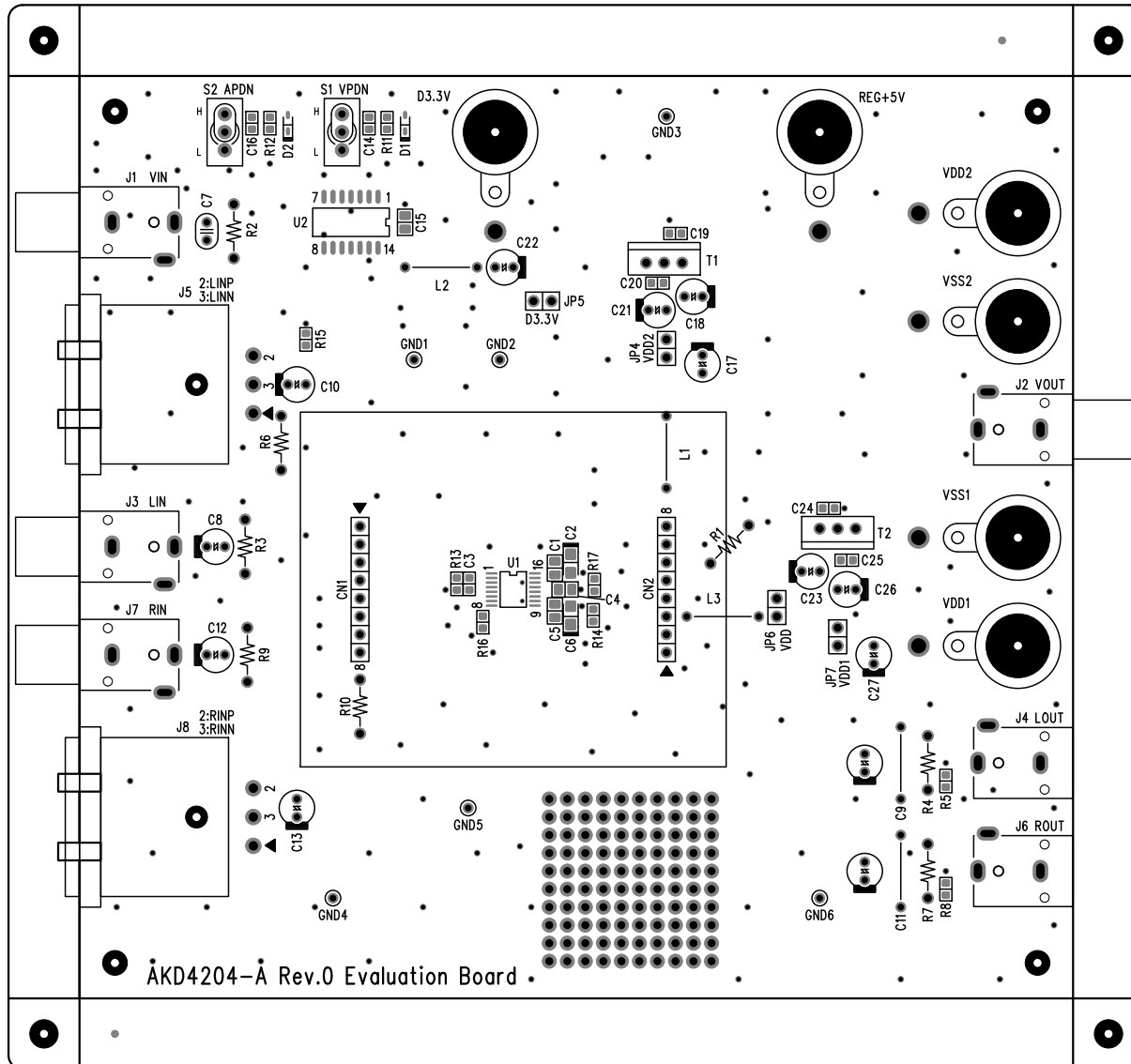


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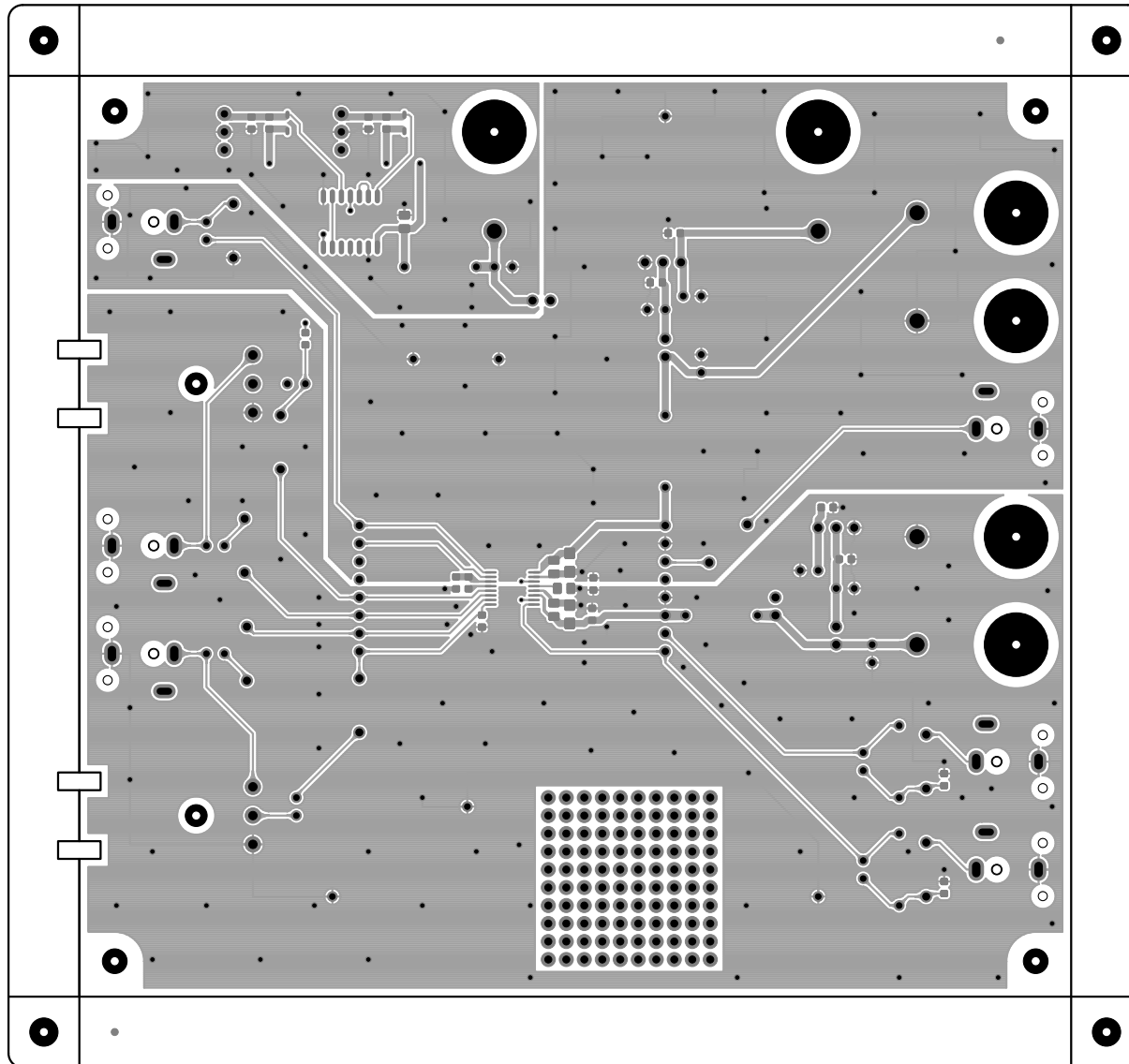




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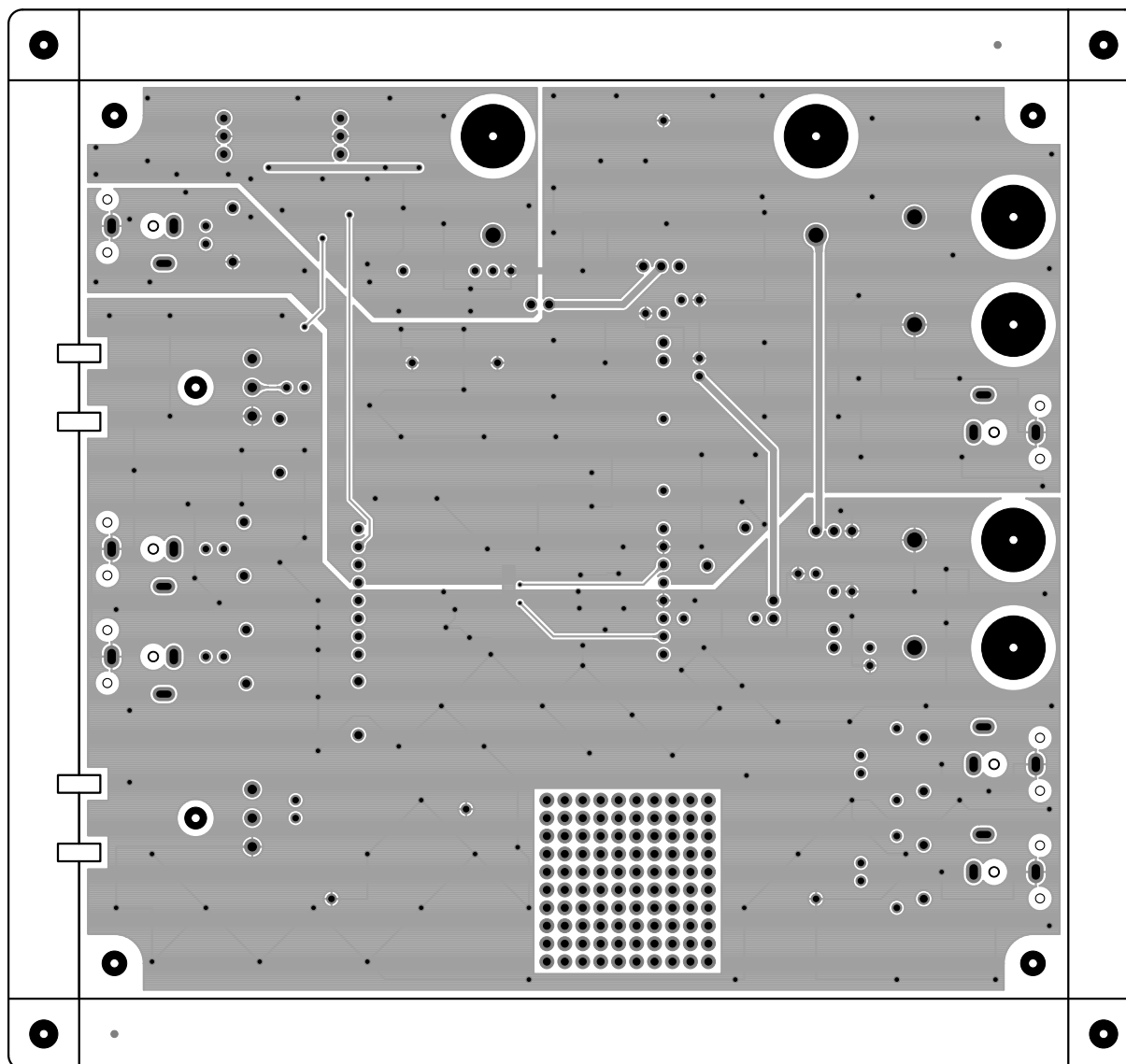
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