

AMIS-30421

Micro-Stepping Stepper Motor Bridge Controller

Introduction

The AMIS-30421 is a micro-stepping stepper motor bridge controller for large current range bipolar applications. The chip interfaces via a SPI interface with an external controller in order to control 2 external power NMOS H-bridges. It has an on-chip voltage regulator, current sensing, self adapting PWM controller and pre-driver with smart slope control switching allowing the part to be EMC compliant with industrial and automotive applications. It uses a proprietary PWM algorithm for reliable current control.

The AMIS-30421 contains a current translation table and takes the next micro-step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (direction) register or input pin. The chip provides a so-called "Speed and Load Angle" output. This allows the creation of stall detection algorithms and control loops based on load angle to adjust torque and speed.

The AMIS-30421 is implemented in a mature technology, enabling fast high voltage analog circuitry and multiple digital functionalities on the same chip. The chip is fully compatible with automotive voltage requirements.

The AMIS-30421 is easy to use and ideally suited for large current stepper motor applications in the automotive, industrial, medical and marine environment. With the on-chip voltage regulator it further reduces the BOM for mechatronic stepper applications.

Key Features

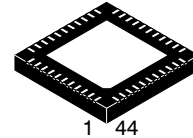
- Dual H-Bridge Pre-Drivers for 2-Phase Stepper Motors
- Programmable Current via SPI
- On-chip Current Translator
- SPI Interface
- Speed and Load Angle Output
- 8 Step Modes from Full Step up to 64 Micro-Steps
- Current-Sense via Two External Sense Resistors
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Low EMC PWM with Selectable Voltage Slopes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Compatible with 3.3 V Microcontrollers
- Integrated 3.3 V Regulator to Supply External Microcontroller
- Integrated Reset Function to Reset External Microcontroller
- These Devices are Pb-Free and are RoHS Compliant*

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



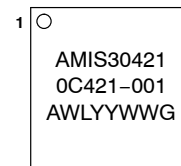
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QFN44
CASE 485BY

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 40 of this data sheet.

AMIS-30421

BLOCK DIAGRAM

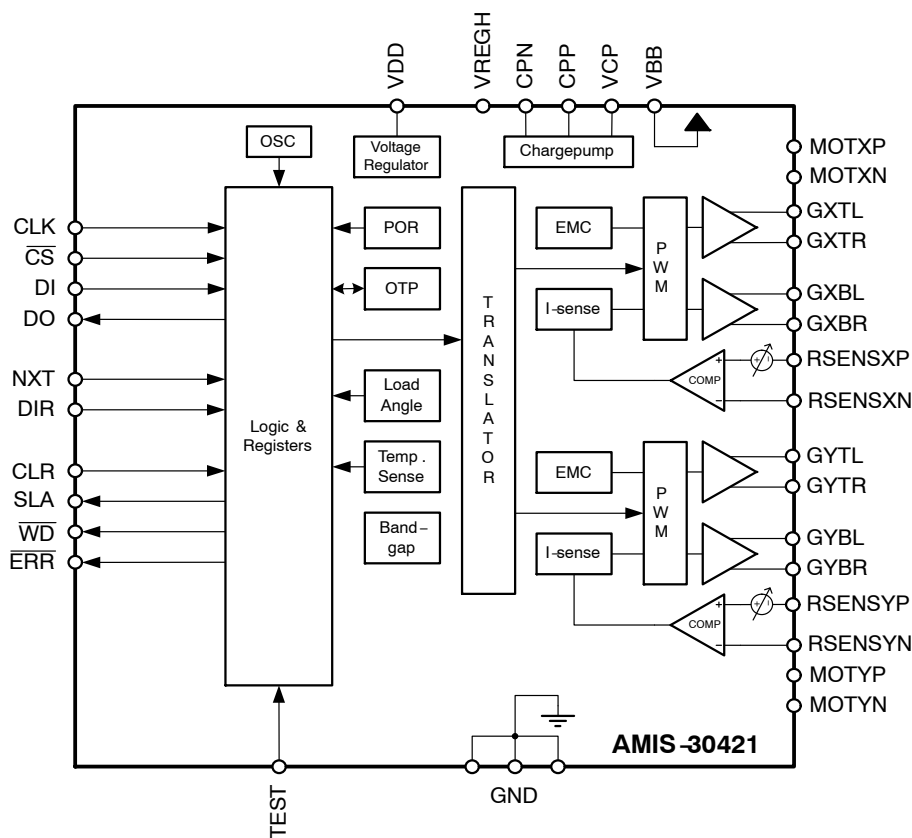


Figure 1. Block Diagram AMIS-30421

PIN OUT

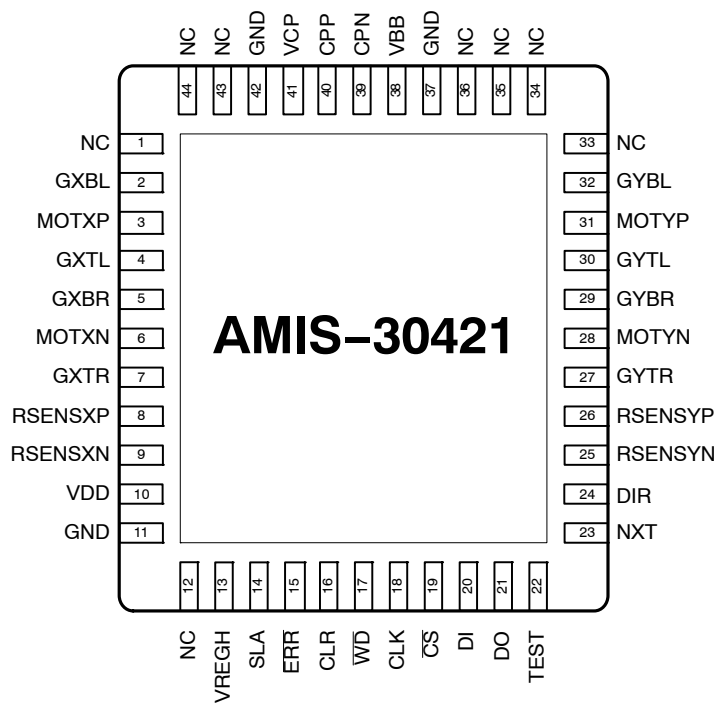


Figure 2. Pin Out AMIS-30421

AMIS-30421

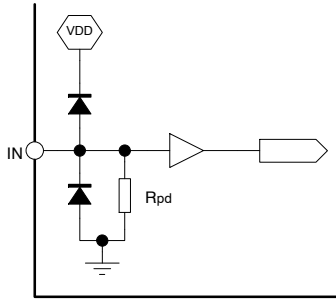
Table 1. PIN LIST AND DESCRIPTION

| Name | Pin | Description | Type | Equivalent Schematic |
|---------|--|---|----------------|----------------------|
| GXBL | 2 | Gate of external NMOS FET of the X bridge bottom left side | Analog Output | |
| MOTXP | 3 | Positive end of phase X-coil | Analog I/O | |
| GXTL | 4 | Gate of external NMOS FET of the X bridge top left side | Analog Output | |
| GXBR | 5 | Gate of external NMOS FET of the X bridge bottom right side | Analog Output | |
| MOTXN | 6 | Negative end of phase X-coil | Analog I/O | |
| GXTR | 7 | Gate of external NMOS FET of the X bridge top right side | Analog Output | |
| RSENSXP | 8 | Resistor sense of the X bridge positive pin | Analog Input | |
| RSENSXN | 9 | Resistor sense of the X bridge negative pin | Analog Input | |
| VDD | 10 | Low voltage supply output (needs external decoupling capacitor) | Supply | Type 7 |
| GND | 11 | Ground, heat sink | Supply | |
| VREGH | 13 | High voltage supply output | Analog output | |
| SLA | 14 | Speed and Load Angle output | Analog output | Type 6 |
| ERRb | 15 | Error output | Digital Output | Type 2 or 4 |
| CLR | 16 | Clear input | Digital Input | Type 1 |
| WDb | 17 | Watchdog and Power On Reset output | Digital Output | Type 2 or 4 |
| CLK | 18 | SPI Clock input | Digital Input | Type 1 |
| CSb | 19 | SPI Chip Select input | Digital Input | Type 3 |
| DI | 20 | SPI Data input | Digital Input | Type 1 |
| DO | 21 | SPI Data output | Digital Output | Type 2 or 4 |
| TEST | 22 | Test input. To be tied to ground. | Digital Input | Type 1 |
| NXT | 23 | Next Microstep input | Digital Input | Type 1 |
| DIR | 24 | Direction input | Digital Input | Type 1 |
| RSENSYN | 25 | Resistor sense of the Y bridge negative pin | Analog Input | |
| RSENSYP | 26 | Resistor sense of the Y bridge positive pin | Analog Input | |
| GYTR | 27 | Gate of external NMOS FET of the Y bridge top right side | Analog Output | |
| MOTYN | 28 | Negative end of phase Y-coil | Analog I/O | |
| GYBR | 29 | Gate of external NMOS FET of the Y bridge bottom right side | Analog Output | |
| GYTL | 30 | Gate of external NMOS FET of the Y bridge top left side | Analog Output | |
| MOTYP | 31 | Positive end of phase Y-coil | Analog I/O | |
| GYBL | 32 | Gate of external NMOS FET of the Y bridge bottom left side | Analog Output | |
| GND | 37 | Ground, heat sink | Supply | |
| VBB | 38 | High voltage supply input | Supply | Type 8 |
| CPN | 39 | Negative connection of charge pump capacitor | Analog I/O | |
| CPP | 40 | Positive connection of charge pump capacitor | Analog I/O | |
| VCP | 41 | Charge Pump filter capacitor | Analog I/O | |
| GND | 42 | Ground, heat sink | Supply | |
| NC | 1, 12, 33, 34, 35, 36, 43, 44 | Not connected or connect with ground | | |

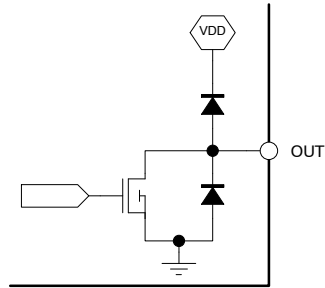
NOTE: Output type of WDb-, ERRb- and DO-pin is selectable through SPI

EQUIVALENT SCHEMATICS

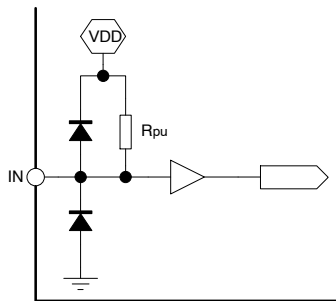
Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.



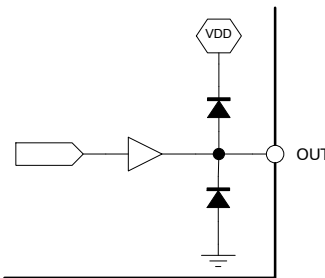
TYPE 1: CLK, DI, NXT, DIR, CLR, TEST Input



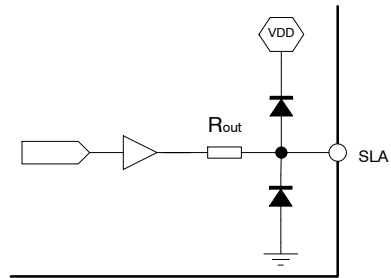
TYPE 2: DO, WDb, ERRb Open Drain Output



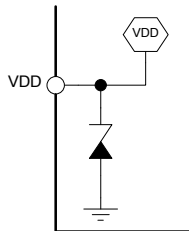
TYPE 3: CSb Input



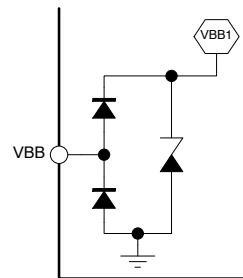
TYPE 4: DO, WDb, ERRb Push Pull Output



TYPE 6: SLA Analog Output



TYPE 7: VDD Power Supply



TYPE 8: VBB Power Supply

NOTE: Output type of WDb-, ERRb- and DO-pin is selectable through SPI

Figure 3. In- and Output Equivalent Diagrams

AMIS-30421

ELECTRICAL SPECIFICATION

Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|------|-----------------------|------|
| V _{BB} | Analog DC supply voltage (Note 3) | -0.3 | +40 | V |
| I _{load} | Logic supply external load current, Normal Mode | 0 | -10 | mA |
| | Logic supply external load current, Sleep Mode | 0 | -1 | mA |
| V _{RSNS} | Voltage on pins RSENSXP, RSENSXN, RSENSYP and RSENYN | -2.0 | +2.0 | V |
| V _{LVI0} | Voltage on digital I/O pins and SLA-pin | -0.3 | 3.6 | V |
| | | | V _{DD} + 0.3 | |
| I _{SLA} | Load current on SLA-pin | 0 | -40 | μA |
| T _{ST} | Storage temperature | -55 | +160 | °C |
| T _J | Junction Temperature under bias (Note 4) | -50 | +175 | °C |
| V _{HBM} | Human Body Model electrostatic discharge immunity (Note 5) | -1.5 | +1.5 | kV |
| V _{HBM} | Human Body Model electrostatic discharge immunity, high voltage pins (Note 6) | -4 | +4 | kV |
| V _{MM} | Machine Model electrostatic discharge immunity (Note 7) | -150 | +150 | V |
| V _{CDM} | Charge Device Model electrostatic discharge immunity (Note 8) | -500 | +500 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. If more than one value is mentioned, the most stringent applies.
2. Convention: currents flowing in the circuit are defined as positive.
3. +36 V < V_{BB} < +40 V limited to 1 day over lifetime
4. Circuit functionality not guaranteed.
5. According to JEDEC JESD22-A114C
6. High Voltage Pins MOTxx, VBB, GND; According to JEDEC JESD22-A114C
7. According to JEDEC EIA-JESD22-A115-A
8. According to STM5.3.1-1999

RECOMMEND OPERATION CONDITIONS

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 3. OPERATING RANGES

| Symbol | Parameter | Min | Max | Unit |
|-----------------|---|------|------|------|
| V _{BB} | Analog DC supply | +6 | +30 | V |
| V _{DD} | Logic Supply Output Voltage (Normal Mode) | +3.0 | +3.6 | V |
| T _J | Junction temperature (Note 9) | -40 | +125 | °C |

9. High junction temperature can result in reduced lifetime.

AMIS-30421

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.
 Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|---------------------------------------|---|-------------------------------------|--|-------|------|----------|----------|
| SUPPLY & VOLTAGE REGULATOR | | | | | | | |
| V_{BB} | VBB | Nominal operating supply range | | 6 | | 30 | V |
| I_{BB} | | Total internal current consumption | Unloaded outputs, I_{INT} included, H-bridge disabled | | | 20 | mA |
| I_{SLEEP} | | Sleep mode current consumption | Unloaded outputs, $CSb = V_{DD}$ | | | 150 | μ A |
| V_{DD} | VDD | Regulated Output Voltage | $-10 \text{ mA} \leq I_{load} \leq 0 \text{ mA}$ | 3.0 | 3.3 | 3.6 | V |
| V_{DD_SLEEP} | | Regulated Output Voltage in Sleep | $-1 \text{ mA} \leq I_{load} \leq 0 \text{ mA}$ | 2.1 | 2.95 | 3.63 | V |
| I_{INT} | | Internal load current | Unloaded outputs | | | 8 | mA |
| I_{LOAD} | | External load current | | | | -10 | mA |
| I_{DDLIM} | | Current limitation | Pin shorted to ground | -20 | | -80 | mA |
| I_{LOAD_PD} | | Output current in sleep | | | | -1 | mA |
| V_{REGH} | VREGH | High voltage regulator | $V_{BBLV} \leq V_{BB} \leq 30 \text{ V}$ Based on Figure 9 H-bridge disabled $13.25 \text{ V} \leq V_{BBLV} \leq 15.75 \text{ V}$ | 8.0 | 9.5 | 11.5 | V |
| | | | $6 \text{ V} \leq V_{BB} < V_{BBLV}$ Based on Figure 9 H-bridge disabled $13.25 \text{ V} \leq V_{BBLV} \leq 15.75 \text{ V}$ | | | V_{BB} | V |
| POWER ON RESET (POR) | | | | | | | |
| V_{DDH} | VDD | Internal POR comparator threshold | V_{DD} rising, see Figure 4 | 1.44 | 1.8 | 2.53 | V |
| V_{DDL} | | Internal POR comparator threshold | V_{DD} falling, see Figure 4 | 1.16 | 1.5 | 1.93 | |
| V_{DDhys} | | Internal POR comparator hysteresis | | | 0.3 | | |
| UNDERVOLTAGE | | | | | | | |
| V_{BBUH} | VBB | V_{BB} undervoltage release level | V_{BB} rising, see Figure 5 | 5.5 | | 6.5 | V |
| V_{BBUL} | | V_{BB} undervoltage trigger level | V_{BB} falling, see Figure 5 | 5.3 | | 6.3 | |
| V_{BBUhys} | | V_{BB} undervoltage hysteresis | | | 0.25 | | |
| OVERVOLTAGE | | | | | | | |
| V_{BBOH} | VBB | V_{BB} overvoltage trigger level | V_{BB} rising, see Figure 5 | 30.0 | | 32.0 | V |
| V_{BBOL} | | V_{BB} overvoltage release level | V_{BB} falling, see Figure 5 | 29.0 | | 31 | |
| V_{BBOhys} | | V_{BB} overvoltage hysteresis | | | 1 | | |
| PRE-DRIVER | | | | | | | |
| I_{ON} | GXTR, GXTL, GXBR, GXBL, GYTR, GYTL, GYBR, GYBL | Gate charge current | Selectable through SPI | -1.25 | | -33.00 | mA |
| I_{ON_tol} | | Gate charge current tolerance | | -45 | | +45 | % |
| I_{OFF} | | Gate discharge current | Selectable through SPI | -10.5 | | -115.5 | mA |
| I_{OFF_tol} | | Gate discharge current tolerance | | -45 | | +45 | % |
| R_{SW} | | Switch On-resistance | See also Figure 10 | 5 | 10 | 25 | Ω |

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.
Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|-------------------|----------|-------------------------------|------------------------|-------|-----|-------|------|
| PRE-DRIVER | | | | | | | |
| V_{SENS0} | RSSENSxx | PWM comparator toggle level 0 | | 78 | 100 | 122 | mV |
| V_{SENS1} | | PWM comparator toggle level 1 | | 105.3 | 135 | 164.7 | mV |
| V_{SENS2} | | PWM comparator toggle level 2 | | 156 | 200 | 244 | mV |
| V_{SENS3} | | PWM comparator toggle level 3 | | 210.6 | 270 | 391.4 | mV |
| V_{SENS4} | | PWM comparator toggle level 4 | | 261.3 | 335 | 408.7 | mV |
| V_{SENS5} | | PWM comparator toggle level 5 | | 312 | 400 | 488 | mV |
| V_{SENS6} | | PWM comparator toggle level 6 | | 390 | 500 | 610 | mV |
| V_{SENS7} | | PWM comparator toggle level 7 | | 468 | 600 | 732 | mV |

DIGITAL INPUTS

| | | | | | | | |
|----------|--------------------------------------|-----------------------------|------------------------------------|---------------------|----|---------------------|------------|
| V_{IL} | CLK, DI, CSb, NXT, DIR, CLR | Logic Low Threshold | | 0 | | $0.3 \times V_{DD}$ | V |
| V_{IH} | | Logic High Threshold | | $0.7 \times V_{DD}$ | | V_{DD} | V |
| R_{pd} | | Internal Pull Down Resistor | CSb excluded, See also Figure 3 | 25 | 50 | 75 | k Ω |
| R_{pu} | CSb | Internal Pull Up Resistor | See also Figure 3 | 25 | 50 | 75 | k Ω |

DIGITAL OUTPUTS

| | | | | | | | |
|----------------|---------------------|----------------------------|--|----------------|--|-----|---|
| V_{OL} | DO, ERRb, WDb | Logic low output level | Output set to type 4 (see Figure 3) | | | 0.5 | V |
| V_{OH} | | Logic high output level | | $V_{DD} - 0.5$ | | | |
| V_{OL_OPEN} | | Logic Low level open drain | $I_{OL} = 8 \text{ mA}$, Output set to type 2 (see Figure 3) | | | 0.5 | |

SPEED AND LOAD ANGLE OUTPUT

| | | | | | | | |
|-----------------|-----|--|------------------------|--------|--|----------------|---------------|
| V_{out} | SLA | Output Voltage Range | | 0.5 | | $V_{DD} - 0.5$ | V |
| V_{off} | | Output Offset SLA-pin | Selectable through SPI | 0.6 | | 1.2 | V |
| V_{off_tol} | | Tolerance on SLA output offset | | -17 | | +17 | % |
| G_{SLA} | | Gain of SLA-pin = V_{BEMF} / V_{SLA} | Selectable through SPI | 0.0625 | | 1 | |
| G_{SLA_tol} | | Tolerance on SLA gain | | -10 | | +10 | % |
| R_{out} | | Output Resistance SLA-pin | See also Figure 3 | | | 1 | k Ω |
| I_{SLA_load} | | Load current SLA-pin | | 0 | | -40 | μA |

THERMAL WARNING & SHUTDOWN

| | | | | | | | |
|-----------|--|-------------------------------|---------------|-----|---------------|-----|--------------------|
| T_1 | | Trigger level thermal range 1 | See Figure 22 | -5 | 15 | 35 | $^{\circ}\text{C}$ |
| T_2 | | Trigger level thermal range 2 | See Figure 22 | 55 | 70 | 85 | $^{\circ}\text{C}$ |
| T_3 | | Trigger level thermal range 3 | See Figure 22 | 138 | 150 | 162 | $^{\circ}\text{C}$ |
| T_{TW} | | Thermal Warning | See Figure 22 | 138 | 150 | 162 | $^{\circ}\text{C}$ |
| T_{TSD} | | Thermal shutdown | See Figure 22 | | $T_{TW} + 20$ | | $^{\circ}\text{C}$ |

CHARGE PUMP

| | | | | | | | |
|---------------------|---------|------------------------------|-------------------------|-----|----------------|-------|----|
| $V_{CP} - V_{BB}$ | VCP | Chargepump overdrive voltage | Based on Figure 9 | 3.5 | $V_{BB} - 2.5$ | 15.75 | V |
| $V_{CPP} - V_{CPN}$ | | Chargepump pumping voltage | | 3.5 | $V_{BB} - 2.5$ | 15.75 | V |
| C_{pump} | | External pump capacitor | See also C_2 Figure 9 | | 220 | | nF |
| C_{buffer} | CPP CPN | External buffer capacitor | See also C_3 Figure 9 | | 220 | | nF |

AMIS-30421

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.
Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|---|--------|---|--|-----|------|-----|------|
| PACKAGE THERMAL RESISTANCE VALUE | | | | | | | |
| R_{thja} | | Thermal Resistance Junction-to-Ambient | Simulated Conform JEDEC JESD-51, (2S2P) | | 30 | | K/W |
| | | | Simulated Conform JEDEC JESD-51, (1S0P) | | 60 | | K/W |
| R_{thjp} | | Thermal Resistance Junction-to-Exposed Pad | | | 0.95 | | K/W |

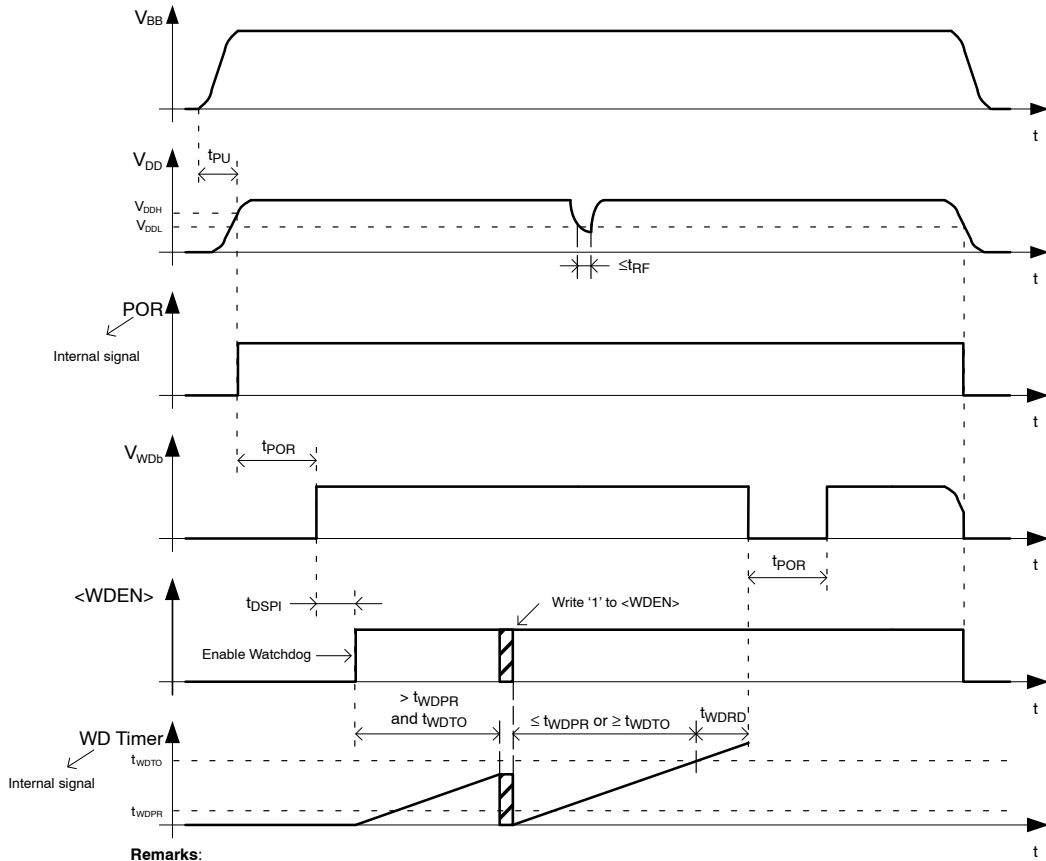
Table 5. AC PARAMETER The AC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|----------------------------|--------|---------------------------------------|--|------|-----|--------|---------------|
| INTERNAL OSCILLATOR | | | | | | | |
| f_{osc} | | Frequency of internal oscillator | | 6.4 | 8 | 9.6 | MHz |
| POWER-UP | | | | | | | |
| t_{PU} | POR | Power-up time | $C_{VDD} = 200 \text{ nF}$, See Figure 4 | | | 60 | μs |
| t_{POR} | | Reset duration | See Figure 4 | 80 | 100 | 120 | ms |
| t_{RF} | | Reset filter time | See Figure 4 | 1 | | 15 | μs |
| t_{DSPI} | | SPI Delay | See Figure 4 | | | 500 | μs |
| PREDRIVER | | | | | | | |
| f_{PWM} | | PWM frequency | Frequency depends only on internal oscillator | 20 | 25 | 30 | kHz |
| t_1 | | Bridge MOSFET switch on time t_1 | Selectable through SPI. See Figure 11. | 375 | | 1250 | ns |
| t_2 | | Bridge MOSFET switch on time t_2 | Selectable through SPI. See Figure 11. | 1250 | | 4750 | ns |
| t_{off} | | Bridge MOSFET switch off time | Selectable through SPI. See Figure 11. | 1250 | | 4750 | ns |
| t_{switch_tol} | | Bridge MOSFET switch on/off tolerance | | -20 | | +20 | % |
| t_{open} | | Open circuit time out | Selectable through SPI | 0.32 | | 163.84 | ms |
| t_{open_acc} | | Open circuit time out accuracy | | -20 | | +20 | % |
| $t_{nocross}$ | | Non overlap time | Selectable through SPI | 0 | | 1 | μs |
| $t_{nocross_acc}$ | | Non overlap accuracy | | -20 | | +20 | % |

AMIS-30421

Table 5. AC PARAMETER The AC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|--|---------------|---|--|-----|-----|---------|---------|
| DIGITAL INPUTS | | | | | | | |
| t_{NXT_HI} | | NXT Minimum, high pulse width | See Figure 6 | 625 | | | ns |
| t_{NXT_LO} | | NXT Minimum, low pulse width | | 625 | | | ns |
| t_{DIR_SET} | | NXT set up time, following change of DIR or <DIRCTRL> | | 1 | | | μ s |
| t_{DIR_HOLD} | | NXT hold time, before change of DIR or <DIRCTRL> | | 1 | | | μ s |
| t_{SLP_SET} | | <SLP> set up time | | 300 | | | μ s |
| t_{SLP_HOLD} | | <SLP> hold time | | 1 | | | μ s |
| t_{MOTEN_SET} | | <MOTEN> set up time | | 1 | | | μ s |
| t_{MOTEN_HOLD} | | <MOTEN> hold time | | 1 | | | μ s |
| t_{MSP} | | <MSP[7:0]> update delay | | | 1 | μ s | |
| CLEAR FUNCTION | | | | | | | |
| t_{CLR_SET} | CLR | Clear set up time | See Figure 7 | 40 | | | μ s |
| t_{CLR} | | Clear duration time | See Figure 7 | 20 | | 90 | μ s |
| DIGITAL OUTPUTS | | | | | | | |
| t_{H2L} | DO, WDb, ERRb | Output fall-time from V_{OH} to V_{OL} | Output type 2, capacitive load 400 pF and pull-up resistor of 1.5 k Ω | | | 50 | ns |
| WATCHDOG | | | | | | | |
| t_{WDPR} | | Prohibited watchdog acknowledge time | | | | 2.5 | ms |
| t_{WDTO} | | Watchdog time out interval | | 32 | | 512 | ms |
| t_{WDTO_acc} | | Watchdog time out accuracy | | -20 | | +20 | % |
| t_{WDRD} | | Watchdog Reset Delay | | | | 500 | ns |
| SERIAL PERIPHERAL INTERFACE (SPI) | | | | | | | |
| t_{CLK} | CLK | SPI Clock period | See Figure 8 | 1 | | | μ s |
| t_{CLK_HIGH} | | SPI Clock high time | | 100 | | | ns |
| t_{CLK_LOW} | | SPI Clock low time | | 100 | | | ns |
| t_{DI_SET} | DI | SPI Data Input set up time | | 50 | | | ns |
| t_{DI_HOLD} | | SPI Data Input hold time | | 50 | | | ns |
| t_{CS_HIGH} | CSb | SPI Chip Select high time | | 2.5 | | | μ s |
| t_{CS_SET} | | SPI Chip Select set up time | | 100 | | | ns |
| t_{CS_HOLD} | | SPI Chip Select hold time | | 100 | | | ns |
| SPEED AND LOAD ANGLE OUTPUT | | | | | | | |
| t_{SLA_DELAY} | SLA | SLA output update delay | Not-transparent Mode See Figure 20 | | | 60 | μ s |
| t_{MinSLA} | | Minimum zero crossing time | Selectable through SPI | 40 | | 360 | μ s |
| t_{MinSLA_Acc} | | Minimum zero crossing accuracy | | -20 | | +20 | % |
| CHARGE PUMP | | | | | | | |
| f_{CP} | CPN CPP | Charge pump frequency | | 160 | 200 | 250 | kHz |
| t_{CPU} | MOTxx | Start-up time of charge pump | Spec external components in Table 4 | | 250 | | μ s |



Remarks:
 -WDb-pin pulled up to V_{DD}
 - $t_{WDTO} = \langle WDT[3:0] \rangle$
 - $\langle WDEN \rangle$ and $\langle WDT[3:0] \rangle$ are SPI bits

Figure 4. Power-On-Reset Timing Diagram

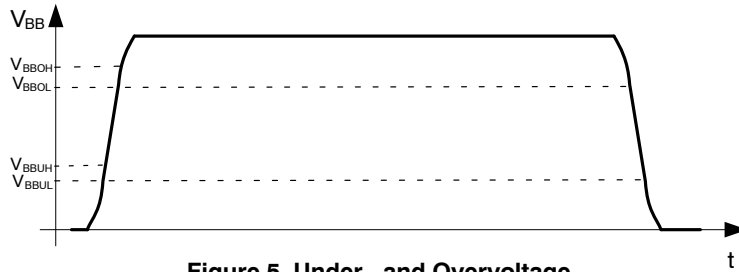
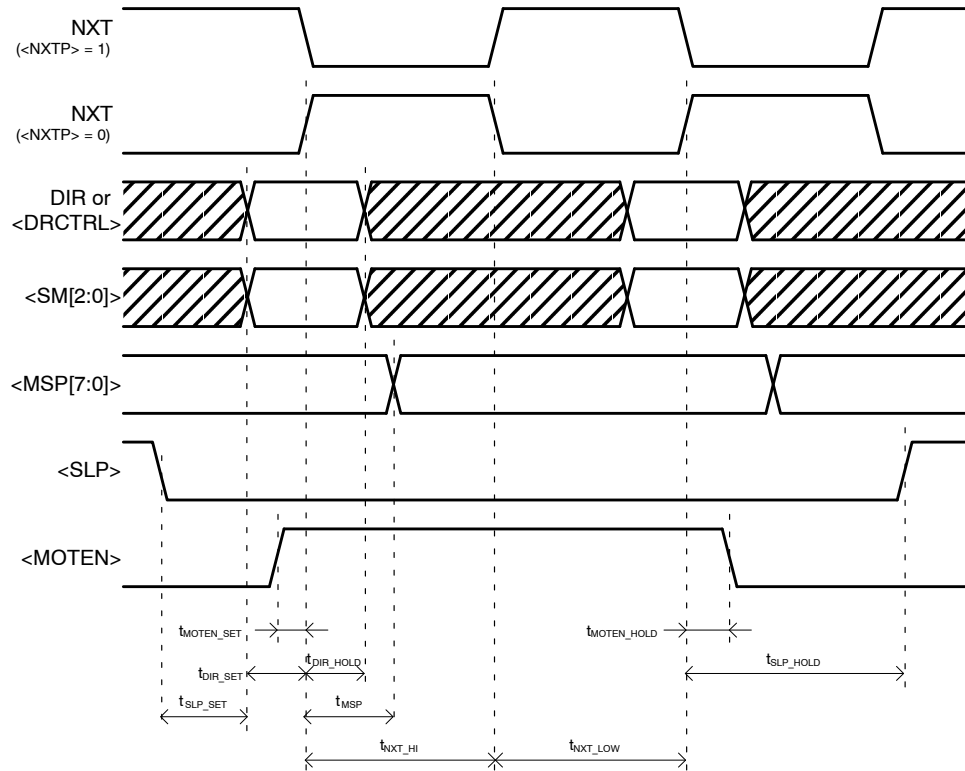


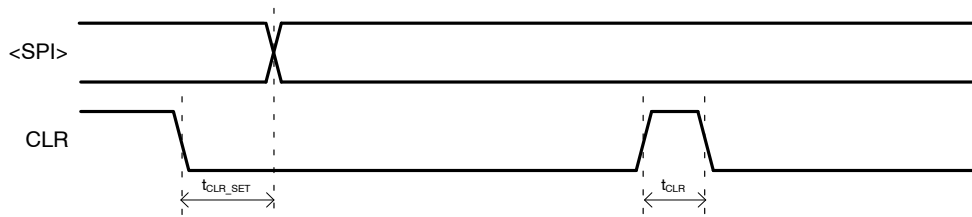
Figure 5. Under- and Overvoltage

AMIS-30421



Remarks:
 -<DIRCTRL>, <SM[2:0]>, <MSP[7:0]>, <SLP>, <MOTEN> and <NXTP> are SPI bits
 -Timing for SPI bits starts after CS is high
 -t_SLP_SET only relates to the digital inputs pins DIR and NXT

Figure 6. Digital Input Timing Diagram



Remarks:
 <SPI> is any SPI data

Figure 7. CLR-pin Timing Diagram

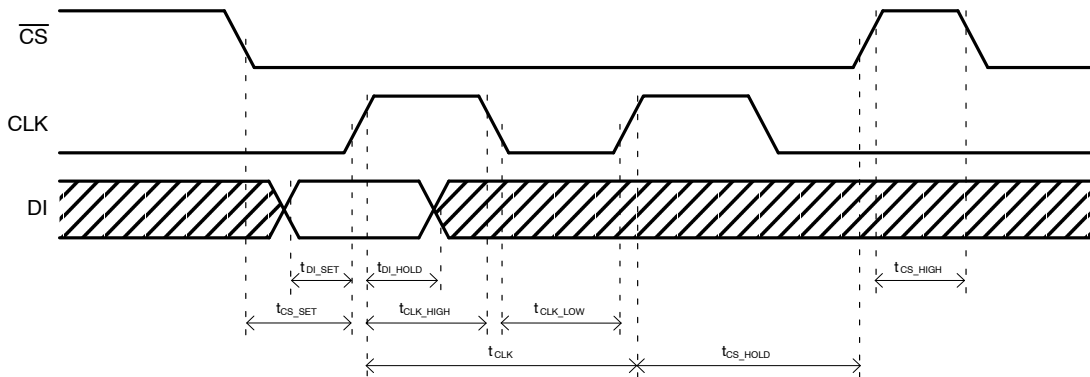


Figure 8. SPI Bus Timing Diagram

AMIS-30421

TYPICAL APPLICATION SCHEMATIC

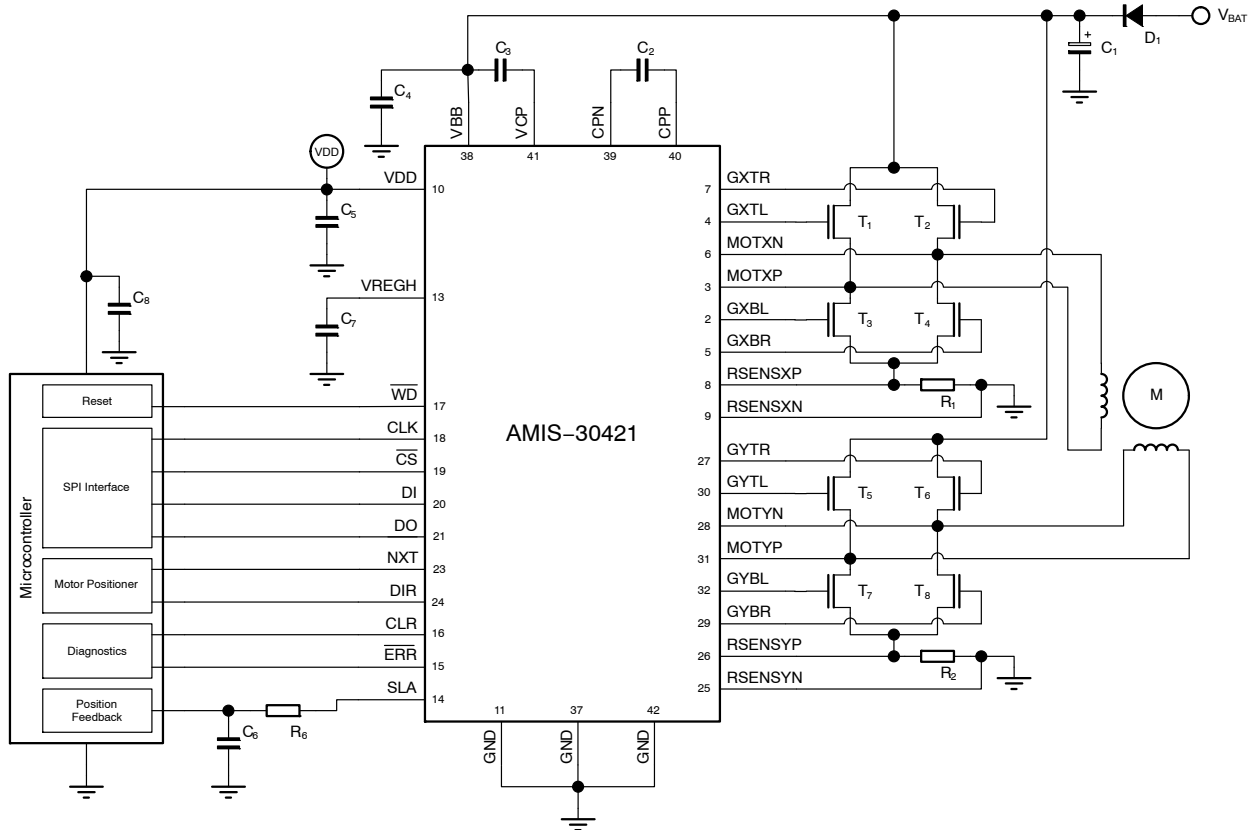


Figure 9. Typical Application Schematic AMIS-30421

Table 6. EXTERNAL COMPONENTS LIST AND DESCRIPTION

| Component | Function | Typ Value | Tolerance | Unit |
|-----------------------------------|---|--|-----------|------|
| C ₁ | V _{BB} buffer capacitor (Note 1) | 100 | ±20% | μF |
| C ₂ | Charge-pump pumping capacitor | 220 | ± 20% | nF |
| C ₃ | Charge-pump buffer capacitor | 220 | ±20% | nF |
| C ₄ | V _{BB} decoupling capacitor (Note 2) | 100 | ±20% | nF |
| C ₅ , C ₈ | V _{DD} buffer capacitor | 100 | ±20 % | nF |
| C ₆ | Low pass filter SLA | 1 | ±20% | nF |
| C ₇ | VREGH buffer capacitor | 4.7 | ±20% | uF |
| R ₁ , R ₂ | Sense Resistors | >25 | ±1% | mΩ |
| R ₆ | Low pass filter SLA | 5.6 | ±1% | kΩ |
| D ₁ | Optional reverse protection diode | MBRD1045 | | |
| T ₁ ... T ₈ | H-Bridge N-MOSFET | NTD4815N or NTD4813N or NTD40N03R or NTD5807N | | |

10. ESR < 1 Ω.

11. ESR < 50 mΩ.

FUNCTIONAL DESCRIPTION

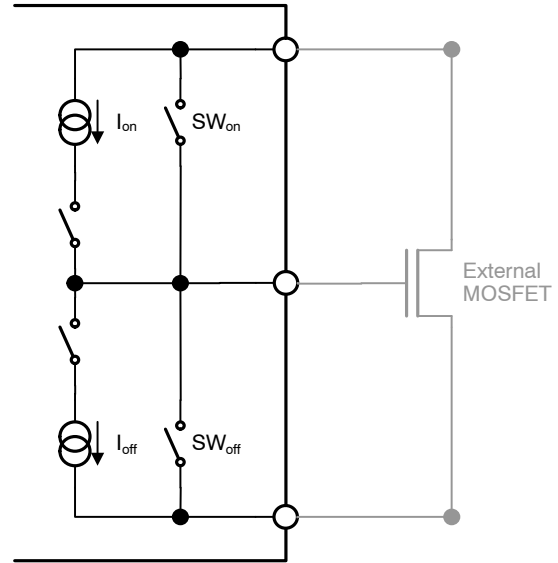
H-Bridge Pre-Drivers

The H-bridge pre-drivers for external N-type MOSFETs are controlled by means of current sources for slope regulation (Figure 10). The current source value can be set through SPI (see p35 and further). During the MOSFET switch-on and switch-off phase this current source will be applied for a certain time (respectively t_{on} and t_{off} where t_{on} is divided in t_1 and t_2). After this time (t_{on} or t_{off}) the gate of the MOSFET is pulled high or low by means of a switch (SW_{on} or SW_{off}). The timings can also be set through SPI (see p37 and further).

To prevent short circuits, an additional time $t_{nocross}$ can be added between switching off one MOSFET and switching on the other MOSFET of a half H-bridge (SPI bits $\langle NO_CROSS[1:0] \rangle$).

More information on the current sources and timings can be found in Table 5. A detailed description of the SPI settings for the H-bridge pre-drivers can be found at p31 and further.

Figure 11 gives a detailed view on the different stages during switching of the MOSFET.



AMIS-30421

Figure 10. Pre-driver Topology

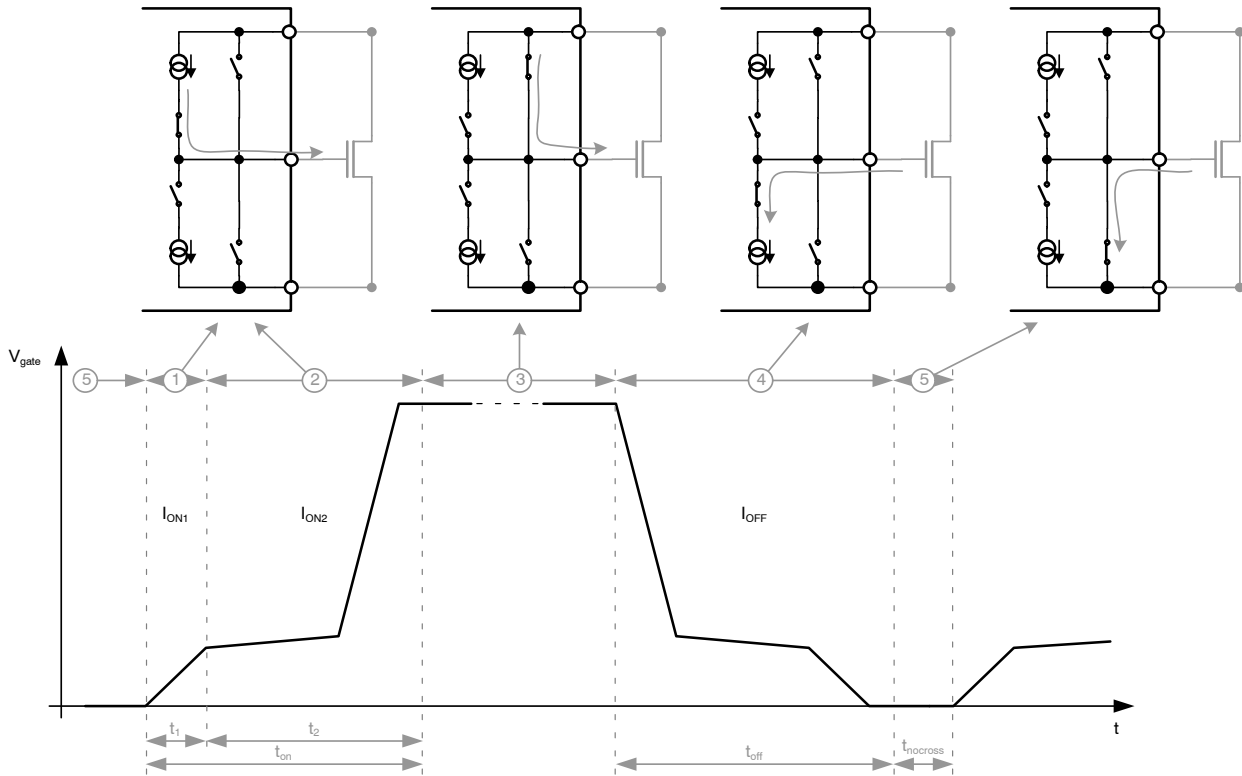


Figure 11. Detailed View on MOSFET Switching

PWM Current Control

A PWM comparator compares continuously the actual winding current (measured over the external sense resistor) with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the current sources (I_{on} , I_{off}) and switches (SW_{on} , SW_{off}). The switching points of the PWM duty-cycle are synchronized to the on-chip PWM clock. The frequency of the PWM controller is fixed and will not vary with changes in the supply voltage. Also variations in motor-speed or load-conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

For EMC reasons it's possible to add jitter to the PWM by means of the <PWMJ> bit.

Step Translator and Step Mode

The step translator provides the control of the motor by means of the stepmode SPI bits <SM[2:0]>, the enable SPI bit <MOTEN>, the direction SPI bit <DIRCTRL> and input

pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode. One out of 8 possible stepping modes can be selected through SPI bits <SM[2:0]>.

After power-up or clear (CLR-pin) the coil current translator is set to position 0. For all stepping modes except full step this means that the coil current is maximum in the Y-coil and zero in the X-coil (see Table 7). If NXT pulses are applied when the DIR-pin is pulled low, SPI bit <DIRCTRL> is zero and SPI bit <MOTEN> is one, the coil current translator will step through Table 7 from top till bottom. If DIR-pin is pulled high or SPI bit <DIRCTRL> is set to '1', the coil current translator will step in opposite direction through the table.

Figures 12 up to 15 gives another view on the different stepping modes. The Y-coil current is plotted on the Y-axes, the X-coil current on the X-axes. Notice that all stepping modes from Table 7 can be plotted on a circle with the exception of half step uncompensated and full step. These are plotted on a square.

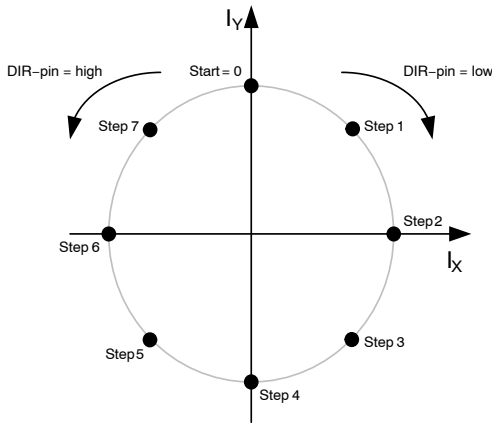


Figure 12. Circular representation Half-step Compensated

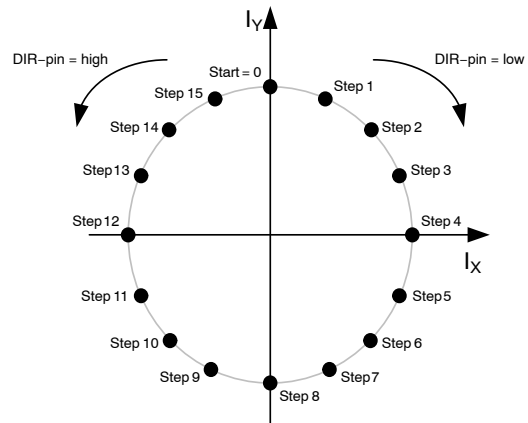


Figure 13. Circular representation 1/4 Microstepping

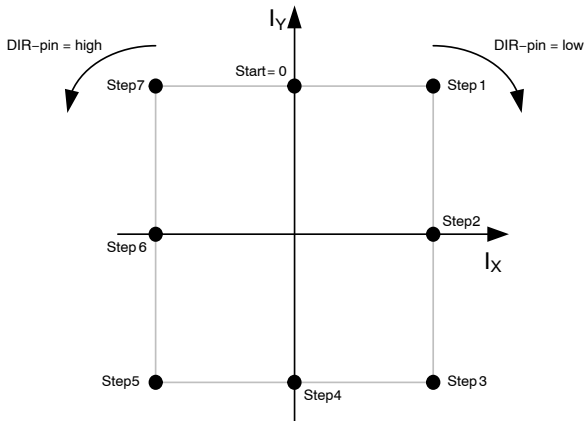


Figure 14. Square Representation Half-step Uncompensated

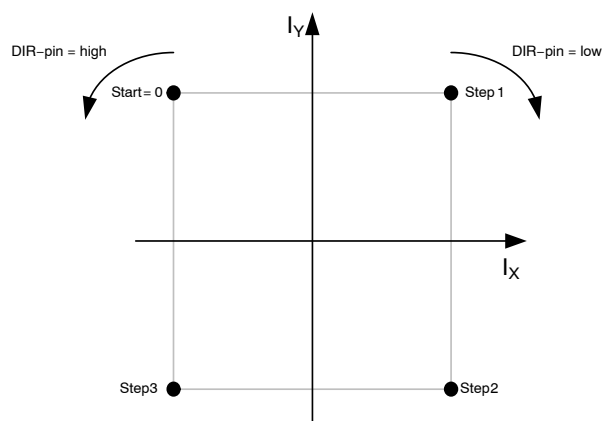


Figure 15. Square Representation Full-step

Remark:

- ◆ Positive coil current flows from MOTXP to MOTXN and MOTYP to MOTYN.
- ◆ In above figures SPI bit <DIRCTRL> is set to '0'. When set to '1', rotation will be reversed.

Table 7. CIRCULAR TRANSLATOR TABLE

| Stepmode (<SM[2:0]>) | | | | | | | | % of I _{max} | |
|------------------------|------|------|-----|-----|----------|------------|------|-----------------------|----------|
| 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | Coil x | Coil y |
| 1/64 | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 comp | 1/2 uncomp | Full | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | 0 | 100 |
| 1 | - | - | - | - | - | - | - | 3 | 100 |
| 2 | 1 | - | - | - | - | - | - | 5 | 100 |
| 3 | - | - | - | - | - | - | - | 8 | 100 |
| 4 | 2 | 1 | - | - | - | - | - | 10 | 100 |
| 5 | - | - | - | - | - | - | - | 13 | 100 |
| 6 | 3 | - | - | - | - | - | - | 14 | 100 |
| 7 | - | - | - | - | - | - | - | 17 | 98 |
| 8 | 4 | 2 | 1 | - | - | - | - | 19 | 98 |
| 9 | - | - | - | - | - | - | - | 22 | 98 |
| 10 | 5 | - | - | - | - | - | - | 25 | 97 |
| 11 | - | - | - | - | - | - | - | 27 | 97 |
| 12 | 6 | 3 | - | - | - | - | - | 30 | 97 |
| 13 | - | - | - | - | - | - | - | 32 | 95 |
| 14 | 7 | - | - | - | - | - | - | 35 | 95 |
| 15 | - | - | - | - | - | - | - | 37 | 94 |
| 16 | 8 | 4 | 2 | 1 | - | - | - | 38 | 94 |
| 17 | - | - | - | - | - | - | - | 41 | 92 |
| 18 | 9 | - | - | - | - | - | - | 43 | 90 |
| 19 | - | - | - | - | - | - | - | 46 | 90 |
| 20 | 10 | 5 | - | - | - | - | - | 48 | 89 |
| 21 | - | - | - | - | - | - | - | 51 | 87 |
| 22 | 11 | - | - | - | - | - | - | 52 | 87 |
| 23 | - | - | - | - | - | - | - | 54 | 86 |
| 24 | 12 | 6 | 3 | - | - | - | - | 56 | 84 |
| 25 | - | - | - | - | - | - | - | 59 | 83 |
| 26 | 13 | - | - | - | - | - | - | 60 | 81 |
| 27 | - | - | - | - | - | - | - | 62 | 79 |
| 28 | 14 | 7 | - | - | - | - | - | 63 | 78 |
| 29 | - | - | - | - | - | - | - | 67 | 76 |
| 30 | 15 | - | - | - | - | - | - | 68 | 75 |
| 31 | - | - | - | - | - | - | - | 70 | 73 |
| 32 | 16 | 8 | 4 | 2 | 1 | 1 | 1 | 71 / 100 | 71 / 100 |
| 33 | - | - | - | - | - | - | - | 73 | 70 |
| 34 | 17 | - | - | - | - | - | - | 75 | 68 |
| 35 | - | - | - | - | - | - | - | 76 | 67 |
| 36 | 18 | 9 | - | - | - | - | - | 78 | 63 |
| 37 | - | - | - | - | - | - | - | 79 | 62 |
| 38 | 19 | - | - | - | - | - | - | 81 | 60 |
| 39 | - | - | - | - | - | - | - | 83 | 59 |
| 40 | 20 | 10 | 5 | - | - | - | - | 84 | 56 |
| 41 | - | - | - | - | - | - | - | 86 | 54 |
| 42 | 21 | - | - | - | - | - | - | 87 | 52 |
| 43 | - | - | - | - | - | - | - | 87 | 51 |
| 44 | 22 | 11 | - | - | - | - | - | 89 | 48 |
| 45 | - | - | - | - | - | - | - | 90 | 46 |
| 46 | 23 | - | - | - | - | - | - | 90 | 43 |
| 47 | - | - | - | - | - | - | - | 92 | 41 |
| 48 | 24 | 12 | 6 | 3 | - | - | - | 94 | 38 |
| 49 | - | - | - | - | - | - | - | 94 | 37 |
| 50 | 25 | - | - | - | - | - | - | 95 | 35 |
| 51 | - | - | - | - | - | - | - | 95 | 32 |
| 52 | 26 | 13 | - | - | - | - | - | 97 | 30 |
| 53 | - | - | - | - | - | - | - | 97 | 27 |
| 54 | 27 | - | - | - | - | - | - | 97 | 25 |
| 55 | - | - | - | - | - | - | - | 98 | 22 |
| 56 | 28 | 14 | 7 | - | - | - | - | 98 | 19 |
| 57 | - | - | - | - | - | - | - | 98 | 17 |
| 58 | 29 | - | - | - | - | - | - | 100 | 14 |
| 59 | - | - | - | - | - | - | - | 100 | 13 |
| 60 | 30 | 15 | - | - | - | - | - | 100 | 10 |
| 61 | - | - | - | - | - | - | - | 100 | 8 |
| 62 | 31 | - | - | - | - | - | - | 100 | 5 |
| 63 | - | - | - | - | - | - | - | 100 | 3 |

Table 7. CIRCULAR TRANSLATOR TABLE

| Stepmode (<SM[2:0]>) | | | | | | | | % of I _{max} | |
|------------------------|------|------|-----|-----|----------|------------|------|-----------------------|------------|
| 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | Coil x | Coil y |
| 1/64 | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 comp | 1/2 uncomp | Full | | |
| 64 | 32 | 16 | 8 | 4 | 2 | 2 | - | 100 | 0 |
| 65 | - | - | - | - | - | - | - | 100 | -3 |
| 66 | 33 | - | - | - | - | - | - | 100 | -5 |
| 67 | - | - | - | - | - | - | - | 100 | -8 |
| 68 | 34 | 17 | - | - | - | - | - | 100 | -10 |
| 69 | - | - | - | - | - | - | - | 100 | -13 |
| 70 | 35 | - | - | - | - | - | - | 100 | -14 |
| 71 | - | - | - | - | - | - | - | 98 | -17 |
| 72 | 36 | 18 | 9 | - | - | - | - | 98 | -19 |
| 73 | - | - | - | - | - | - | - | 98 | -22 |
| 74 | 37 | - | - | - | - | - | - | 97 | -25 |
| 75 | - | - | - | - | - | - | - | 97 | -27 |
| 76 | 38 | 19 | - | - | - | - | - | 97 | -30 |
| 77 | - | - | - | - | - | - | - | 95 | -32 |
| 78 | 39 | - | - | - | - | - | - | 95 | -35 |
| 79 | - | - | - | - | - | - | - | 94 | -37 |
| 80 | 40 | 20 | 10 | 5 | - | - | - | 94 | -38 |
| 81 | - | - | - | - | - | - | - | 92 | -41 |
| 82 | 41 | - | - | - | - | - | - | 90 | -43 |
| 83 | - | - | - | - | - | - | - | 90 | -46 |
| 84 | 42 | 21 | - | - | - | - | - | 89 | -48 |
| 85 | - | - | - | - | - | - | - | 87 | -51 |
| 86 | 43 | - | - | - | - | - | - | 87 | -52 |
| 87 | - | - | - | - | - | - | - | 86 | -54 |
| 88 | 44 | 22 | 11 | - | - | - | - | 84 | -56 |
| 89 | - | - | - | - | - | - | - | 83 | -59 |
| 90 | 45 | - | - | - | - | - | - | 81 | -60 |
| 91 | - | - | - | - | - | - | - | 79 | -62 |
| 92 | 46 | 23 | - | - | - | - | - | 78 | -63 |
| 93 | - | - | - | - | - | - | - | 76 | -67 |
| 94 | 47 | - | - | - | - | - | - | 75 | -68 |
| 95 | - | - | - | - | - | - | - | 73 | -70 |
| 96 | 48 | 24 | 12 | 6 | 3 | 3 | 2 | 71 / 100 | -71 / -100 |
| 97 | - | - | - | - | - | - | - | 70 | -73 |
| 98 | 49 | - | - | - | - | - | - | 68 | -75 |
| 99 | - | - | - | - | - | - | - | 67 | -76 |
| 100 | 50 | 25 | - | - | - | - | - | 63 | -78 |
| 101 | - | - | - | - | - | - | - | 62 | -79 |
| 102 | 51 | - | - | - | - | - | - | 60 | -81 |
| 103 | - | - | - | - | - | - | - | 59 | -83 |
| 104 | 52 | 26 | 13 | - | - | - | - | 56 | -84 |
| 105 | - | - | - | - | - | - | - | 54 | -86 |
| 106 | 53 | - | - | - | - | - | - | 52 | -87 |
| 107 | - | - | - | - | - | - | - | 51 | -87 |
| 108 | 54 | 27 | - | - | - | - | - | 48 | -89 |
| 109 | - | - | - | - | - | - | - | 46 | -90 |
| 110 | 55 | - | - | - | - | - | - | 43 | -90 |
| 111 | - | - | - | - | - | - | - | 41 | -92 |
| 112 | 56 | 28 | 14 | 7 | - | - | - | 38 | -94 |
| 113 | - | - | - | - | - | - | - | 37 | -94 |
| 114 | 57 | - | - | - | - | - | - | 35 | -95 |
| 115 | - | - | - | - | - | - | - | 32 | -95 |
| 116 | 58 | 29 | - | - | - | - | - | 30 | -97 |
| 117 | - | - | - | - | - | - | - | 27 | -97 |
| 118 | 59 | - | - | - | - | - | - | 25 | -97 |
| 119 | - | - | - | - | - | - | - | 22 | -98 |
| 120 | 60 | 30 | 15 | - | - | - | - | 19 | -98 |
| 121 | - | - | - | - | - | - | - | 17 | -98 |
| 122 | 61 | - | - | - | - | - | - | 14 | -100 |
| 123 | - | - | - | - | - | - | - | 13 | -100 |
| 124 | 62 | 31 | - | - | - | - | - | 10 | -100 |
| 125 | - | - | - | - | - | - | - | 8 | -100 |
| 126 | 63 | - | - | - | - | - | - | 5 | -100 |
| 127 | - | - | - | - | - | - | - | 3 | -100 |

Table 7. CIRCULAR TRANSLATOR TABLE

| Stepmode (<SM[2:0]>) | | | | | | | | % of I _{max} | |
|------------------------|------|------|-----|-----|----------|------------|------|-----------------------|------------|
| 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | Coil x | Coil y |
| 1/64 | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 comp | 1/2 uncomp | Full | | |
| 128 | 64 | 32 | 16 | 8 | 4 | 4 | - | 0 | -100 |
| 129 | - | - | - | - | - | - | - | -3 | -100 |
| 130 | 65 | - | - | - | - | - | - | -5 | -100 |
| 131 | - | - | - | - | - | - | - | -8 | -100 |
| 132 | 66 | 33 | - | - | - | - | - | -10 | -100 |
| 133 | - | - | - | - | - | - | - | -13 | -100 |
| 134 | 67 | - | - | - | - | - | - | -14 | -100 |
| 135 | - | - | - | - | - | - | - | -17 | -98 |
| 136 | 68 | 34 | 17 | - | - | - | - | -19 | -98 |
| 137 | - | - | - | - | - | - | - | -22 | -98 |
| 138 | 69 | - | - | - | - | - | - | -25 | -97 |
| 139 | - | - | - | - | - | - | - | -27 | -97 |
| 140 | 70 | 35 | - | - | - | - | - | -30 | -97 |
| 141 | - | - | - | - | - | - | - | -32 | -95 |
| 142 | 71 | - | - | - | - | - | - | -35 | -95 |
| 143 | - | - | - | - | - | - | - | -37 | -94 |
| 144 | 72 | 36 | 18 | 9 | - | - | - | -38 | -94 |
| 145 | - | - | - | - | - | - | - | -41 | -92 |
| 146 | 73 | - | - | - | - | - | - | -43 | -90 |
| 147 | - | - | - | - | - | - | - | -46 | -90 |
| 148 | 74 | 37 | - | - | - | - | - | -48 | -89 |
| 149 | - | - | - | - | - | - | - | -51 | -87 |
| 150 | 75 | - | - | - | - | - | - | -52 | -87 |
| 151 | - | - | - | - | - | - | - | -54 | -86 |
| 152 | 76 | 38 | 19 | - | - | - | - | -56 | -84 |
| 153 | - | - | - | - | - | - | - | -59 | -83 |
| 154 | 77 | - | - | - | - | - | - | -60 | -81 |
| 155 | - | - | - | - | - | - | - | -62 | -79 |
| 156 | 78 | 39 | - | - | - | - | - | -63 | -78 |
| 157 | - | - | - | - | - | - | - | -67 | -76 |
| 158 | 79 | - | - | - | - | - | - | -68 | -75 |
| 159 | - | - | - | - | - | - | - | -70 | -73 |
| 160 | 80 | 40 | 20 | 10 | 5 | 5 | 3 | -71 / -100 | -71 / -100 |
| 161 | - | - | - | - | - | - | - | -73 | -70 |
| 162 | 81 | - | - | - | - | - | - | -75 | -68 |
| 163 | - | - | - | - | - | - | - | -76 | -67 |
| 164 | 82 | 41 | - | - | - | - | - | -78 | -63 |
| 165 | - | - | - | - | - | - | - | -79 | -62 |
| 166 | 83 | - | - | - | - | - | - | -81 | -60 |
| 167 | - | - | - | - | - | - | - | -83 | -59 |
| 168 | 84 | 42 | 21 | - | - | - | - | -84 | -56 |
| 169 | - | - | - | - | - | - | - | -86 | -54 |
| 170 | 85 | - | - | - | - | - | - | -87 | -52 |
| 171 | - | - | - | - | - | - | - | -87 | -51 |
| 172 | 86 | 43 | - | - | - | - | - | -89 | -48 |
| 173 | - | - | - | - | - | - | - | -90 | -46 |
| 174 | 87 | - | - | - | - | - | - | -90 | -43 |
| 175 | - | - | - | - | - | - | - | -92 | -41 |
| 176 | 88 | 44 | 22 | 11 | - | - | - | -94 | -38 |
| 177 | - | - | - | - | - | - | - | -94 | -37 |
| 178 | 89 | - | - | - | - | - | - | -95 | -35 |
| 179 | - | - | - | - | - | - | - | -95 | -32 |
| 180 | 90 | 45 | - | - | - | - | - | -97 | -30 |
| 181 | - | - | - | - | - | - | - | -97 | -27 |
| 182 | 91 | - | - | - | - | - | - | -97 | -25 |
| 183 | - | - | - | - | - | - | - | -98 | -22 |
| 184 | 92 | 46 | 23 | - | - | - | - | -98 | -19 |
| 185 | - | - | - | - | - | - | - | -98 | -17 |
| 186 | 93 | - | - | - | - | - | - | -100 | -14 |
| 187 | - | - | - | - | - | - | - | -100 | -13 |
| 188 | 94 | 47 | - | - | - | - | - | -100 | -10 |
| 189 | - | - | - | - | - | - | - | -100 | -8 |
| 190 | 95 | - | - | - | - | - | - | -100 | -5 |
| 191 | - | - | - | - | - | - | - | -100 | -3 |

Table 7. CIRCULAR TRANSLATOR TABLE

| Stepmode (<SM[2:0]>) | | | | | | | | % of I _{max} | |
|------------------------|------|------|-----|-----|----------|------------|------|-----------------------|----------|
| 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | Coil x | Coil y |
| 1/64 | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 comp | 1/2 uncomp | Full | | |
| 192 | 96 | 48 | 24 | 12 | 6 | 6 | - | -100 | 0 |
| 193 | - | - | - | - | - | - | - | -100 | 3 |
| 194 | 97 | - | - | - | - | - | - | -100 | 5 |
| 195 | - | - | - | - | - | - | - | -100 | 8 |
| 196 | 98 | 49 | - | - | - | - | - | -100 | 10 |
| 197 | - | - | - | - | - | - | - | -100 | 13 |
| 198 | 99 | - | - | - | - | - | - | -100 | 14 |
| 199 | - | - | - | - | - | - | - | -98 | 17 |
| 200 | 100 | 50 | 25 | - | - | - | - | -98 | 19 |
| 201 | - | - | - | - | - | - | - | -98 | 22 |
| 202 | 101 | - | - | - | - | - | - | -97 | 25 |
| 203 | - | - | - | - | - | - | - | -97 | 27 |
| 204 | 102 | 51 | - | - | - | - | - | -97 | 30 |
| 205 | - | - | - | - | - | - | - | -95 | 32 |
| 206 | 103 | - | - | - | - | - | - | -95 | 35 |
| 207 | - | - | - | - | - | - | - | -94 | 37 |
| 208 | 104 | 52 | 26 | 13 | - | - | - | -94 | 38 |
| 209 | - | - | - | - | - | - | - | -92 | 41 |
| 210 | 105 | - | - | - | - | - | - | -90 | 43 |
| 211 | - | - | - | - | - | - | - | -90 | 46 |
| 212 | 106 | 53 | - | - | - | - | - | -89 | 48 |
| 213 | - | - | - | - | - | - | - | -87 | 51 |
| 214 | 107 | - | - | - | - | - | - | -87 | 52 |
| 215 | - | - | - | - | - | - | - | -86 | 54 |
| 216 | 108 | 54 | 27 | - | - | - | - | -84 | 56 |
| 217 | - | - | - | - | - | - | - | -83 | 59 |
| 218 | 109 | - | - | - | - | - | - | -81 | 60 |
| 219 | - | - | - | - | - | - | - | -79 | 62 |
| 220 | 110 | 55 | - | - | - | - | - | -78 | 63 |
| 221 | - | - | - | - | - | - | - | -76 | 67 |
| 222 | 111 | - | - | - | - | - | - | -75 | 68 |
| 223 | - | - | - | - | - | - | - | -73 | 70 |
| 224 | 112 | 56 | 28 | 14 | 7 | 7 | 0 | -71 / -100 | 71 / 100 |
| 225 | - | - | - | - | - | - | - | -70 | 73 |
| 226 | 113 | - | - | - | - | - | - | -68 | 75 |
| 227 | - | - | - | - | - | - | - | -67 | 76 |
| 228 | 114 | 57 | - | - | - | - | - | -63 | 78 |
| 229 | - | - | - | - | - | - | - | -62 | 79 |
| 230 | 115 | - | - | - | - | - | - | -60 | 81 |
| 231 | - | - | - | - | - | - | - | -59 | 83 |
| 232 | 116 | 58 | 29 | - | - | - | - | -56 | 84 |
| 233 | - | - | - | - | - | - | - | -54 | 86 |
| 234 | 117 | - | - | - | - | - | - | -52 | 87 |
| 235 | - | - | - | - | - | - | - | -51 | 87 |
| 236 | 118 | 59 | - | - | - | - | - | -48 | 89 |
| 237 | - | - | - | - | - | - | - | -46 | 90 |
| 238 | 119 | - | - | - | - | - | - | -43 | 90 |
| 239 | - | - | - | - | - | - | - | -41 | 92 |
| 240 | 120 | 60 | 30 | 15 | - | - | - | -38 | 94 |
| 241 | - | - | - | - | - | - | - | -37 | 94 |
| 242 | 121 | - | - | - | - | - | - | -35 | 95 |
| 243 | - | - | - | - | - | - | - | -32 | 95 |
| 244 | 122 | 61 | - | - | - | - | - | -30 | 97 |
| 245 | - | - | - | - | - | - | - | -27 | 97 |
| 246 | 123 | - | - | - | - | - | - | -25 | 97 |
| 247 | - | - | - | - | - | - | - | -22 | 98 |
| 248 | 124 | 62 | 31 | - | - | - | - | -19 | 98 |
| 249 | - | - | - | - | - | - | - | -17 | 98 |
| 250 | 125 | - | - | - | - | - | - | -14 | 100 |
| 251 | - | - | - | - | - | - | - | -13 | 100 |
| 252 | 126 | 63 | - | - | - | - | - | -10 | 100 |
| 253 | - | - | - | - | - | - | - | -8 | 100 |
| 254 | 127 | - | - | - | - | - | - | -5 | 100 |
| 255 | - | - | - | - | - | - | - | -3 | 100 |

Remarks:

- ◆ Positive coil current conducts from MOTXP to MOTXN or MOTYP to MOTYN.
- ◆ For some microstep positions 2 values are given for Coil X and Coil Y. The second value is only valid for <SM[2:0]> = "11x"

Direction

The direction of rotation can be changed by means of the DIR-pin and the SPI bit <DIRCTRL>. See also Figure 12 up to Figure 15. Setup and hold times need to be respected when changing direction (see Figure 6).

NXT Input

Every rising or falling edge on the NXT-pin (selectable through SPI bit <NXTP>) will move the coil current one step up or down (dependant on the DIR-pin and <DIRCTRL> bit) in the translator table (see Table 7). The motor current will be updated at the next PWM cycle.

Enable

The enable SPI bit <MOTEN> is used to enable the PWM regulator and drive coil current through the stepper motor coils. When '1' the motor driver is enabled and coil current will be conducted. If '0' (zero), the H-bridge drivers are disabled.

When the motor driver is enabled, the NXT- and DIR-pin as also the <DIRCTRL> SPI bit can be used to control the movement of the stepper motor. It's not allowed to apply pulses on the NXT-pin when the motor driver is disabled.

Certain errors (see Error Output p24) will automatically disable the motor driver (<MOTEN> = 0). The errors first need to be cleared before one is able to enable the motor driver again.

Setup and hold times need to be respected (see Figure 6).

Microstep Position

To be able to track the position in the current translator table (Table 7), the microstep position SPI byte can be used (<MSP[7:0]>). This byte gives the position within the current translator table in units of 1/64 microsteps. This means that when working in 1/4th microstepping the read out microstep positions will be 0, 16, 32, ...

The microstep position can be used to track/verify the real position of the stepper motor and as a reference point for changing the stepping mode (to avoid phase shift (see further)). See also Application Note AND8399 for more information on this (this application note is based on AMIS-305xx but is similar for AMIS-30421).

Keep in mind that <MSP[7:0]> will only be update 1 μ s after the NXT pulse was applied.

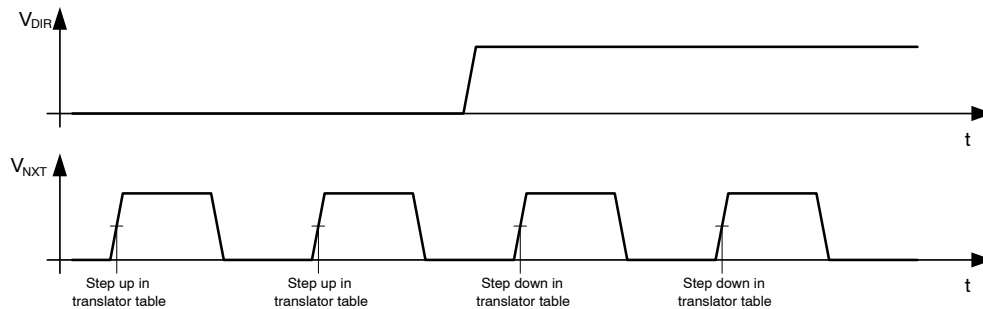


Figure 16. Translator table update

Microstep

<SM[2:0]> is used to set the microstep stepping mode. Changing to another microstep stepping mode can be done but the setup and hold timings need to be respected (see Figure 6). Additionally, one needs to be careful to not introduce an offset (or phase shift) in the translator table.

Increasing to a higher stepping mode (e.g. from 1/2 to 1/4) can be done at any moment without introducing an offset or phase shift. Decreasing to a lower stepping mode (e.g. from 1/4 to 1/2) can introduce an offset or phase shift if the change to the lower stepping mode is not done at the right moment. One needs to make sure that the translator table position is shared both by the old and new stepping mode setting. Figure 17 gives a good and bad example of reducing the stepping mode.

To avoid the creation of an offset it's advised to only change the stepping mode at a full-step position (<MSP[7:0]> equal to 0, 64, 128 or 192).

Changing the stepping mode to (or from) full step stepping mode also needs to be done with care. Changing to

full step mode at the moment the coil current is 100% in one of the coils will result in a movement of the rotor. Reversed, changing from full step to any other stepping mode will also result in a movement of the rotor (see Figure 18, top left).

If the stepping mode is changed to full step when the coil current in both coils is 71%, the coil current in both coils will only be 71% in full step stepping mode instead of 100% (see Figure 18, top right). Changing to full step stepping mode when the coil current in one of the coils is not 100% nor 71% will result in an offset (see Figure 18, bottom). Notice that stepping is now done on a rectangle instead of a square.

There will always be coil current present in both coils when working in full step stepping mode (see Table 7). When zero current is requested in one of the coils, half step stepping mode can be used to mimic full step (see section *Full Step Stepping Mode* in application note AND8399/D for more info).

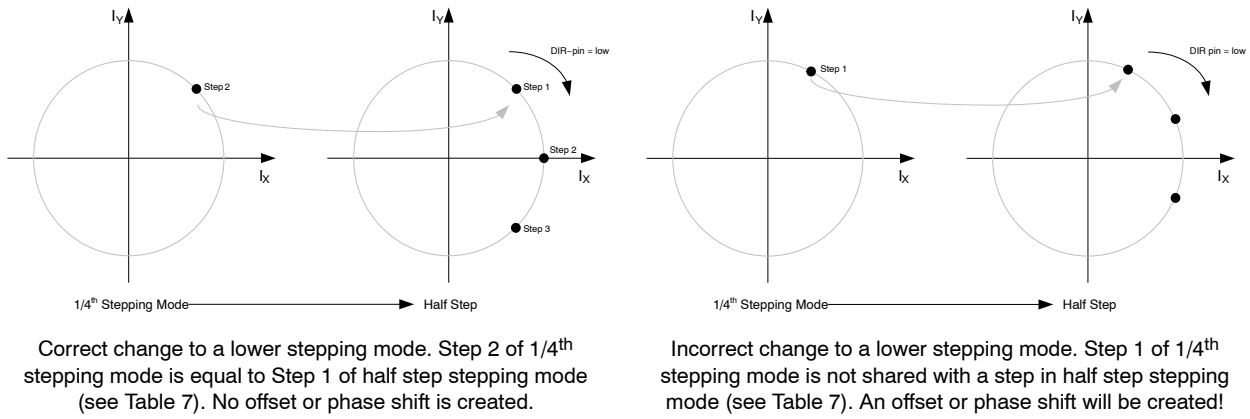


Figure 17. NXT-Step Mode Synchronization

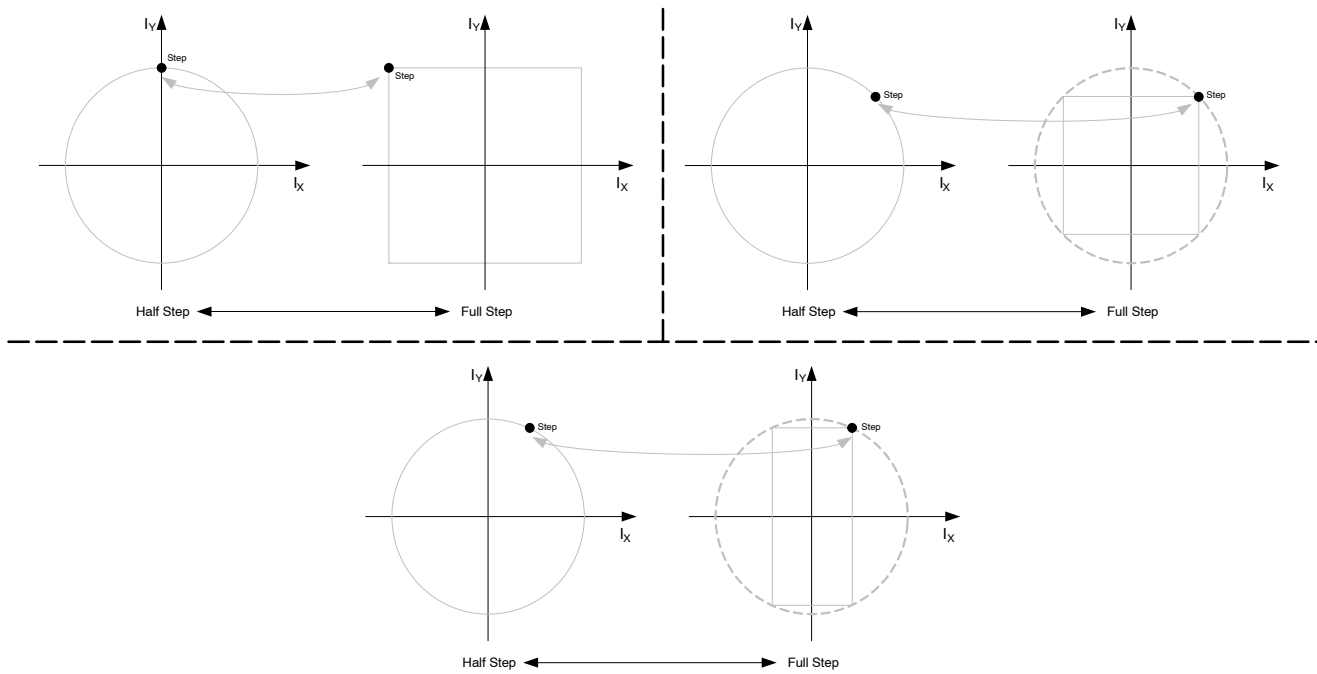


Figure 18. Changing to/from Full step Stepping Mode

Programmable Peak-Current

The amplitude of the current waveform in the motor coils (I_{max}) can be programmed through SPI bits <CUR[2:0]>. The coil current can be calculated as next:

$$I_{max} = \text{<CUR[2:0]>} / R_{SENSE}$$

R_{SENSE} is resistor R_1 and R_2 as given in Figure 9.

A change in the coil current (<CUR[2:0]>) will be updated at the next PWM cycle.

Clear

Logic 0 on the CLR-pin allows normal operation of the chip. To clear the complete digital inside AMIS-30421, the CLR-pin needs to be pulled to logic 1 for a minimum time of t_{CLR} (Table 5). Clearing the motor driver can not be done during Sleep Mode. During a clear the charge pump remains

active. The voltage regulator remains functional during and after the clear action and the WDb-pin is not activated.

After a clear, NXT pulses can be applied after t_{CLR_SET} (see Figure 7).

Speed and Load Angle Output

The SLA-pin provides an output voltage that indicates the level of the BEMF (Back Electro Magnetic Force) voltage of the motor. This BEMF voltage is sampled during every so-called "coil current zero crossing". Per coil, two zero-current positions exist per electrical period, yielding in a total of four zero-current observation points per electrical period.

Because of the relatively high recirculation currents in the coil during current decay, the coil voltage V_{COIL} shows a

transient behavior. This transient behavior (which is not the BEMF) can be made visible or invisible on the SLA-pin by means of SPI bit <SLAT>. When set to transparent (<SLAT> = '1'), the coil voltage is sampled every PWM cycle and updated on the SLA-pin (see Figure 19). When set to not-transparent (<SLAT> = '0'), only the last sample (taken right before leaving the “coil current zero crossing”) will be copied to the SLA-pin (see Figure 20).

When working in not-transparent mode (<SLAT> = '0') keep in mind that there is a delay between applying the NXT pulse (to leave the “coil current zero crossing”) and the updated voltage on the SLA-pin (see t_{SLA_DELAY} in Figure 20 and Table 5).

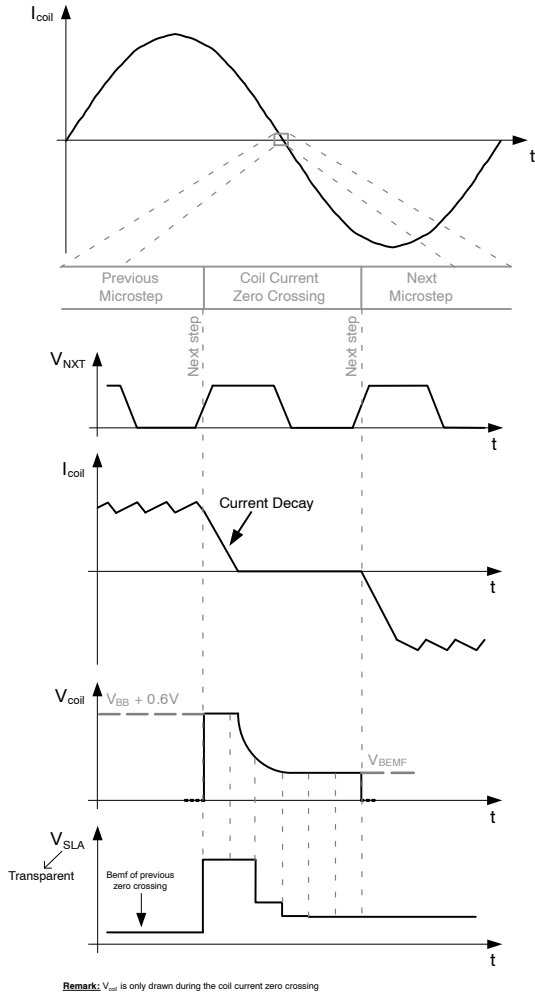


Figure 19. Principle of BEMF Measurement in Transparent Mode

The relationship between the voltage measured on the SLA-pin and the coil voltage is:

$$V_{SLA} = 0.6 + (0.6 \times \langle SLA_OFFS \rangle) + (V_{coil} \times \langle SLAG \rangle)$$

SPI bit <SLA_OFFS> can be used to add an additional offset of 0.6 V. Five different SLA gain values can be set by means of SPI bits <SLAG[2:0]>.

AMIS-30421 has the ability to stretch the “coil current zero crossing”. If NXT pulses are applied too fast it’s possible that the “coil current zero crossing” is too short making it impossible to measure the real BEMF (see

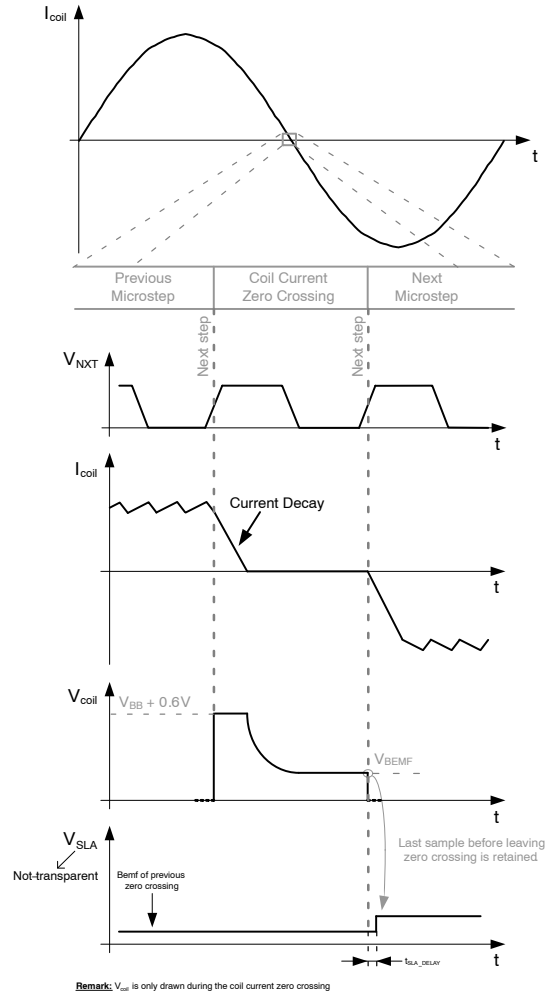


Figure 20. Principle of BEMF Measurement in Not-Transparent Mode

Figure 21). By using SPI bits <MIN_SLA_TIME[1:0]> one can stretch the “coil current zero crossing” without changing the speed of the motor (see Figure 21). AMIS-30421 will ignore but keep track of the NXT pulses applied during the “stretched coil current zero crossing” and compensate the ignored pulses when leaving the “coil current zero crossing”.

More information on using the SLA-pin can be found in application note AND8399. Although this application note refers to AMIS-305xx, it is also valid for AMIS-30421.

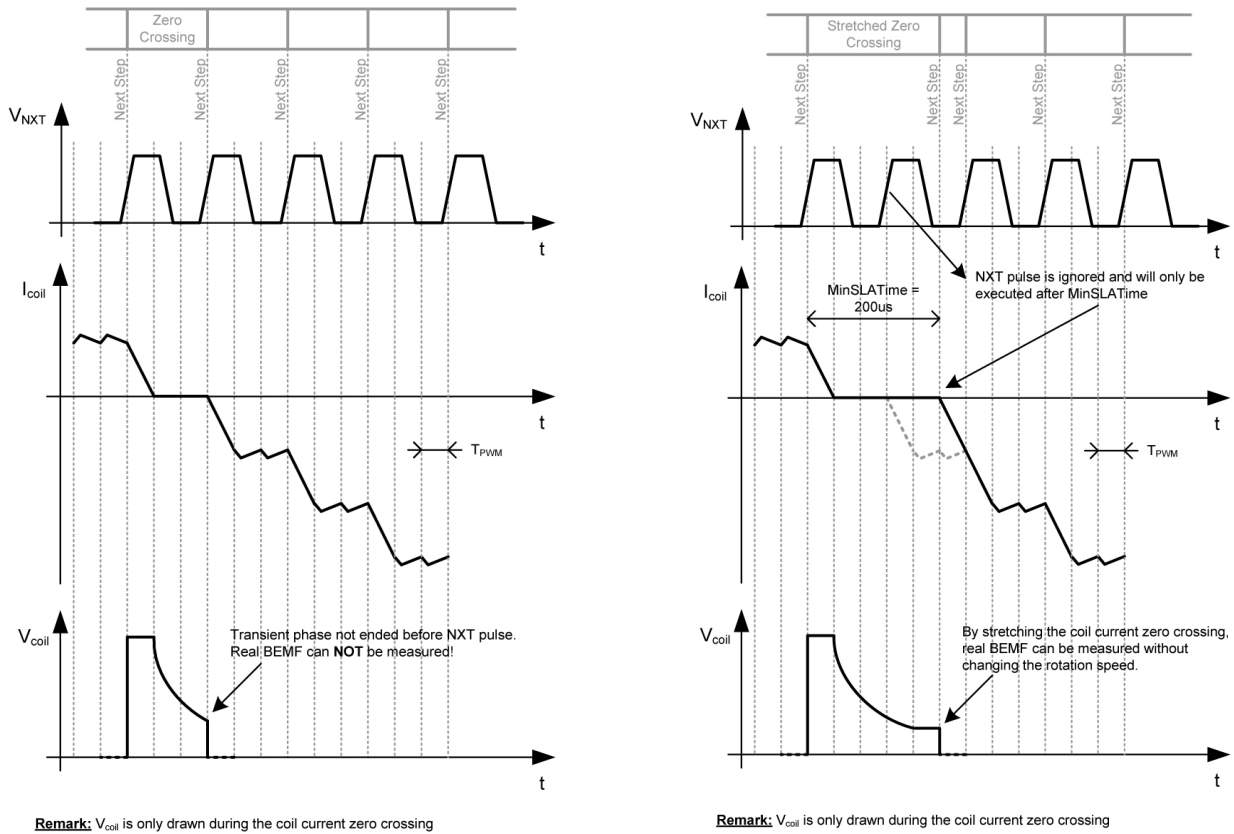


Figure 21. BEMF sampling without (left) and with (right) zero crossing stretching

Sleep Mode

AMIS-30421 can be placed in Sleep Mode by means of SPI bit <SLP>. This mode allows reduction of current-consumption when the motor is not in operation. The effect of sleep mode is as follows:

- The drivers are put in HiZ
- All analog circuits are disabled and in low-power mode
- All SPI registers maintain their logic content
- SPI communication is still possible (slightly current increase during SPI communication).
- Status Registers can not be cleared by reading out
- NXT and DIR inputs are forbidden
- Oscillator and digital clocks are silent
- Motor driver can not be cleared by means of the CLR-pin

The voltage regulator remains active but with reduced current-output capability (I_{LOAD_PD}).

When Sleep Mode is left a start-up time is needed for the charge pump to stabilize. After this time (t_{SLP_SET}) NXT commands can be issued (see also Figure 6). Enabling the motor when the charge pump is not stable can result in overcurrent errors (see section *Over-Current Detection*). Because of this it's advised to keep the motor disabled during the stabilization time (t_{SLP_SET}).

The IO-pins of AMIS-30421 have internal pull-down or pull-up resistors (see Figure 3). Keep this in mind when entering Sleep Mode.

In Sleep Mode V_{DD} can drop to 2.1 V minimum (see V_{DD_SLEEP} in Table 4). Keep in mind that in this case it's not allowed to pull the input pins above 2.1 V!

WARNING, ERROR DETECTION AND DIAGNOSTICS FEEDBACK

Thermal Warning and Shutdown

AMIS-30421 has 4 thermal ranges which can be read out through SPI bits <TR[1:0]> and <TSD>. Thermal Range 1 goes from -40°C up to T₁. Thermal Range 2 goes from T₁ to T₂ and Thermal Range 3 goes from T₂ up to T₃ (T₁, T₂ and T₃ can be found in Table 4). Once above T₃ the 4th thermal level is reached which is the thermal warning range.

When junction temperature rises above T_{TW} (= T₃), the ERRb-pin will be activated. If junction temperature increases above thermal shutdown level (T_{TSD}), then the circuit goes in Thermal Shutdown Mode and all driver transistors are disabled (high impedance). The condition to get out of the Thermal Shutdown Mode is to be at a temperature lower than T_{TW} and by clearing the <TSD> SPI bit.

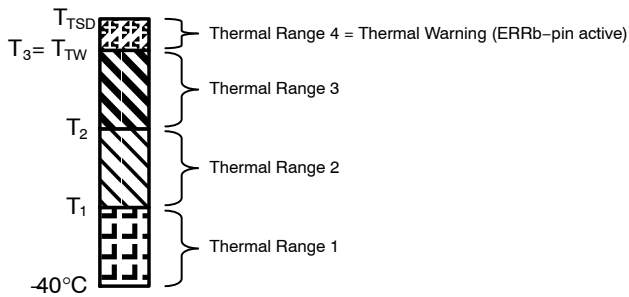


Figure 22. Thermal Ranges

Over-Current Detection

The over-current detection circuit monitors the load current in each activated output stage. If the load current exceeds the over-current detection threshold, the ERRb-pin will be activated and the drivers are switched off (motor driver disabled) to reduce the power dissipation and to protect the H-bridge. Each driver has an individual detection bit (see Status Register 1 and 2). The error condition is latched and the microcontroller needs to read out the error to reset the error and to be able to re-enable the motor driver again.

Note: Successive resetting the motor driver in case of a short circuit condition may damage the drivers.

Open Coil/Current Not Reached Detection

Open coil detection is based on the observation of 100% duty cycle of the PWM regulator. If in a coil 100% duty cycle is detected for a certain time, an open coil will be latched (see Status Register 1 and 2) and the ERRb-pin will be activated (drivers are disabled). The time this 100% duty cycle needs to be present is adjustable with SPI bits <OPEN_COIL[1:0]>. A short time will result in fast detection of an open-coil but could also trigger unwanted open-coil errors. Increase the timing if this is the case.

When the resistance of a motor coil is very large and the supply voltage is low, it can happen that the motor driver is not able to deliver the requested current to the motor. Under these conditions the PWM controller duty cycle will be 100% and the ERRb-pin will flag this situation. This feature can be used to test if the operating conditions (supply voltage, motor coil resistance) still allow reaching the requested coil-current or else the coil current should be reduced.

Note: A short circuit could trigger an open coil.

Charge Pump Failure

The charge pump is an important circuit that guarantees low R_{DS(on)} for all external MOSFET's, especially for low supply voltages. If supply voltage is too low or external components are not properly connected to guarantee a low R_{DS(on)} of the drivers, a charge pump failure is latched (<CPFAIL>), the ERRb-pin is activated and the driver is disabled (<MOTEN> = '0'). One needs to read Status Register 1 to clear the charge pump failure.

After power on reset (POR) the charge pump voltage will need some time to exceed the required threshold. During that time the ERRb-pin will be active but not latched for 250µs. If the slope of the power supply V_{BB} is slow during power up (charge pump not started after 250 µs), a charge pump failure will be latched and the ERRb-pin is activated (see also Figure 23).

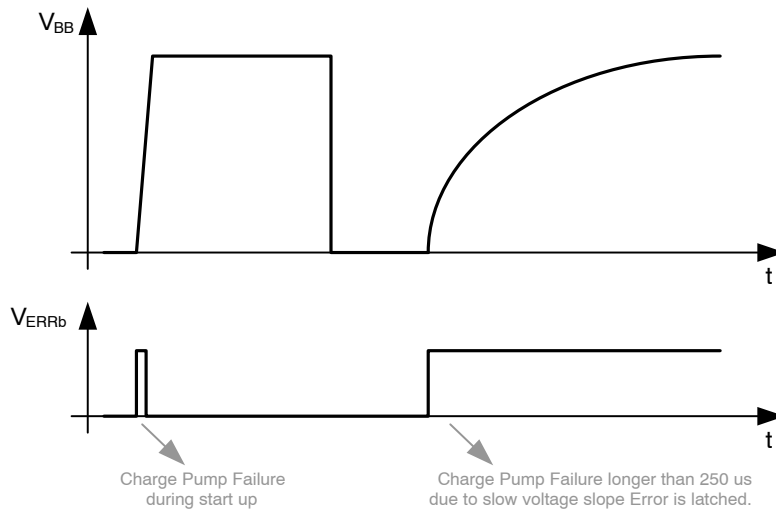


Figure 23. Charge Pump Failure

Watchdog

When V_{BB} is applied, the WDb-pin is kept low for t_{por} (Table 5). This can for instance be used to reset an external microcontroller at power up.

The WDb-pin also has a second function, a Watchdog function. When the watchdog is enabled ($\langle WDEN \rangle = '1'$), a timer will start counting up. When the counter reaches a certain value ($\langle WDT[3:0] \rangle$), the $\langle WD \rangle$ SPI bit will be set and the WDb-pin will be pulled low for a time equal to t_{POR} to reset the external microcontroller. To avoid that the microcontroller gets reset, the microcontroller needs to re-enable the watchdog before the count value is reached (= write '1' to $\langle WDEN \rangle$ before $\langle WDT[3:0] \rangle$ is reached). This functionality can be used to reset a “stuck” microcontroller.

The SPI bit $\langle WD \rangle$ can be used to detect a cold or warm boot. When powering the application (cold boot), $\langle WD \rangle$ will be zero. If the microcontroller has been reset by the WDb-pin (warm boot), $\langle WD \rangle$ bit will be '1'. The microcontroller can use this information to detect a cold or warm boot.

It's forbidden to re-enable the watchdog too fast (minimum time between re-enabling must be above t_{WDPR} (see Figure 4)). One may also not enable the watchdog too fast after power up (see t_{DSPI} , Figure 4).

A small analogue filter avoids resetting due to spikes or noise on the VDD supply (t_{rf}).

During and after power up the WDb-pin is an open drain output. One can change this to a push-pull output by using SPI bit $\langle IO_OT \rangle$.

Error Output

The error output (ERRb-pin) will be activated if an error is reported. Next errors will be reported:

- Thermal Warning
- Thermal Shutdown
- Overcurrent
- Open Coil
- Charge Pump Failure
- All errors except a Thermal Warning will disable the H-bridge drivers to protect the motor driver ($\langle MOTEN \rangle = '0'$). To reset the error one needs to read out the error. Only when all errors are reset it will be possible to re-enable the motor driver ($\langle MOTEN \rangle = '1'$).

Keep in mind that during power up a charge pump failure will be reported during the first 250us but will not be latched (see also *Charge Pump Failure*).

During and after power up the ERRb-pin is an open drain output. One can change this to a push-pull output with SPI bit $\langle IO_OT \rangle$.

POWER SUPPLY AND THERMAL CALCULATION

Logic Supply Regulator

AMIS-30421 has an on-chip 3.3V low-drop regulator to supply the digital part of the chip itself, some low-voltage analog blocks and external circuitry. See Table 4 for the limitations.

Over- and Undervoltage

AMIS-30421 has undervoltage detection. If V_{BB} drops below V_{BBUL} , the drivers are disabled. To be able to enable the drivers again the V_{BB} voltage needs to rise above V_{BBUH} .

Overvoltage detection is also present. If the voltage rises above V_{BBOH} the drivers are disabled. The voltage needs to drop below V_{BBOL} to be able to enable the driver again. See also Figure 5.

Start-Up Behavior

Figure 4 gives the start-up of AMIS-30421. After V_{BB} is applied and after a certain power up time (t_{PU}), the internal voltage regulator V_{DD} will start-up. When V_{DD} gets above V_{DDH} , the internal POR will be released and the digital will start-up. The WDb-pin will be kept low for an additional 100ms (t_{POR}). After the WDb-pin is deactivated and after a time t_{DSPI} , SPI communication can be initiated.

Junction Temperature Calculation

To calculate the junction temperature of AMIS-30421 the thermal resistance junction-to-ambient must be known. When only a PCB heat sink is used, a typical value is 30°C/W (see Table 4).

There are three modes the junction temperature can be calculated for.

- In Sleep Mode (<SLP> = '1') the V_{BAT} consumption is maximum 150 μ A making $T_j = T_{amb}$.
- In Normal Mode when the driver is disabled (<MOTEN> = '0'), the V_{BAT} consumption is maximum 20 mA (no external load on VDD-pin). The junction temperature can be calculated as next:

$$T_j = T_A + (V_{BAT} \times I_{BAT} \times R_{thJA})$$

For an 18 V application operating at an ambient temperature of 125°C this would give:

$$T_j = 125^\circ C + (18 V \times 20 mA \times 30^\circ C/W)$$

$$T_j = 135.8^\circ C$$

- In Normal Mode with the driver enabled (<MOTEN> = '1') the gate charge current needs to be included in the calculations.

$$I_{BAT} = 20 mA + (6 \times V_{REGH} \times C_{ISS} \times f_{PWM})$$

For an 18 V application driving external MOSFET's with an input capacitance of 1 nF this would result in:

$$I_{BAT} = 20 mA + (6 \times 12.8 V \times 1 nF \times 30 kHz)$$

$$I_{BAT} = 22.3 mA$$

Operating at 125°C ambient temperature this result in a junction temperature of:

$$T_j = 125^\circ C + (18 V \times 22.3 mA \times 30^\circ C/W)$$

$$T_j = 137^\circ C$$

SPI INTERFACE

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS-30421. The implemented SPI block is designed to interface directly with numerous microcontrollers from several manufacturers. AMIS-30421 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI).

DO signal is the output from the Slave (AMIS-30421), and DI signal is the output from the Master. A chip select line (CSb) allows individual selection of a Slave SPI device in a multiple-slave system. The CSb line is active low. If AMIS-30421 is not selected, DO is in HiZ and does not interfere with SPI bus activity. The output type of DO can be set in SPI (<IO_OT>). Since AMIS-30421 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

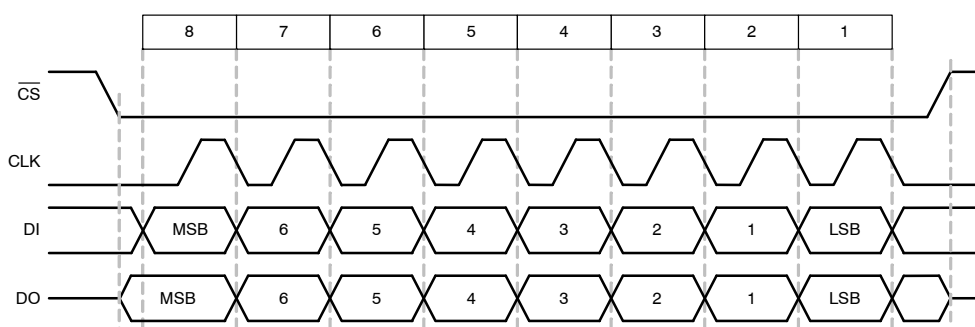


Figure 24. Timing Diagram of a SPI Transfer

Transfer Packet

Serial data transfer is assumed to follow MSB first rule. The transfer packet contains one or more bytes.

Byte 1 contains the Command and the SPI Register Address and indicates to AMIS-30421 the chosen type of operation and addressed register. Byte 2 contains data, or sent from the Master in a WRITE operation, or received from AMIS-30421 in a READ operation.

Two command types can be distinguished in the communication between master and AMIS-30421:

- CMD2 = '0': READ from SPI Register with address ADDR[4:0]
- CMD2 = '1': WRITE to SPI Register with address ADDR[4:0]

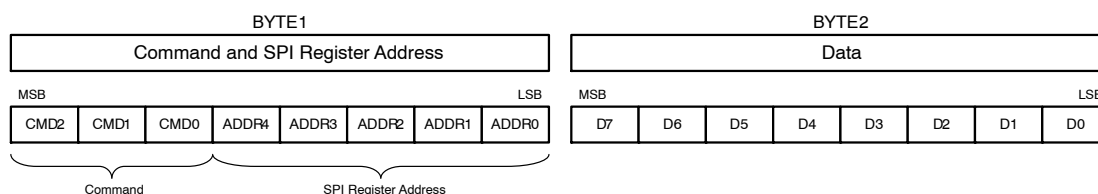


Figure 25. SPI Transfer Packet

READ Operation

If the Master wants to read data from a Status or Control Register, it initiates the communication by sending a READ command. This READ command contains the address of the SPI register to be read out. At the falling edge of the eight clock pulse the data-out shift register is updated with the content of the corresponding internal SPI register. In the next 8-bit clock pulse train this data is shifted out via DO pin. At

the same time the data shifted in from DI (Master) should be interpreted as the following successive command or dummy data.

Status Register 0, 1 and 2 (see SPI Registers) contain 7 data bits and a parity check bit. The most significant bit (D7) represents a parity of D[6:0]. If the number of logical ones in D[6:0] is odd, the parity bit D7 equals '1'. If the number of logical ones in D[6:0] is even then the parity bit D7 equals

'0'. This simple mechanism protects against noise and increases the consistency of the transmitted data. If a parity check error occurs it is recommended to initiate an additional READ command to obtain the status again.

The CSb-pin is active low and may remain low between successive READ commands as illustrated in Figure 28. There is one exception. In case an error condition occurs the

root cause of the problem can be determined by reading out the Status Registers. However, if the error occurs at the moment CSb is low, one first needs to pull CSb high to update the Status Registers properly. Only then the Status Registers can be read out to determine the error. For this reason it is also recommended to keep CSb high when the SPI bus is idle.

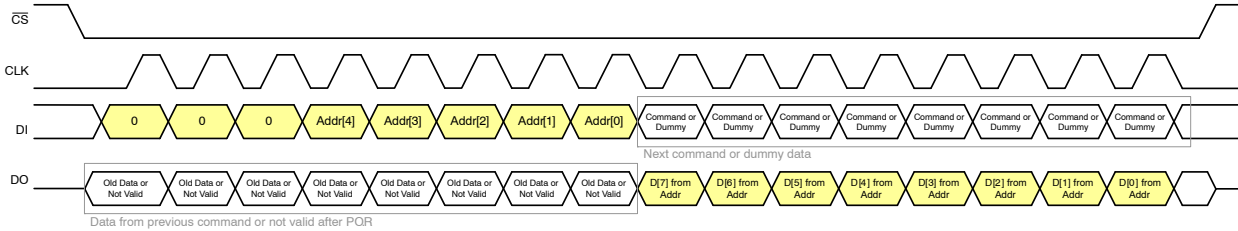


Figure 26. Single READ Operation Where Data from SPI Register is Read by the Master

WRITE Operation

If the Master wants to write data to a Control Register it initiates the communication by sending a WRITE command. This contains the address of the SPI register to write to. The command is followed with a data byte. This incoming data will be stored in the corresponding Control Register after CSb goes from low to high. It is important that the writing action to the Control Register is exactly 16 bits long and that CSb goes high after these 16 bits. If more or

less bits are transmitted the complete transfer packet is ignored.

A WRITE command executed for a read-only register (e.g. Status Registers) will not affect the addressed register and the device operation.

AMIS-30421 responds on every incoming byte by shifting out via DO the data stored in the last received address. Because after a power-on-reset the initial address is unknown the data shifted out via DO is not valid.

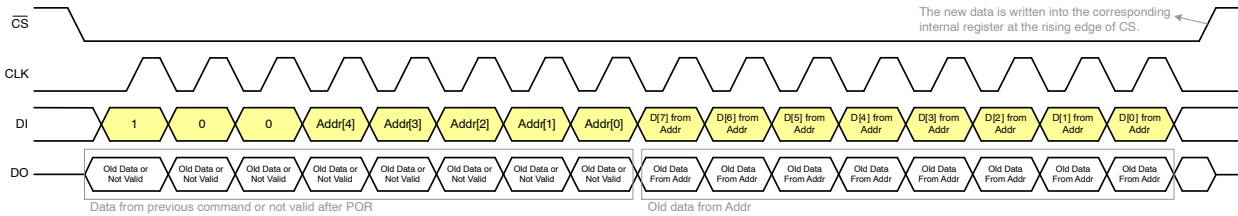


Figure 27. Single WRITE Operation Where Data from the Master is Written in SPI Register

Examples of READ and WRITE Operations

In the following examples successive READ and/or WRITE operations are combined. In Figure 28 the Master first reads the status from Register at Addr1 and at Addr2

followed by writing a control byte in Control Register at Addr3. Note that during the WRITE command the old data of the pointed register is returned at the moment the new data is shifted in.

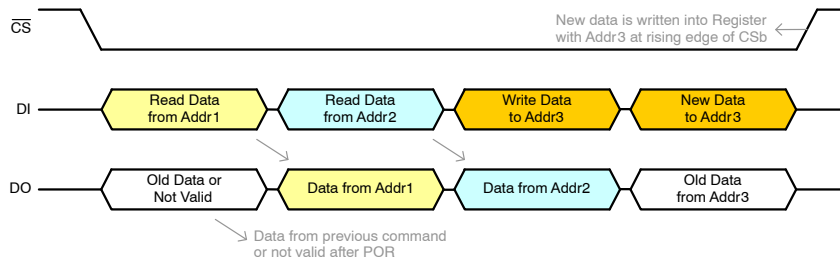


Figure 28. 2 Successive READ Commands Followed by a WRITE Command

After a WRITE operation the Master could initiate a READ command in order to verify the data correctly written as illustrated in Figure 29. During reception of the READ

command the old data is returned for a second time. Only after receiving the READ command the new data is transmitted. This rule also applies when the master device

wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status

Registers only when CSb line is high, the first read out byte might represent old status information (Figure 30).

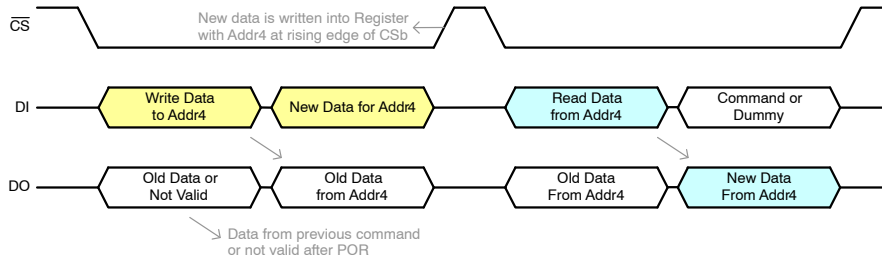


Figure 29. WRITE Operation Followed by a READ operation to verify

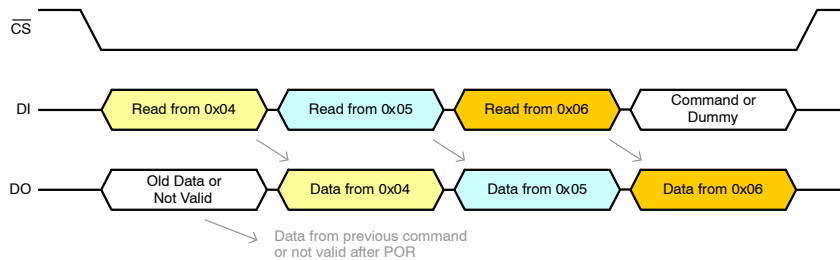


Figure 30. 3 READ Operations in a Row

Bad Examples of READ and WRITE Operations

The following example demonstrates a bad WRITE operation. After a WRITE operation a read operation is done before CSb is made high. The data will not be written in the Register. Figure 32 demonstrates how it should be done (see also Figure 29).

The second example (Figure 33) demonstrates an incorrect way of reading errors. After a WRITE operation the ERRb-pin toggles indication an error. Without toggling CSb the 3 Status Registers are read out to determine the error. Because CSb was not high after the error was detected, the Status Registers will not be updated and the error can not

be determined. A second problem with Figure 33 is that the data written to Addr9 will not be stored because CSb was not toggled after the write operation.

Figure 34 gives the correct way of reading out errors. When the error is detected (toggling of ERRb-pin), CSb is made high to make sure the Status Registers are updated. Then the Status Registers are read out. Notice that ERRb toggles after Status Register 1 is read out (Addr 0x05). This indicates that the error was an overcurrent in the X-coil, a charge pump failure or an open X-coil. Also notice that because CSb is made high after the write operation, the write operation will now be done correctly.

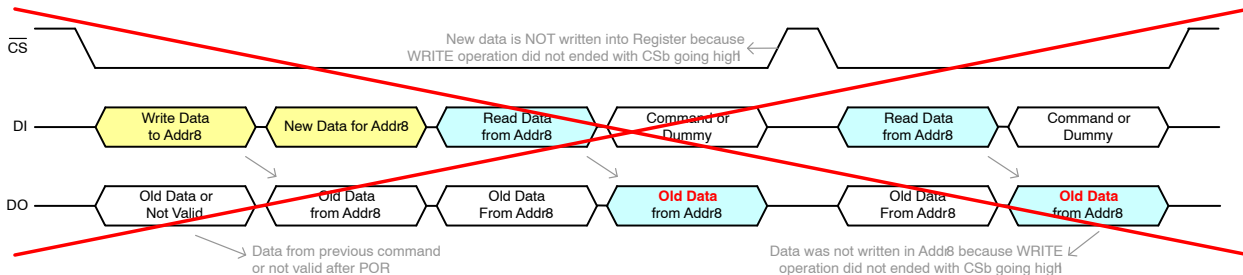


Figure 31. Bad Example of Write Operation

AMIS-30421

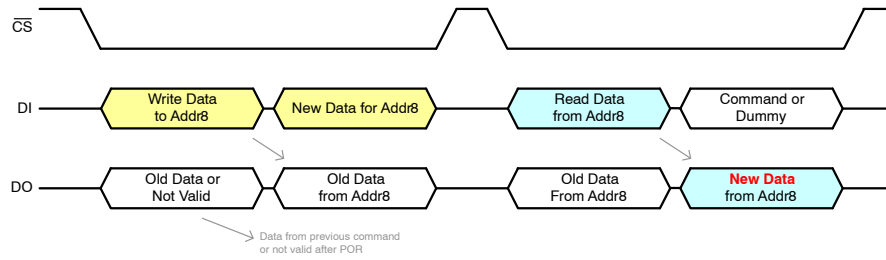


Figure 32. Good Write Operation

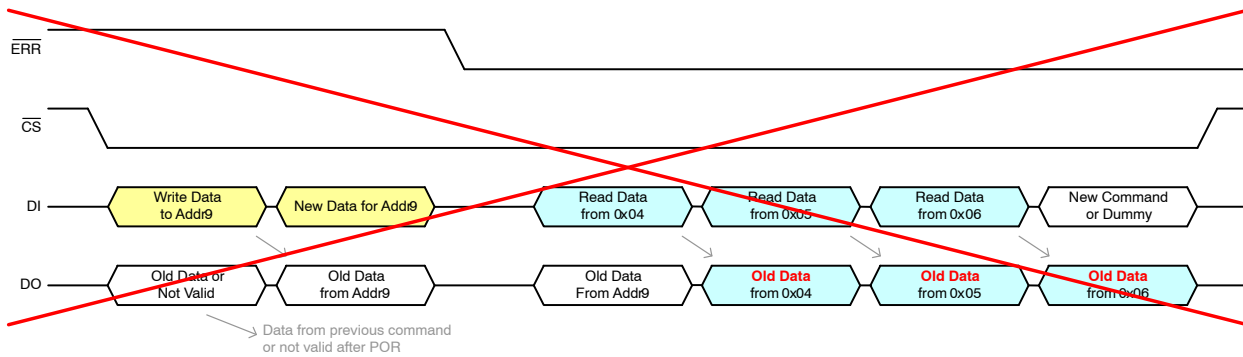


Figure 33. Bad Example of Error Read Out

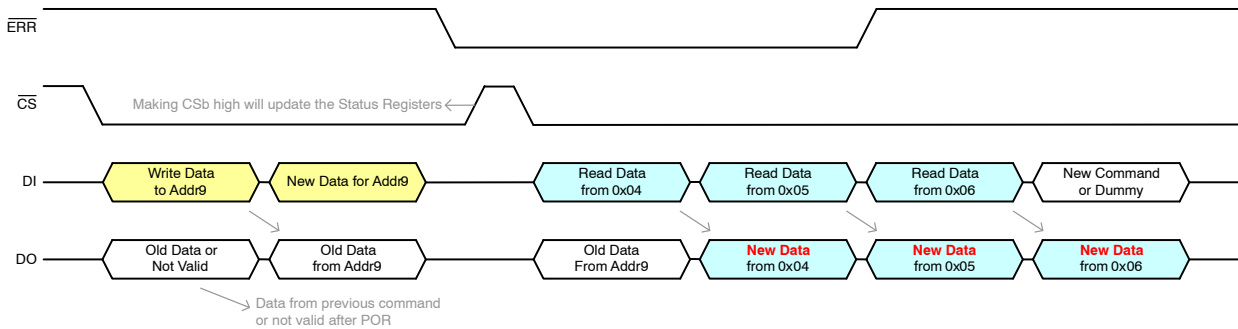


Figure 34. Correct Read Out of Error

SPI Register Description

Below table gives an overview of all SPI Registers that can be used.

Table 8. SPI REGISTER OVERVIEW

| SPI Register | Address | Access | Abbreviation |
|----------------------|---------|--------|--------------|
| Watchdog Register | 0x00 | R/W | WR |
| Control Register 0 | 0x01 | R/W | CR0 |
| Control Register 1 | 0x02 | R/W | CR1 |
| Control Register 2 | 0x03 | R/W | CR2 |
| Status Register 0 | 0x04 | R | SR0 |
| Status Register 1 | 0x05 | R | SR1 |
| Status Register 2 | 0x06 | R | SR2 |
| Status Register 3 | 0x07 | R | SR3 |
| Predriver Register 0 | 0x09 | R/W | PDRV0 |

Table 8. SPI REGISTER OVERVIEW

| SPI Register | Address | Access | Abbreviation |
|----------------------|---------|--------|--------------|
| Predriver Register 1 | 0x0A | R/W | PDRV1 |
| Predriver Register 2 | 0x0B | R/W | PDRV2 |
| Predriver Register 3 | 0x0C | R/W | PDRV3 |
| Predriver Register 4 | 0x0D | R/W | PDRV4 |
| Predriver Register 5 | 0x0E | R/W | PDRV5 |
| Predriver Register 6 | 0x0F | R/W | PDRV6 |
| Predriver Register 7 | 0x10 | R/W | PDRV7 |

Where: R/W = read and write access, R = read access only

Watchdog Register (WR)

The Watchdog Register is located at address 0x00 and can be used to enable the watchdog and set the watchdog time-out. It can also be used to set the short circuit and open coil detection time-out.

Table 9. WATCHDOG REGISTER

| Watchdog Register (WR) | | | | | | | | | |
|------------------------|--------|-------|----------|-------|-------|-------|----------------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x00 | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | Data | WDEN | WDT[3:0] | | | | OPEN_COIL[1:0] | | - |

Table 10. WATCHDOG REGISTER PARAMETERS

| Parameter | Value | Value | Description | Info |
|----------------|--------|-----------|--|------|
| WDEN | 0 | Disable | Enables the watchdog | p24 |
| | 1 | Enable | | |
| WDT[3:0] | 0000 | 32 ms | Defines the watchdog time-out period. The watchdog needs to be re-enabled (WDEN) within this time or WDb-pin is activated for t_{POR} . | p24 |
| | 0001 | 64 ms | | |
| | 0010 | 96 ms | | |
| | 0011 | 128 ms | | |
| | 0100 | 160 ms | | |
| | 0101 | 192 ms | | |
| | 0110 | 224 ms | | |
| | 0111 | 256 ms | | |
| | 1000 | 288 ms | | |
| | 1001 | 320 ms | | |
| | 1010 | 352 ms | | |
| | 1011 | 384 ms | | |
| | 1100 | 416 ms | | |
| | 1101 | 448 ms | | |
| 1110 | 480 ms | | | |
| 1111 | 512 ms | | | |
| OPEN_COIL[1:0] | 00 | 2.56 ms | Defines the open coil detection time-out. If an open coil is detected for a time longer than OpenTimeOut[1:0], an open coil (OPEN_X and/or OPEN_Y) will be reported. Note: Short circuit could trigger open coil detection. | p23 |
| | 01 | 0.32 ms | | |
| | 10 | 20.48 ms | | |
| | 11 | 163.84 ms | | |

Remark: Bit 0 of Watchdog Register should always be '0' (zero)!

Control Register 0 (CR0)

Control Register 0 is located at address 0x01 and is used to set the maximum coil current and stepping mode. It's also used to set the “coil current zero crossing” duration.

Table 11. CONTROL REGISTER 0

| Control Register 0 (CR0) | | | | | | | | | |
|--------------------------|--------|---------|-------|-------|-------------------|-------|----------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x01 | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | SM[2:0] | | | MIN_SLA_TIME[1:0] | | CUR[2:0] | | |

Table 12. CONTROL REGISTER 0 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-------------------|-------|-------------------------|---|------|
| SM[2:0] | 000 | 64 th | Defines the 8 stepping modes for the PWM regulator. | p19 |
| | 001 | 32 nd | | |
| | 010 | 16 th | | |
| | 011 | 8 th | | |
| | 100 | 4 th | | |
| | 101 | Half step compensated | | |
| | 110 | Half step uncompensated | | |
| | 111 | Full Step | | |
| MIN_SLA_TIME[1:0] | 00 | 40 μs | Defines the minimum “coil current zero crossing” duration. Remark: when NXT frequency gets above PWM frequency (f _{PWM}), MIN_SLA_TIME could be 40us longer. | p20 |
| | 01 | 120 μs | | |
| | 10 | 200 μs | | |
| | 11 | 360 μs | | |
| CUR[2:0] | 000 | 100 mV | Defines the maximum voltage over the coil current sense resistor which defines the maximum coil current. The maximum coil current is calculated as next: $I_{coil} = CUR[2:0] / R_{sense}$ | p20 |
| | 001 | 135 mV | | |
| | 010 | 200 mV | | |
| | 011 | 270 mV | | |
| | 100 | 335 mV | | |
| | 101 | 400 mV | | |
| | 110 | 500 mV | | |
| | 111 | 600 mV | | |

Control Register 1 (CR1)

Control Register 1 is located at address 0x02 and can used to set the direction, NXT-pin polarity, output configuration of WDb-, ERRb- and DO-pin and to enable PWM jitter. It can also be used to set an additional delay between switching off and on MOSFET's of one half H-bridge (to prevent a short circuit).

Table 13. CONTROL REGISTER 1

| Control Register 1 (CR1) | | | | | | | | | |
|--------------------------|--------|---------|-------|-------|-------|-------|-------|---------------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x02 | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| | Data | DIRCTRL | NXTP | - | IO_OT | - | PWMJ | NO_CROSS[1:0] | |

Table 14. CONTROL REGISTER 1 PARAMETERS

| Parameter | Value | Value | Description | Info |
|---------------|-------|---------------|--|------|
| DIRCTRL | 0 | CW | Defines the direction of rotation. <u>Remark:</u> CW and CCW is relative. Direction of rotation will be defined by the status of the DIR-pin and connection of the stepper motor! | p19 |
| | 1 | CCW | | |
| NXTP | 0 | Positive Edge | Defines the active edge on the NXT-pin. | p19 |
| | 1 | Negative Edge | | |
| IO_OT | 0 | Push Pull | Defines the output type of WDb-, ERRb- and DO-pin | p24 |
| | 1 | Open Drain | | |
| PWMJ | 0 | Disabled | Enables or disables PWM jitter | p15 |
| | 1 | Enabled | | |
| NO_CROSS[1:0] | 00 | 0 ns | Defines the time between switching off one MOSFET and switching on the other MOSFET of the same half H-bridge (= $t_{nocross}$). | p13 |
| | 01 | 250 ns | | |
| | 10 | 500 ns | | |
| | 11 | 1000 ns | | |

Remark: Bit 3 and bit 5 of Control Register 1 should always be '0' (zero)!

Control Register 2 (CR2)

Control Register 2 is located at address 0x03 and can be used to enable the motor driver and to put the motor driver in sleep mode. It also has some parameters that can be used to set the SLA.

Table 15. CONTROL REGISTER 2

| Control Register 2 (CR2) | | | | | | | | | |
|--------------------------|--------|-------|-------|-------|-------|-----------|-------|-------|----------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x03 | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | MOTEN | SLP | - | SLAT | SLAG[2:0] | | | SLA_OFFS |

Table 16. CONTROL REGISTER 2 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-----------|-------|-----------------|---|------|
| MOTEN | 0 | Disabled | Enables the PWM regulator. <u>Remark:</u> the regulator is automatically disabled if one of the bits in Status Register 1 or 2 is set. | p19 |
| | 1 | Enabled | | |
| SLP | 0 | Normal Mode | Enables the sleep mode (power down mode) | p22 |
| | 1 | Sleep Mode | | |
| SLAT | 0 | Not Transparent | Defines the type of SLA sampling. | p20 |
| | 1 | Transparent | | |
| SLAG[2:0] | 000 | 1 | Defines the motor terminal voltage division factor for the SLA-pin. | p20 |
| | 001 | 0.5 | | |
| | 010 | 0.25 | | |
| | 011 | 0.125 | | |
| | 100 | 0.0625 | | |
| | 101 | 0.0625 | | |
| | 110 | 0.0625 | | |
| | 111 | 0.0625 | | |

Table 16. CONTROL REGISTER 2 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-----------|-------|----------------------------|--|------|
| SLA_OFFS | 0 | No additional offset | To enable an additional offset on the SLA-pin of 0.6V. | p20 |
| | 1 | Additional offset of 0.6 V | | |

Remark: Bit 5 of Control Register 2 should always be ‘0’ (zero)!

Status Register 0 (SR0)

Status Register 0 is located at address 0x04 and can only be read. Status Register 0 is a non-latched register meaning that the value of the register can change without the need of reading out the register. The register can be used to retrieve the temperature range or to verify a watchdog event.

Notice that bit 7 is the parity bit (see READ operation p26).

Table 17. STATUS REGISTER 0

| Status Register 0 (SR0) | | | | | | | | | |
|-------------------------|--------|-------|---------|-------|-------|-------|-------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x04 | Access | R | R | R | R | R | R | R | R |
| | Reset | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | Data | PAR | TR[1:0] | | WD | - | - | - | - |

Table 18. STATUS REGISTER 0 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-----------|-------|--|---|------|
| TR[1:0] | 00 | -40°C to 15°C | Motor driver thermal range. Remark: TR[1:0] = 11 and TSD = 0 => Thermal Warning TR[1:0] = 11 and TSD = 1 => Thermal Shutdown TSD is located in Status Register 2 | p23 |
| | 01 | 15°C to 72°C | | |
| | 10 | 73°C to 150°C | | |
| | 11 | TSD = 0: 150°C to 170°C TSD = 1: >170°C | | |
| WD | 0 | No watchdog event | If WDEN = 1 and watchdog not acknowledged before the Watchdog Time-out (WDT[3:0]), WDb-pin will be pulled low for 100ms to reset an external microcontroller and WD bit will be set to ‘1’ to indicate this event. The external microcontroller can use this bit to verify a cold (WD = 0) or warm boot (WD = 1). | p24 |
| | 1 | Watchdog event occurred | | |

Status Register 1 (SR1)

Status Register 1 is located at address 0x05 and can only be read. Status Register 1 is a latched register. If an error occurs the bit will be set and can only be cleared by reading out this bit¹. The register is used to report an overcurrent or open coil in the X-coil, or to report a charge pump failure.

Notice that bit 7 is the parity bit (see READ operation p26).

Table 19. STATUS REGISTER 1

| Status Register 1 (SR1) | | | | | | | | | |
|-------------------------|--------|-------|--------|--------|--------|--------|--------|--------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x05 | Access | R | R | R | R | R | R | R | R |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | PAR | OVCXPT | OVCXPB | OVCXNT | OVCXNB | CPFAIL | OPEN_X | - |

1. In Sleep mode the register can be read out but will not be cleared!

Table 20. STATUS REGISTER 1 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-----------|-------|------------------------|--|------|
| OVCXPT | 0 | No overcurrent | Overcurrent detection in top transistor XP-terminal | p23 |
| | 1 | Overcurrent | | |
| OVCXPB | 0 | No overcurrent | Overcurrent detection in bottom transistor XP-terminal | p23 |
| | 1 | Overcurrent | | |
| OVCXNT | 0 | No overcurrent | Overcurrent detection in top transistor XN-terminal | p23 |
| | 1 | Overcurrent | | |
| OVCXNB | 0 | No overcurrent | Overcurrent detection in bottom transistor XN-terminal | p23 |
| | 1 | Overcurrent | | |
| CPFAIL | 0 | No charge pump failure | Charge pump failure detection | p23 |
| | 1 | Charge pump failure | | |
| OPEN_X | 0 | No open coil detected | Open coil detection for X-coil Note: a short circuit could trigger an open coil | p23 |
| | 1 | Open coil detected | | |

Status Register 2 (SR2)

Status Register 2 is located at address 0x06 and can only be read. Status Register 2 is a latched register. If an error occurs the bit will be set and can only be cleared by reading out this bit². The register is used to report an overcurrent or open coil in the Y-coil, or to report a thermal shutdown.

Notice that bit 7 is the parity bit (see READ operation p26).

Table 21. STATUS REGISTER 2

| Status Register 2 (SR2) | | | | | | | | | |
|-------------------------|--------|-------|--------|--------|--------|--------|-------|--------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x06 | Access | R | R | R | R | R | R | R | R |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | PAR | OVCYPT | OVCYPB | OVCYNT | OVCYNB | TSD | OPEN_Y | - |

Table 22. STATUS REGISTER 2 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-----------|-------|-----------------------|--|------|
| OVCYPT | 0 | No overcurrent | Overcurrent detection in top transistor YP-terminal | p23 |
| | 1 | Overcurrent | | |
| OVCYPB | 0 | No overcurrent | Overcurrent detection in bottom transistor YP-terminal | p23 |
| | 1 | Overcurrent | | |
| OVCYNT | 0 | No overcurrent | Overcurrent detection in top transistor YN-terminal | p23 |
| | 1 | Overcurrent | | |
| OVCYNB | 0 | No overcurrent | Overcurrent detection in bottom transistor YN-terminal | p23 |
| | 1 | Overcurrent | | |
| TSD | 0 | No thermal shutdown | Thermal Shutdown detection | p23 |
| | 1 | Thermal shutdown | | |
| OPEN_Y | 0 | No open coil detected | Open coil detection for X-coil Note: a short circuit could trigger an open coil | p23 |
| | 1 | Open coil detected | | |

2. In Sleep mode the register can be read out but will not be cleared!

Status Register 3 (SR3)

Status Register 3 is located at address 0x07 and can only be read. Status Register 3 contains the microstepping position and can be used to retrieve the position in the translator table (see Table 7). It is a non-latched register meaning that the microstepping position can be updated by the motor driver at any moment. Status Register 3 does not contain a parity bit.

Table 23. STATUS REGISTER 3

| Status Register 3 (SR3) | | | | | | | | | |
|-------------------------|--------|----------|-------|-------|-------|-------|-------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x07 | Access | R | R | R | R | R | R | R | R |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | MSP[7:0] | | | | | | | |

Table 24. STATUS REGISTER 3 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-----------|-----------|------------------------|--|------|
| MSP[7:0] | xxxx xxxx | Microstepping position | Indicates the position within the translator table | p19 |

Predriver Register 0 (PDRV0)

Predriver Register 0 is located at address 0x09 and can be used to set the current source for the gate charge of the external top MOSFET's during t_1 (see Figure 11).

Table 25. PREDRIVER REGISTER 0

| Predriver Register 0 (PDRV0) | | | | | | | | | |
|------------------------------|--------|---------------|-------|-------|-------|-------|---------------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x09 | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Data | TOP_I0N1[6:3] | | | | - | TOP_I0N1[2:0] | | |

Table 26. PREDRIVER REGISTER 0 PARAMETERS

| Parameter | Value | Value | Description | Info |
|---------------|-------|----------------------|--|------|
| TOP_I0N1[6:3] | xxxx | Current source value | Defines the current source for the external top MOSFET's during t_1 . Current source can be calculated as next: 1 mA + (PDRV0[7:4] x 2 mA) + 0.25 mA + (PDRV0[2:0] x 0.25 mA) | p13 |
| TOP_I0N1[2:0] | xxx | | | |

Predriver Register 1 (PDRV1)

Predriver Register 1 is located at address 0x0A and can be used to set the current source for the gate charge of the external top MOSFET's during t_2 (see Figure 11).

Table 27. PREDRIVER REGISTER 1

| Predriver Register 1 (PDRV1) | | | | | | | | | |
|------------------------------|--------|---------------|-------|-------|-------|-------|---------------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0A | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | Data | TOP_I0N2[6:3] | | | | - | TOP_I0N2[2:0] | | |

Table 28. PREDRIVER REGISTER 1 PARAMETERS

| Parameter | Value | Value | Description | Info |
|---------------|-------|----------------------|--|------|
| TOP_ION2[6:3] | xxxx | Current source value | Defines the current source for the external top MOSFET's during t_2 . Current source can be calculated as next: $1 \text{ mA} + (\text{PDRV1}[7:4] \times 2 \text{ mA}) + 0.25 \text{ mA} + (\text{PDRV1}[2:0] \times 0.25 \text{ mA})$ | p13 |
| TOP_ION2[2:0] | xxx | | | |

Predriver Register 2 (PDRV2)

Predriver Register 2 is located at address 0x0B and can be used to set the current source for the gate charge of the external bottom MOSFET's during t_1 (see Figure 11).

Table 29. PREDRIVER REGISTER 2

| Predriver Register 2 (PDRV2) | | | | | | | | | |
|------------------------------|--------|---------------|-------|-------|-------|-------|---------------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0B | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Data | BOT_ION1[6:3] | | | | - | BOT_ION1[2:0] | | |

Table 30. PREDRIVER REGISTER 2 PARAMETERS

| Parameter | Value | Value | Description | Info |
|---------------|-------|----------------------|---|------|
| BOT_ION1[6:3] | xxxx | Current source value | Defines the current source for the external bottom MOSFET's during t_1 . Current source can be calculated as next: $1 \text{ mA} + (\text{PDRV2}[7:4] \times 2 \text{ mA}) + 0.25 \text{ mA} + (\text{PDRV2}[2:0] \times 0.25 \text{ mA})$ | p13 |
| BOT_ION1[2:0] | xxx | | | |

Predriver Register 3 (PDRV3)

Predriver Register 3 is located at address 0x0C and can be used to set the current source for the gate charge of the external bottom MOSFET's during t_2 (see Figure 11).

Table 31. PREDRIVER REGISTER 3

| Predriver Register 3 (PDRV3) | | | | | | | | | |
|------------------------------|--------|---------------|-------|-------|-------|-------|---------------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0C | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | Data | BOT_ION2[6:3] | | | | - | BOT_ION2[2:0] | | |

Table 32. PREDRIVER REGISTER 3 PARAMETERS

| Parameter | Value | Value | Description | Info |
|---------------|-------|----------------------|---|------|
| BOT_ION2[6:3] | xxxx | Current source value | Defines the current source for the external bottom MOSFET's during t_2 . Current source can be calculated as next: $1 \text{ mA} + (\text{PDRV3}[7:4] \times 2 \text{ mA}) + 0.25 \text{ mA} + (\text{PDRV3}[2:0] \times 0.25 \text{ mA})$ | p13 |
| BOT_ION2[2:0] | xxx | | | |

Predriver Register 4 (PDRV4)

Predriver Register 4 is located at address 0x0D and can be used to set the current source for the gate discharge of the external MOSFET's (see Figure 11).

Table 33. PREDRIVER REGISTER 4

| Predriver Register 4 (PDRV4) | | | | | | | | | |
|------------------------------|--------|---------------|-------|-------|-------|---------------|-------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0D | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | Data | TOP_IOFF[3:0] | | | | BOT_IOFF[3:0] | | | |

Table 34. PREDRIVER REGISTER 4 PARAMETERS

| Parameter | Value | Value | Description | Info |
|---------------|-------|----------------------|---|------|
| TOP_IOFF[3:0] | xxxx | Current source value | Defines the current source for the external top MOSFET's during t_{off} . Current source can be calculated as next: 10.5 mA + (PDRV4[7:4] x 7 mA) | p13 |
| BOT_IOFF[3:0] | xxxx | Current source value | Defines the current source for the external bottom MOSFET's during t_{off} . Current source can be calculated as next: 10.5 mA + (PDRV4[3:0] x 7 mA) | p13 |

Predriver Register 5 (PDRV5)

Predriver Register 5 is located at address 0x0E and can be used to set t_2 (see Figure 11).

Table 35. PREDRIVER REGISTER 5

| Predriver Register 5 (PDRV5) | | | | | | | | | |
|------------------------------|--------|-------|-------------|-------|-------|-------|-------------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0E | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | Data | - | TOP_t2[2:0] | | | - | BOT_t2[2:0] | | |

Table 36. PREDRIVER REGISTER 5 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-------------|-------|--------------|---|------|
| TOP_t2[2:0] | 000 | 1.25 μ s | Defines the switch on duration t_2 for the external top MOSFET's. | p13 |
| | 001 | 1.75 μ s | | |
| | 010 | 2.25 μ s | | |
| | 011 | 2.75 μ s | | |
| | 100 | 3.25 μ s | | |
| | 101 | 3.75 μ s | | |
| | 110 | 4.25 μ s | | |
| | 111 | 4.75 μ s | | |

Table 36. PREDRIVER REGISTER 5 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-------------|-------|--------------|--|------|
| BOT_t2[2:0] | 000 | 1.25 μ s | Defines the switch on duration t_2 for the external bottom MOSFET's. | p13 |
| | 001 | 1.75 μ s | | |
| | 010 | 2.25 μ s | | |
| | 011 | 2.75 μ s | | |
| | 100 | 3.25 μ s | | |
| | 101 | 3.75 μ s | | |
| | 110 | 4.25 μ s | | |
| | 111 | 4.75 μ s | | |

Predriver Register 6 (PDRV6)

Predriver Register 6 is located at address 0x0F and can be used to set t_{off} (see Figure 11).

Table 37. PREDRIVER REGISTER 6

| Predriver Register 6 (PDRV6) | | | | | | | | | |
|------------------------------|--------|-------|---------------|-------|-------|-------|---------------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0F | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | Data | - | TOP_toff[2:0] | | | - | BOT_toff[2:0] | | |

Table 38. PREDRIVER REGISTER 6 PARAMETERS

| Parameter | Value | Value | Description | Info |
|---------------|-------|--------------|---|------|
| TOP_toff[2:0] | 000 | 1.25 μ s | Defines the switch off duration (t_{off}) for the external top MOSFET's. | p13 |
| | 001 | 1.75 μ s | | |
| | 010 | 2.25 μ s | | |
| | 011 | 2.75 μ s | | |
| | 100 | 3.25 μ s | | |
| | 101 | 3.75 μ s | | |
| | 110 | 4.25 μ s | | |
| | 111 | 4.75 μ s | | |
| BOT_toff[2:0] | 000 | 1.25 μ s | Defines the switch off duration (t_{off}) for the external bottom MOSFET's. | p13 |
| | 001 | 1.75 μ s | | |
| | 010 | 2.25 μ s | | |
| | 011 | 2.75 μ s | | |
| | 100 | 3.25 μ s | | |
| | 101 | 3.75 μ s | | |
| | 110 | 4.25 μ s | | |
| | 111 | 4.75 μ s | | |

Predriver Register 7 (PDRV7)

Predriver Register 7 is located at address 0x10 and can be used to set t_1 (see Figure 11).

Table 39. PREDRIVER REGISTER 7

| Predriver Register 7 (PDRV7) | | | | | | | | | |
|------------------------------|--------|-------|-------------|-------|-------|-------|-------------|-------|-------|
| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x10 | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| | Data | - | TOP_t1[2:0] | | | - | BOT_t1[2:0] | | |

Table 40. PREDRIVER REGISTER 7 PARAMETERS

| Parameter | Value | Value | Description | Info |
|-------------|-------|---------|--|------|
| TOP_t1[2:0] | 000 | 375 ns | Defines the switch on duration t_1 for the external top MOSFET's. | p13 |
| | 001 | 500 ns | | |
| | 010 | 625 ns | | |
| | 011 | 750 ns | | |
| | 100 | 875 ns | | |
| | 101 | 1000 ns | | |
| | 110 | 1125 ns | | |
| | 111 | 1250 ns | | |
| BOT_t1[2:0] | 000 | 375 ns | Defines the switch on duration t_1 for the external bottom MOSFET's. | p13 |
| | 001 | 500 ns | | |
| | 010 | 625 ns | | |
| | 011 | 750 ns | | |
| | 100 | 875 ns | | |
| | 101 | 1000 ns | | |
| | 110 | 1125 ns | | |
| | 111 | 1250 ns | | |

PACKAGE THERMAL CHARACTERISTICS

The AMIS-30421 is available in a NQFP44 package. For cooling optimizations, the NQFP has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer.

Figure 35 gives an example of good heat transfer. The exposed thermal pad is soldered directly on the top ground layer (left picture of Figure 35). It's advised to make the top ground layer as large as possible (see arrows Figure 35). To improve the heat transfer even more, the exposed thermal pad is connected to a bottom ground layer by using thermal vias (see right picture of Figure 35). It's advised to make this bottom ground layer as large as possible and with as less as possible interruptions.

For precise thermal cooling calculations the major thermal resistances of the device are given (Table 4). The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)
- PCB board copper area (via the exposed pad)

The major thermal resistances of the device are the R_{th} from the junction to the ambient (R_{thja}) and the overall R_{th} from the junction to exposed pad (R_{thjp}). In Table 4 one can find the values for the R_{thja} and R_{thjp} , simulated according to JESD-51.

The R_{thja} for 2S2P is simulated conform JEDEC JESD-51 as follows:

- A 4-layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
- Board thickness is 1,46mm (FR4 PCB material)
- The 2 signal layers: 70 μ m thick copper with an area of 5500 mm^2 copper and 20% conductivity
- The 2 power internal planes: 36 μ m thick copper with an area of 5500 mm^2 copper and 90% conductivity

The R_{thja} for 1S0P is simulated conform to JEDEC JESD-51 as follows:

- A 1-layer printed circuit board with only 1 layer
- Board thickness is 1.46 mm (FR4 PCB material)
- The layer has a thickness of 70 μ m copper with an area of 5500 mm^2 copper and 20% conductivity

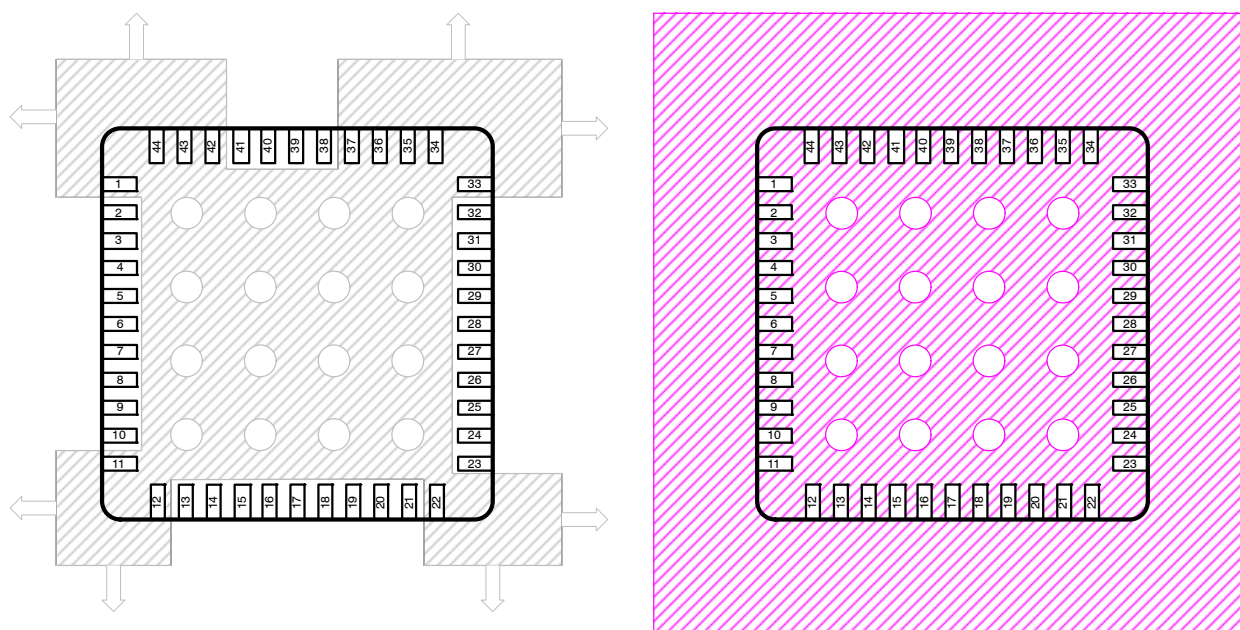


Figure 35. PCB Ground Plane Layout Condition (left picture displays the top ground layer, right picture displays the bottom ground layer)

ORDERING INFORMATION

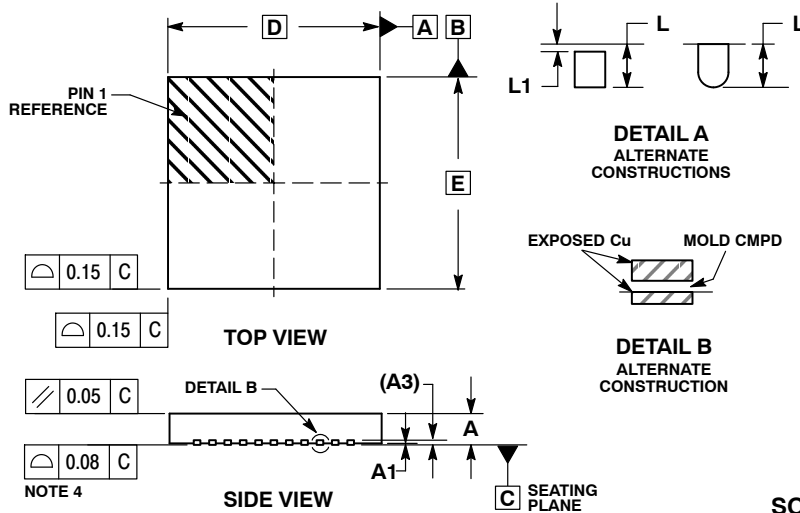
| Part No. | Peak Current | Temperature Range | Package | Shipping [†] |
|------------------|--------------|-------------------|---------------------------------|-----------------------|
| AMIS30421C4211G | NA | -40°C to +170°C | NQFP-44 (7 x 7 mm) (Pb-Free) | Units / Tube |
| AMIS30421C4211RG | | | | Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

AMIS-30421

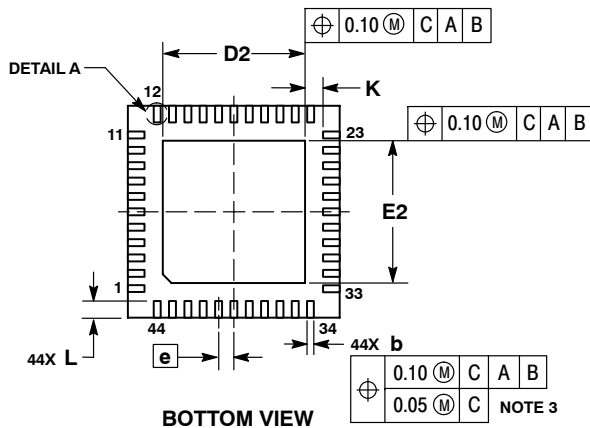
PACKAGE DIMENSIONS

QFN44 7x7, 0.5P
CASE 485BY
ISSUE O

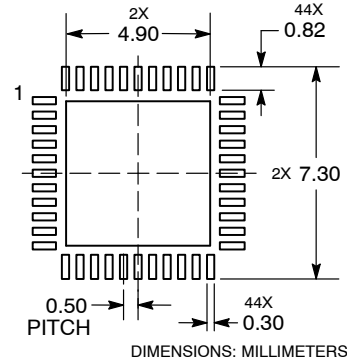


- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.80 | 0.90 |
| A1 | --- | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 7.00 | BSC |
| D2 | 4.60 | 4.80 |
| E | 7.00 | BSC |
| E2 | 4.60 | 4.80 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.45 | 0.65 |
| L1 | --- | 0.15 |



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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