

# SPICE Device Model Si4848DY

## **Vishay Siliconix**

## N-Channel 150-V (D-S) MOSFET

#### **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

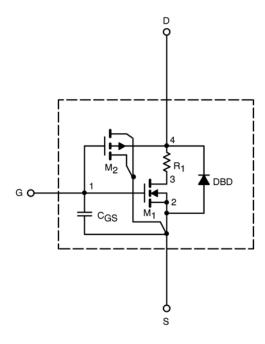
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### **DESCRIPTION**

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to  $125^{\circ}$ C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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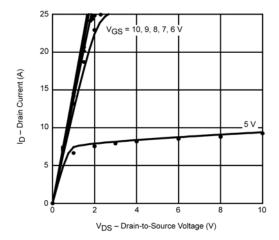
SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	2.8		V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS}$ = $\geq$ 5 V, $V_{GS}$ = 10 V	76		Α
Drain-Source On-State Resistance <sup>a</sup>	_	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A	0.0065	0.068	Ω
	r <sub>DS(on)</sub>	$V_{GS}$ = 6 V, $I_{D}$ = 3.0 A	0.0078	0.076	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_{D} = 5 \text{ A}$	12	15	S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.5 \text{ A}, V_{GS} = 0 \text{ V}$	0.76	0.75	V
Dynamic <sup>b</sup>	•		·		<del>-</del>
Total Gate Charge	$Q_g$	$V_{DS}$ = 75 V, $V_{GS}$ = 10 V, $I_{D}$ = 3.5 A	18	17	nC
Gate-Source Charge	$Q_{gs}$		3.2	32	
Gate-Drain Charge	$Q_{gd}$		6	6	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD}$ = 75 V, $R_L$ = 21 $\Omega$ $I_D \cong 3.5 \text{ A}, V_{GEN}$ = 10 V, $R_G$ = 6 $\Omega$ $I_F$ = 2.5 A, di/dt = 100 A/ $\mu$ s	12	9	ns
Rise Time	t <sub>r</sub>		16	10	
Turn-Off Delay Time	t <sub>d(off)</sub>		19	24	
Fall Time	t <sub>f</sub>		23	17	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		52	45	

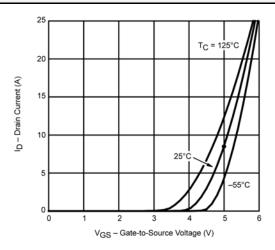
a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2%. b. Guaranteed by design, not subject to production testing.

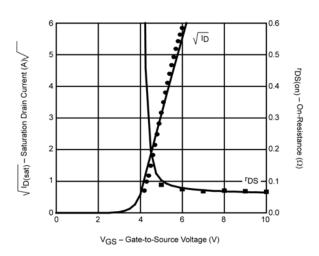


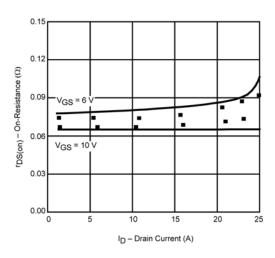
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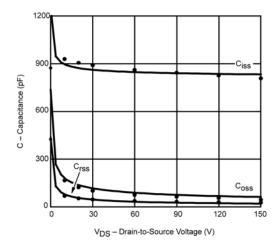
#### COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

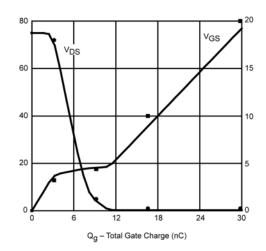












Note: Dots and squares represent measured data.



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