

RJM0404JSC

Silicon N/P Channel Power MOS FET (6 in 1 Type)
High Speed Power Switching

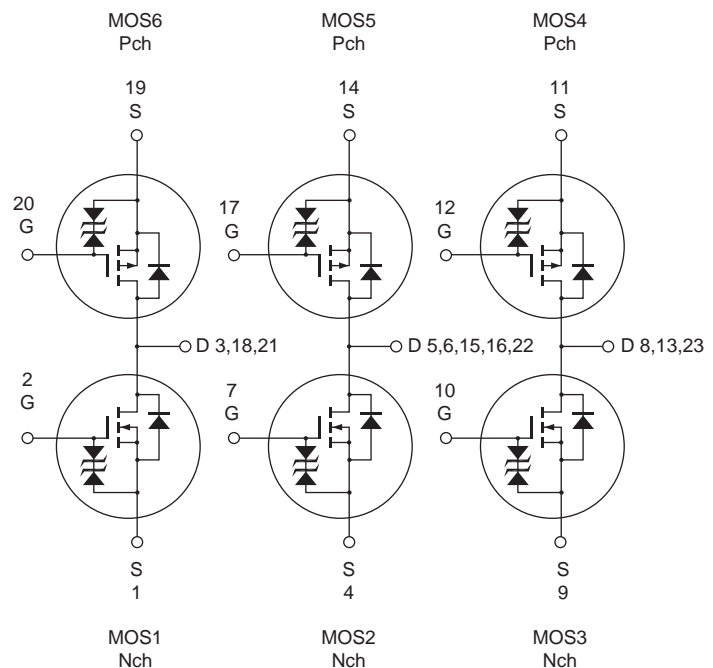
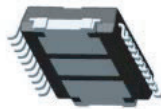
R07DS0338EJ0500
Rev.5.00
May 11, 2011

Features

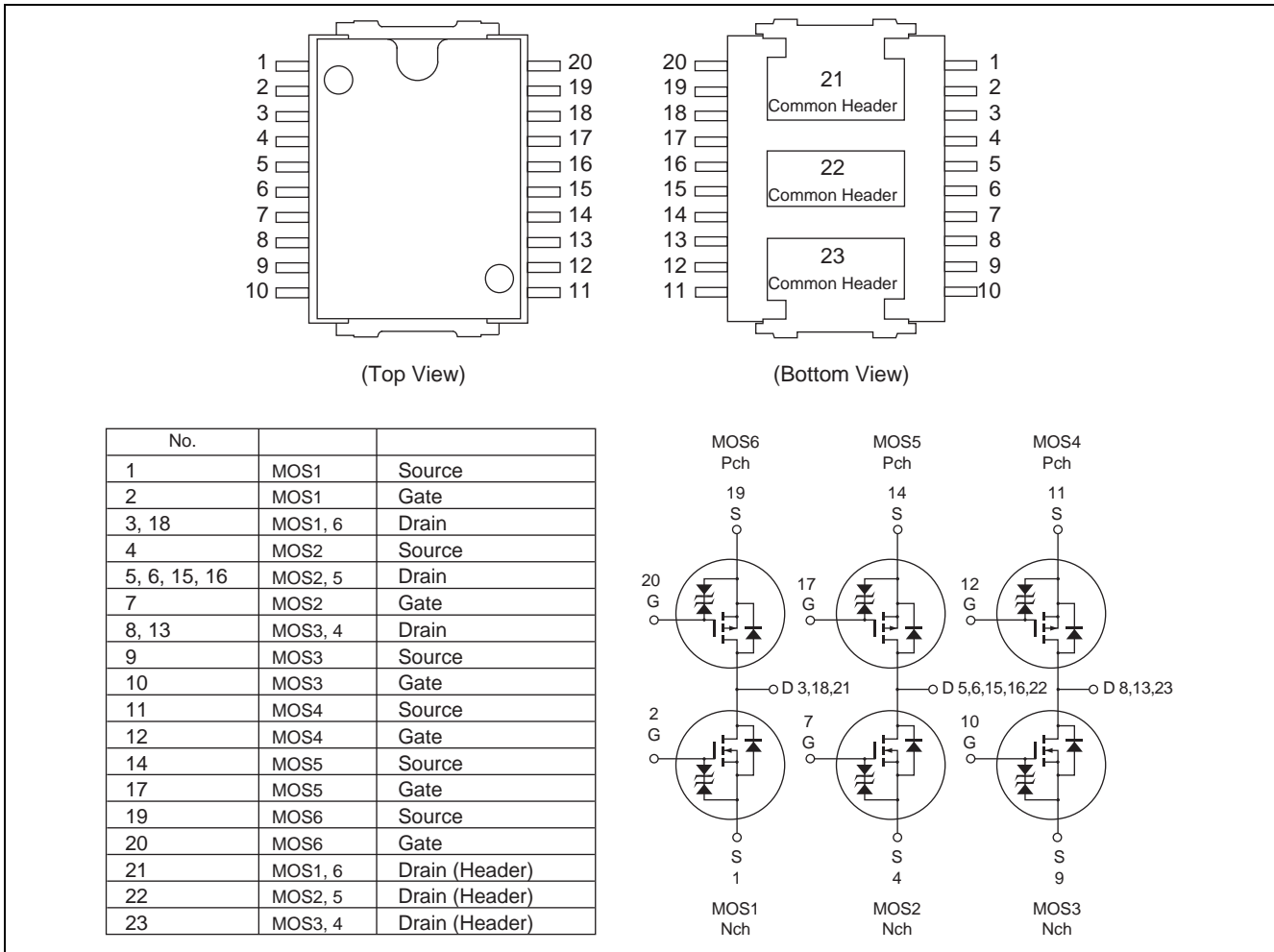
- For Automotive applications
- AEC-Q101 compliant
- N/P Channel MOS FET (6 in 1 Type). High density mounting
- Low on-resistance
- Capable of 4.5 V gate drive

Outline

RENESAS Package Code: PRSP0020DF-A
(Package Name: HSOP-20)



Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		MOS1, 2, 3 (Nch)	MOS4, 5, 6 (Pch)	
Drain to source voltage	V _{DSS}	40	-40	V
Gate to source voltage	V _{GSS}	+20 / -5	-20 / +5	V
Drain current	I _D	20	-20	A
Drain peak current	I _D (pulse) ^{Note1}	80	-80	A
Avalanche current	I _{AP} ^{Note3}	20	-20	A
Avalanche energy	E _{AR} ^{Note3}	53	53	mJ
Channel dissipation	P _{ch} ^{Note2}	54	54	W
Channel temperature	T _{ch} ^{Note4}	175	175	°C
Storage temperature	T _{stg}	-55 to +150	-55 to +150	°C

- Notes: 1. PW ≤ 10μs duty cycle ≤ 1%
 2. Tc = 25°C : 1 Drive Operation.
 3. Tch = 25°C, Rg ≥ 50 Ω
 4. AEC-Q101 compliant

Thermal Impedance Characteristics

- Channel to case thermal impedance θ_{ch-c}: 2.78°C/W

Electrical Characteristics

• MOS1, MOS2, MOS3 (N Channel)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 40 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = +20 / -5 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	1.0	—	2.5	V	V _{DS} = 10 V, I _D = 1 mA
Static drain to source on state resistance	R _{DS(on)}	—	17	21	mΩ	I _D = 10 A, V _{GS} = 10 V ^{Note5}
		—	24	34	mΩ	I _D = 10 A, V _{GS} = 4.5 V ^{Note5}
Input capacitance	C _{iss}	—	1400	—	pF	V _{DS} = 10V, V _{GS} = 0, f = 1 MHz
Output capacitance	C _{oss}	—	230	—	pF	
Reverse transfer capacitance	C _{rss}	—	100	—	pF	
Total gate charge	Q _g	—	23	—	nC	V _{DD} = 25 V, V _{GS} = 10 V, I _D = 20 A
Gate to source charge	Q _{gs}	—	3	—	nC	
Gate to drain charge	Q _{gd}	—	4	—	nC	
Turn-on delay time	t _{d(on)}	—	15	—	ns	V _{GS} = 10 V, I _D = 10 A, V _{DD} ≅ 20 V, R _L = 2 Ω, R _G = 4.7 Ω
Rise time	t _r	—	35	—	ns	
Turn-off delay time	t _{d(off)}	—	50	—	ns	
Fall time	t _f	—	8	—	ns	
Body-drain diode forward voltage	V _{DF}	—	0.92	1.2	V	I _F = 20 A, V _{GS} = 0 ^{Note5}
Body-drain diode reverse recovery time	t _{rr}	—	20	—	ns	I _F = 20 A, V _{GS} = 0 di _F /dt = 50 A/μs

Note: 5. Pulse test

• MOS4, MOS5, MOS6 (P Channel)

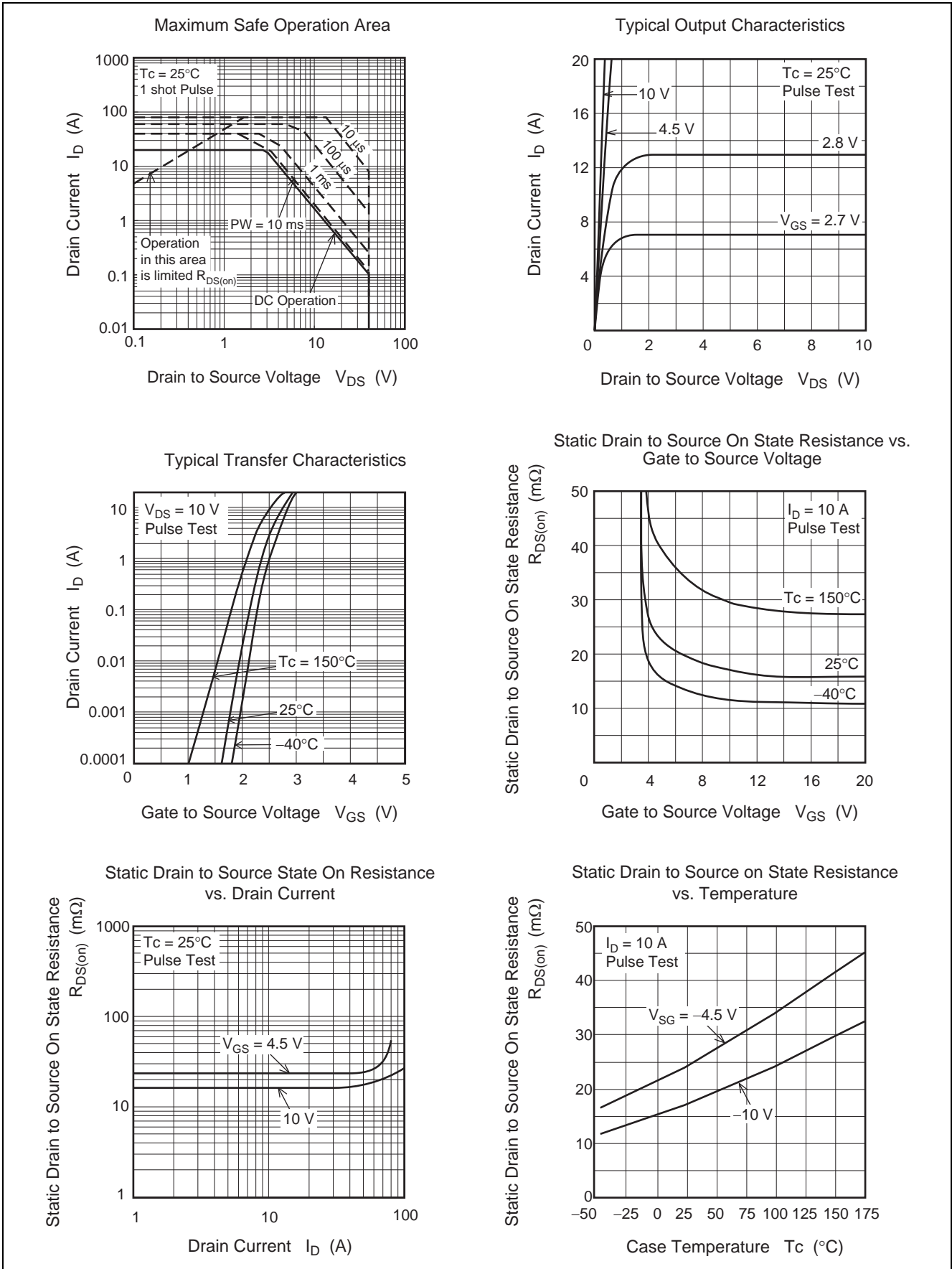
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -40 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = -20 / +5 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS(off)}	-1.0	—	-2.5	V	V _{DS} = -10 V, I _D = -1 mA
Static drain to source on state resistance	R _{DS(on)}	—	34	42	mΩ	I _D = -10 A, V _{GS} = -10 V ^{Note6}
		—	48	68	mΩ	I _D = -10 A, V _{GS} = -4.5 V ^{Note6}
Input capacitance	C _{iss}	—	1500	—	pF	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz
Output capacitance	C _{oss}	—	230	—	pF	
Reverse transfer capacitance	C _{rss}	—	140	—	pF	
Total gate charge	Q _g	—	25	—	nC	V _{DD} = -25 V, V _{GS} = -10 V, I _D = -20 A
Gate to source charge	Q _{gs}	—	5	—	nC	
Gate to drain charge	Q _{gd}	—	4	—	nC	
Turn-on delay time	t _{d(on)}	—	30	—	ns	V _{GS} = -10 V, I _D = -10 A, V _{DD} ≅ -20 V, R _L = 2 Ω, R _G = 4.7 Ω
Rise time	t _r	—	55	—	ns	
Turn-off delay time	t _{d(off)}	—	50	—	ns	
Fall time	t _f	—	20	—	ns	
Body-drain diode forward voltage	V _{DF}	—	-0.97	-1.26	V	I _F = -20 A, V _{GS} = 0 ^{Note6}
Body-drain diode reverse recovery time	t _{rr}	—	30	—	ns	I _F = -20 A, V _{GS} = 0 di _F /dt = 50 A/μs

Note: 6. Pulse test

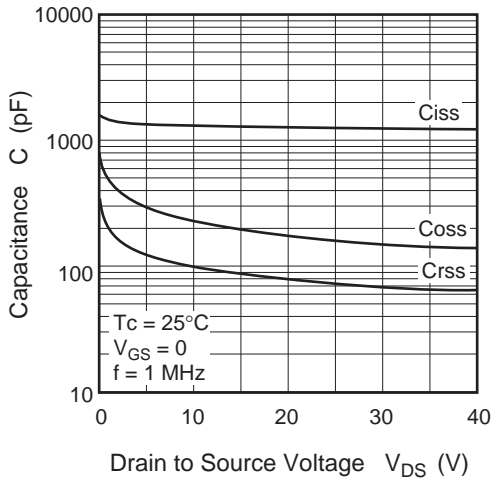
Main Characteristics

- MOS1, 2, 3 (Nch)

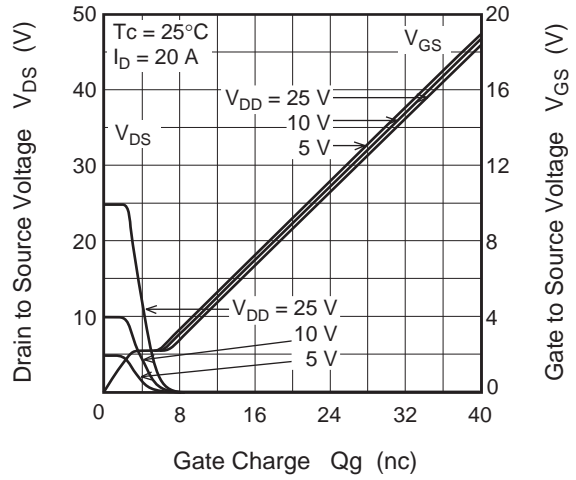


• MOS1, 2, 3(Nch)

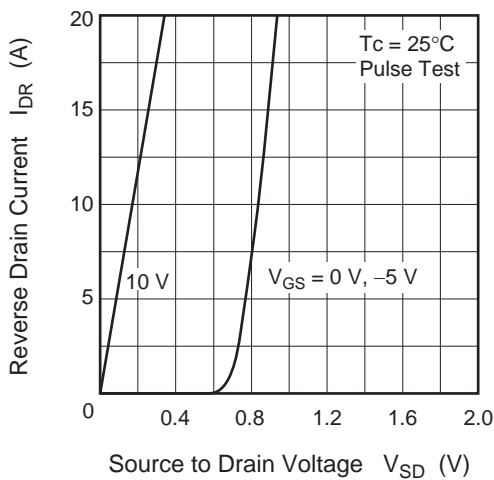
Typical Capacitance vs. Drain to Source Voltage



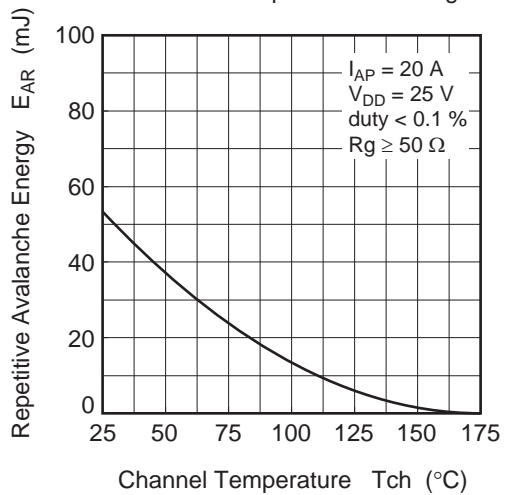
Dynamic Input Characteristics



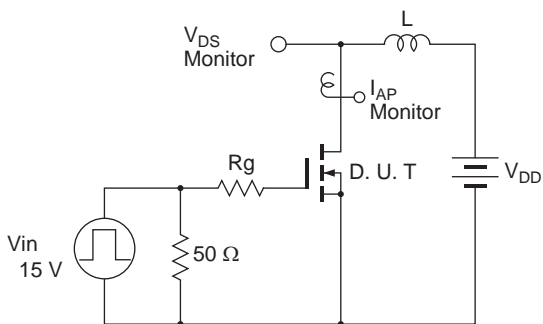
Reverse Drain Current vs. Source to Drain Voltage



Avalanche Energy vs. Channel Temperature Derating

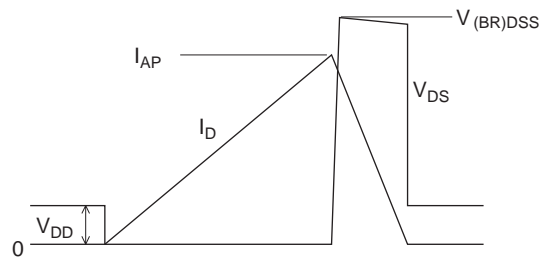


Avalanche Test Circuit

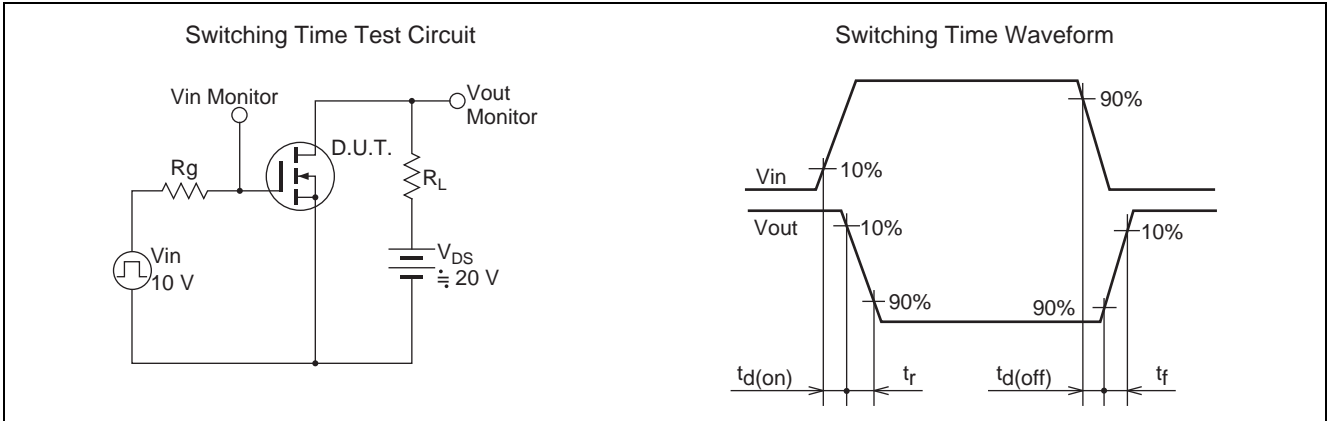


Avalanche Waveform

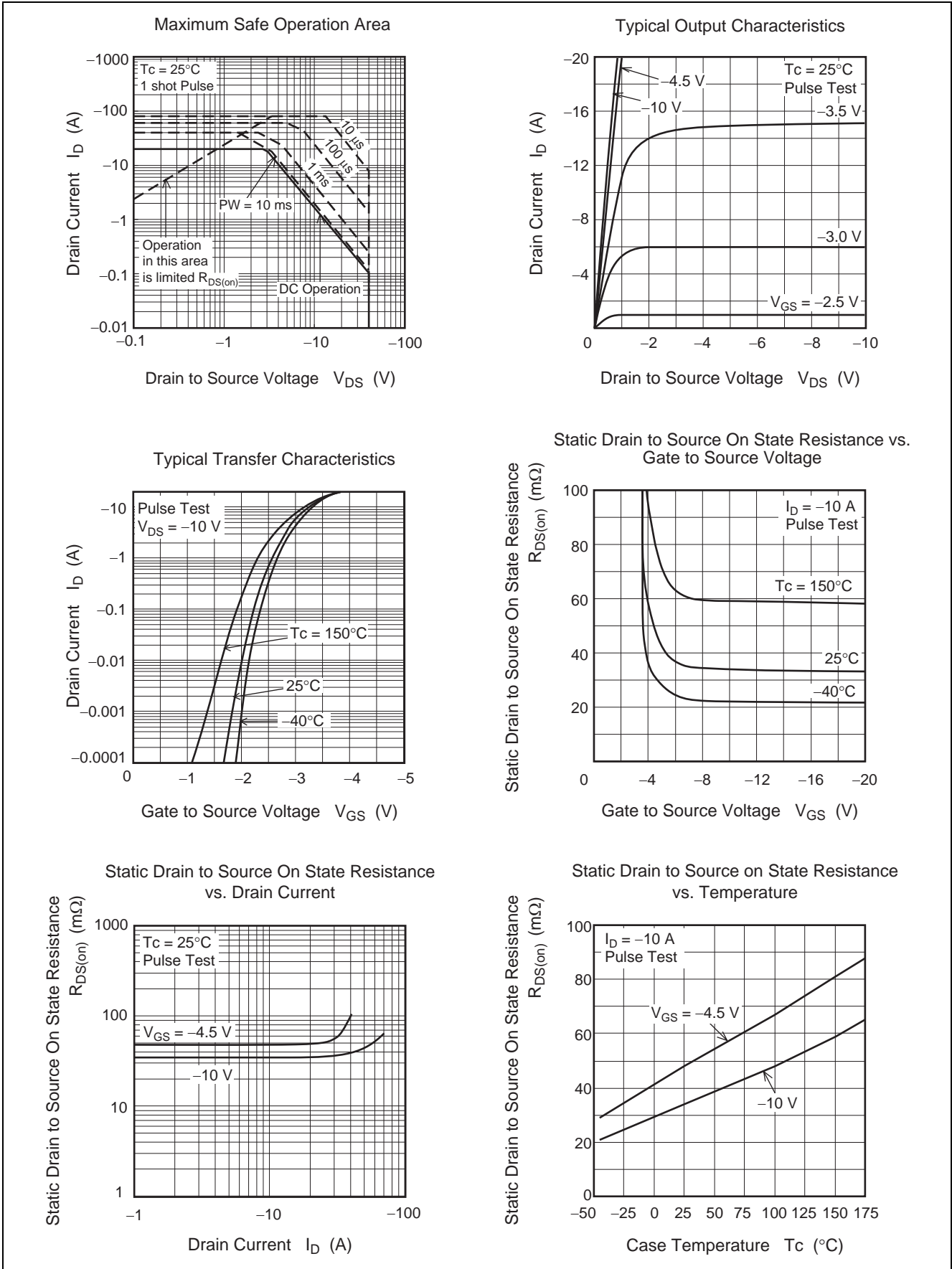
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



• MOS1, 2, 3 (Nch)

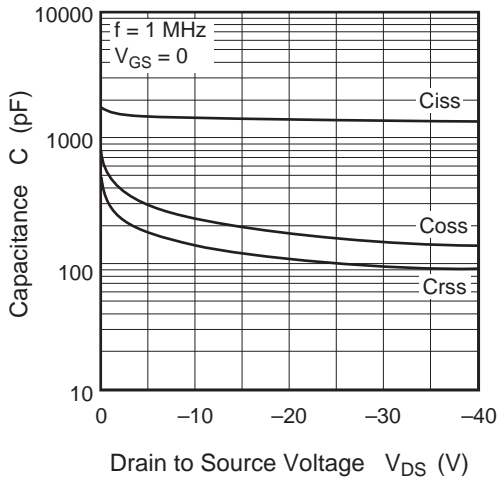


• MOS4, 5, 6 (Pch)

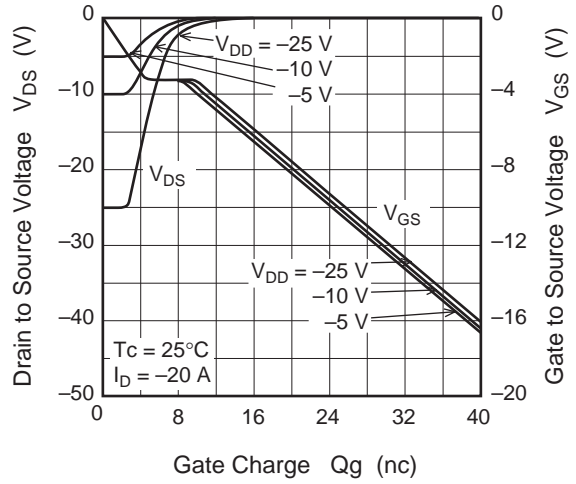


• MOS4, 5, 6 (Pch)

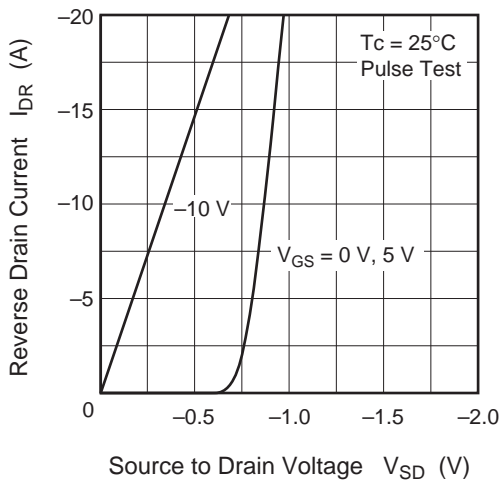
Typical Capacitance vs. Drain to Source Voltage



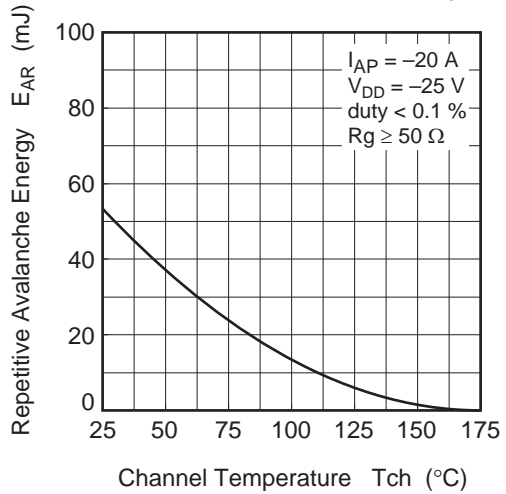
Dynamic Input Characteristics



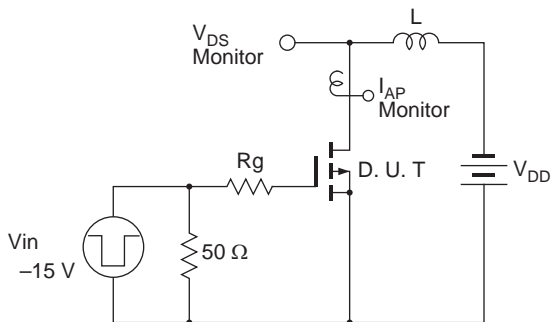
Reverse Drain Current vs. Source to Drain Voltage



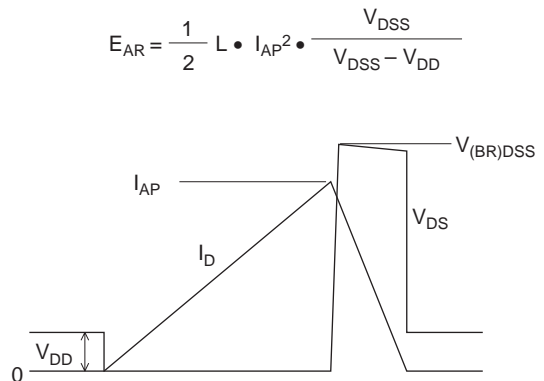
Avalanche Energy vs. Channel Temperature Derating



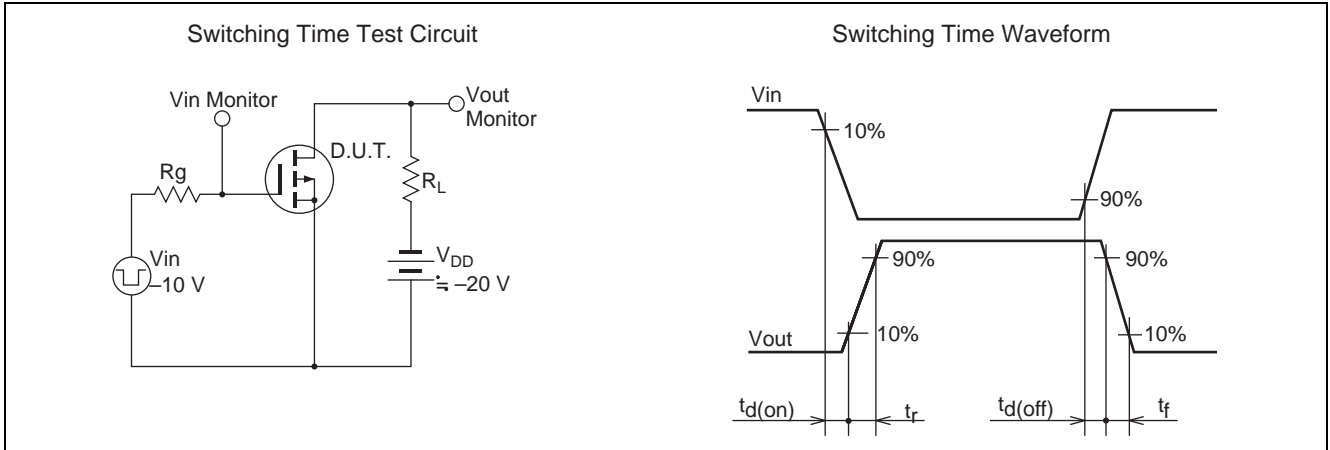
Avalanche Test Circuit



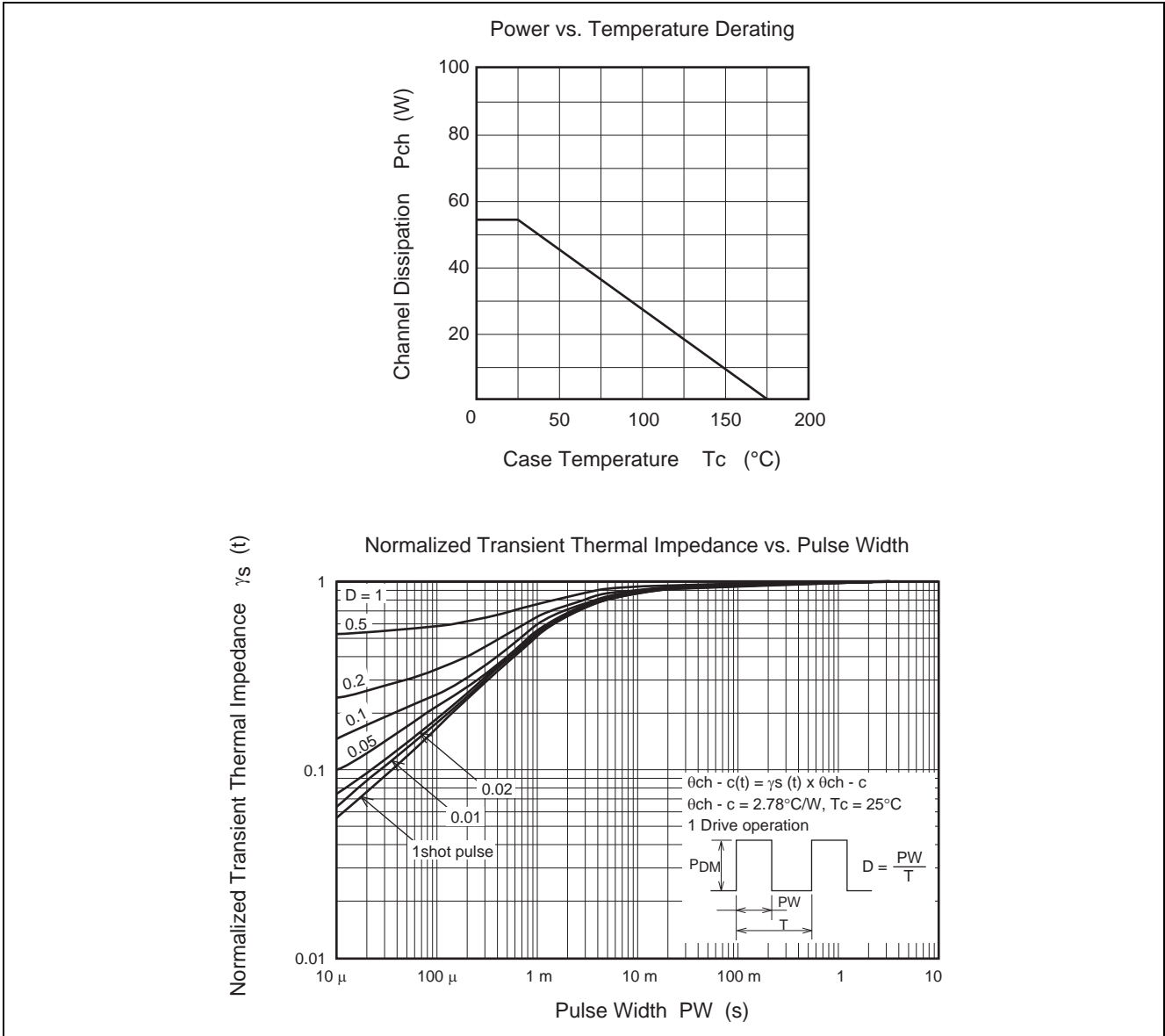
Avalanche Waveform



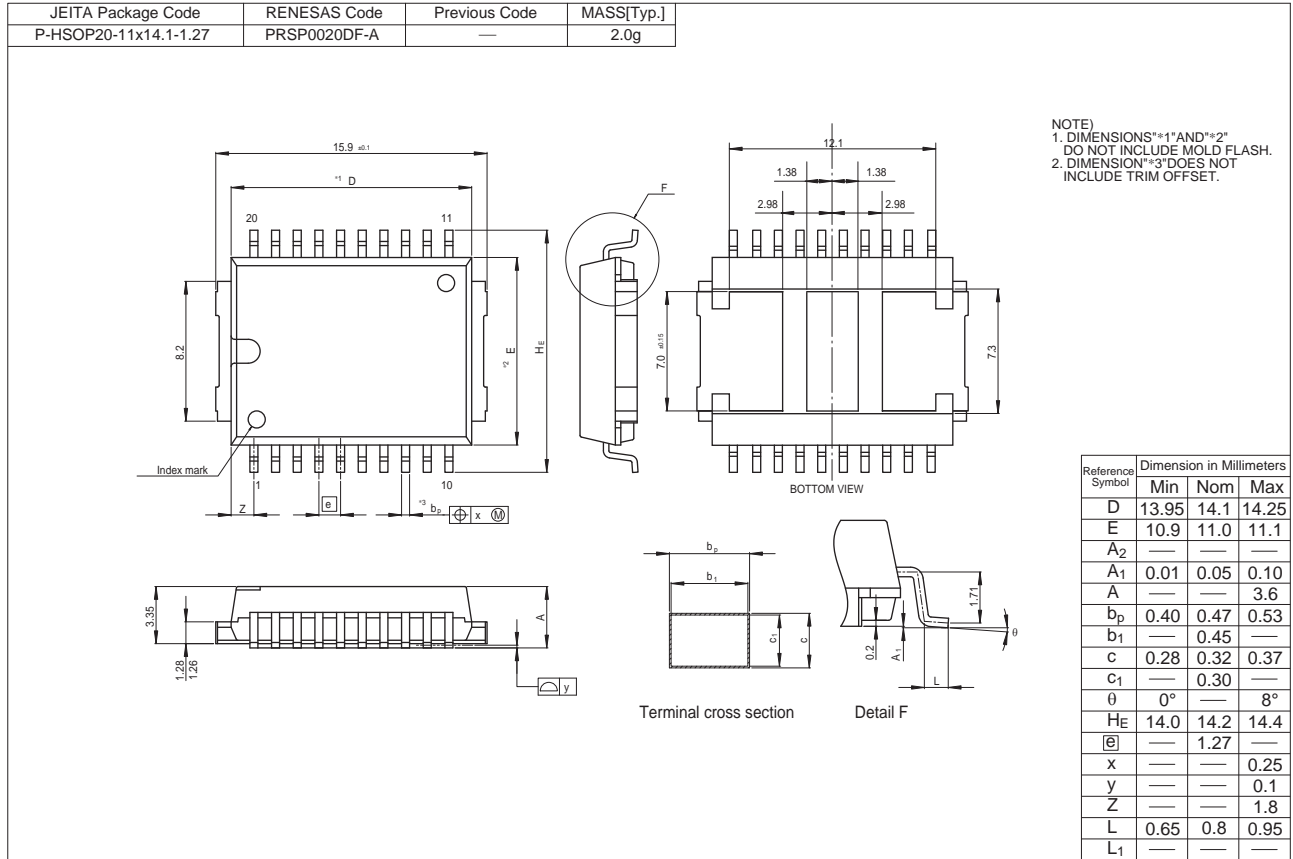
• MOS4, 5, 6 (Pch)



• Common



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJM0404JSC-00-12	700 pcs	Tray

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