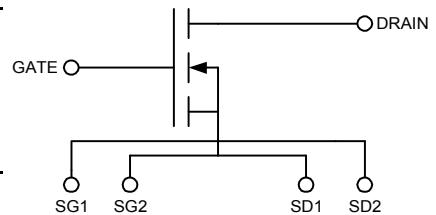


N-Channel Enhancement Mode
 Low Q_g and R_g
 High dv/dt
 Nanosecond Switching
 Ideal for Class C, D, & E Applications

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	1000	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	1000	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_c = 25^\circ\text{C}$	10	A
I_{DM}	$T_c = 25^\circ\text{C}$, pulse width limited by T_{JM}	60	A
I_{AR}	$T_c = 25^\circ\text{C}$	10	A
E_{AR}	$T_c = 25^\circ\text{C}$	30	mJ
dv/dt	$I_S \leq I_{DM}$, $dv/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_j \leq 150^\circ\text{C}$, $R_G = 0.2\Omega$	5	V/ns
	$I_S = 0$	>200	V/ns
P_{DC}		940	W
P_{DHS}	$T_c = 25^\circ\text{C}$ Derate $4.4\text{W}/^\circ\text{C}$ above 25°C	425	W
P_{DAMB}	$T_c = 25^\circ\text{C}$	4.5	W
R_{thJC}		0.16	C/W
R_{thJHS}		0.23	C/W

Symbol	Test Conditions	Characteristic Values		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 3 \text{ mA}$	1000		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.5	3.1	5.5 V
I_{GSS}	$V_{GS} = \pm 20 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 100 \text{ nA}$
I_{DSS}	$V_{DS} = 0.8 V_{DSS}$ $T_J = 25^\circ\text{C}$ $V_{GS} = 0$ $T_J = 125^\circ\text{C}$			$50 \mu\text{A}$ 1 mA
$R_{DS(on)}$	$V_{GS} = 15 \text{ V}$, $I_D = 0.5I_{D25}$ Pulse test, $t \leq 300\mu\text{s}$, duty cycle $d \leq 2\%$			1.2 Ω
g_{fs}	$V_{DS} = 20 \text{ V}$, $I_D = 0.5I_{D25}$, pulse test	4	6	S
T_J		-55		+150 $^\circ\text{C}$
T_{JM}			150	$^\circ\text{C}$
T_{stg}		-55		+150 $^\circ\text{C}$
T_L	1.6mm (0.063 in) from case for 10 s	300		$^\circ\text{C}$
Weight		3		g

$$\begin{aligned} V_{DSS} &= 1000 \text{ V} \\ I_{D25} &= 10 \text{ A} \\ R_{DS(on)} &\leq 1.2 \Omega \\ P_{DC} &= 940 \text{ W} \end{aligned}$$



Features

- Isolated Substrate
 - high isolation voltage (>2500V)
 - excellent thermal transfer
 - Increased temperature and power cycling capability
- IXYS advanced low Q_g process
- Low gate charge and capacitances
 - easier to drive
 - faster switching
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

Advantages

- Optimized for RF and high speed switching at frequencies to 50MHz
- Easy to mount—no insulators needed
- High power density



DE375-102N10A
RF Power MOSFET

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C unless otherwise specified)		
R _G		0.3		Ω
C _{iss}		2750		pF
C _{oss}	V _{GS} = 0 V, V _{DS} = 0.8 V _{DSS(max)} , f = 1 MHz	110		pF
C _{rss}		20		pF
C _{stray}	Back Metal to any Pin	33		pF
T _{d(on)}		5		ns
T _{on}	V _{GS} = 15 V, V _{DS} = 0.8 V _{DSS} I _D = 0.5 I _{DM}	3		ns
T _{d(off)}	R _G = 0.2 Ω (External)	5		ns
T _{off}		8		ns
Q _{g(on)}		81		nC
Q _{gs}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} I _D = 0.5 I _{D25}	16		nC
Q _{gd}		42		nC

Source-Drain Diode

Characteristic Values

(T_J = 25°C unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.
I _S	V _{GS} = 0 V			10 A
I _{SM}	Repetitive; pulse width limited by T _{JM}			80 A
V _{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle ≤ 2%			1.5 V
T _{rr}		200		ns
Q _{RM}	I _F = I _S , -di/dt = 100A/μs, V _R = 100V	0.6		μC
I _{RM}		7		A

For detailed device mounting and installation instructions, see the "Device Installation & Mounting Instructions" technical note on the IXYSRF web site at;

http://www.ixysrf.com/pdf/switch_mode/appnotes/7de_series_mosfet_installation_instructions.pdf

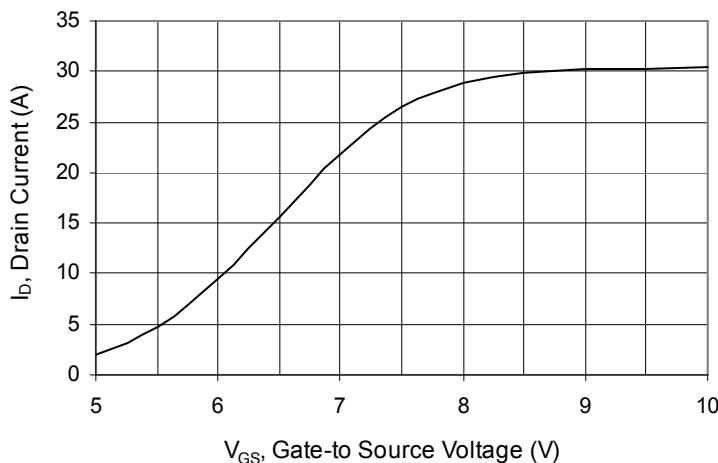
IXYS RF reserves the right to change limits, test conditions and dimensions.

IXYS RF MOSFETS are covered by one or more of the following U.S. patents:

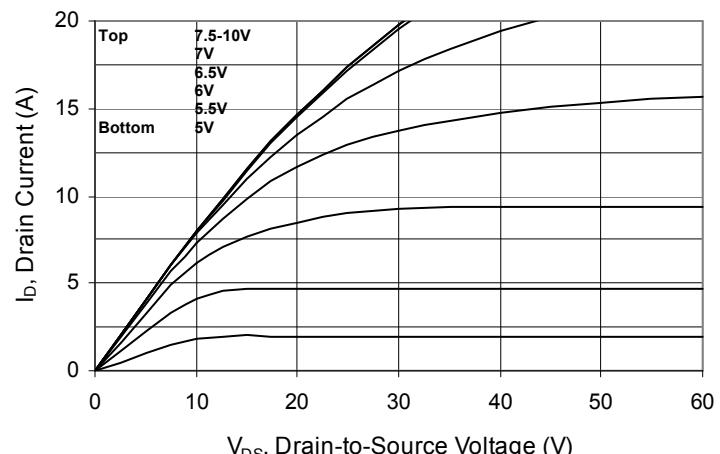
4,835,592	4,860,072	4,881,106	4,891,686	4,931,844	5,017,508
5,034,796	5,049,961	5,063,307	5,187,117	5,237,481	5,486,715
5,381,025	5,640,045				

Fig. 1

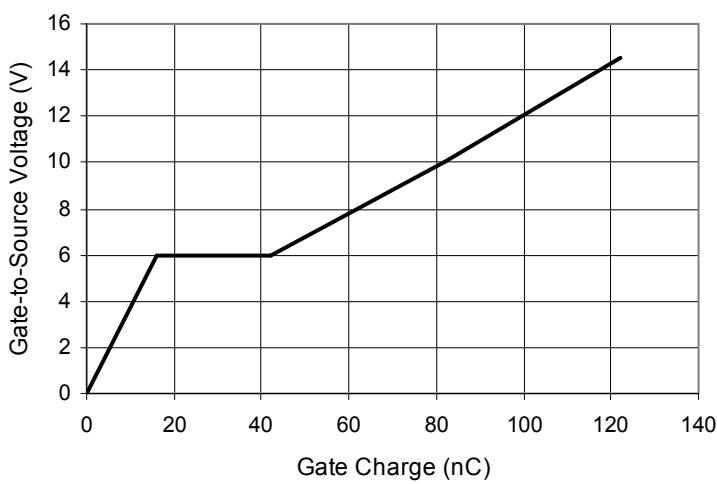
Typical Transfer Characteristics
 $V_{DS} = 60V$, $PW = 4\mu s$


Fig. 2

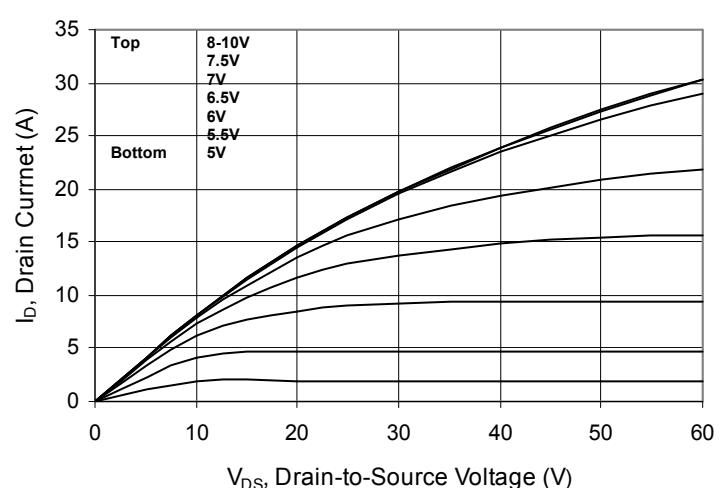
Typical Output Characteristics


Fig. 3

Gate Charge vs. Gate-to-Source Voltage
 $V_{DS} = 500V$, $I_D = 5A$


Fig. 4

Extended Typical Output Characteristics


Fig. 5

V_{DS} vs. Capacitance

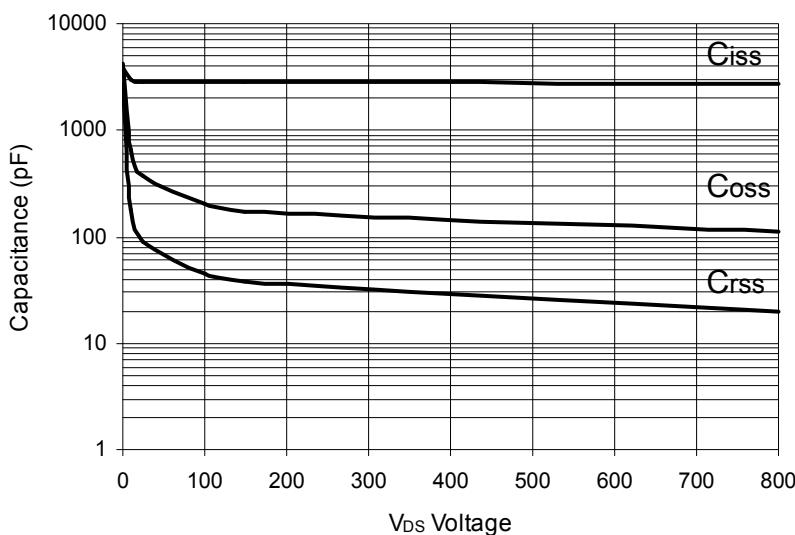
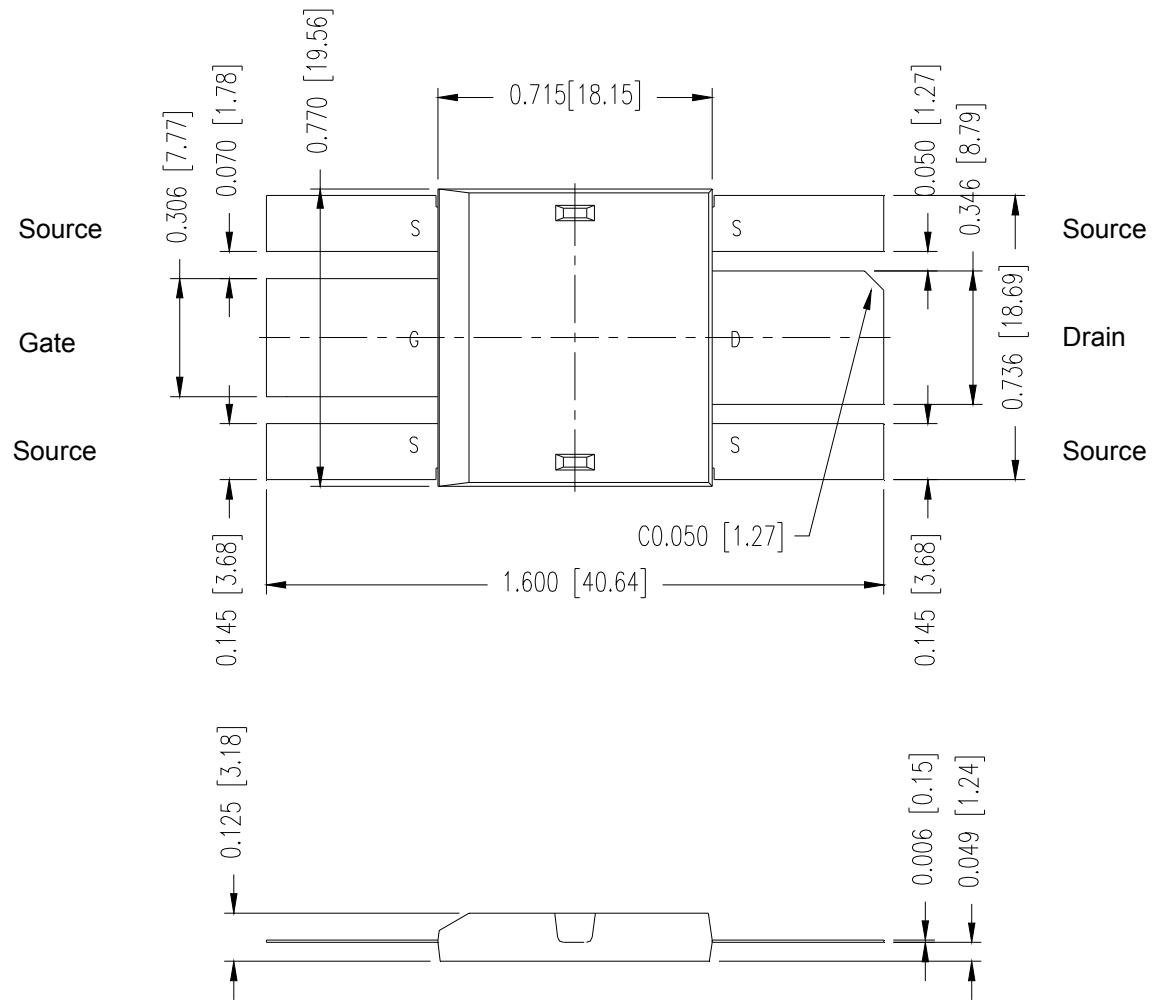


Fig. 6 Package Drawing


DE375-0001 DE-SERIES SPICE Model

The DE-SERIES SPICE Model is illustrated in Figure 7. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms L_G , L_S and L_D . R_d is the $R_{DS(ON)}$ of the device, R_{ds} is the resistive leakage term. The output capacitance, C_{OSS} , and reverse transfer capacitance, C_{RSS} are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via R_{on} and R_{off} .

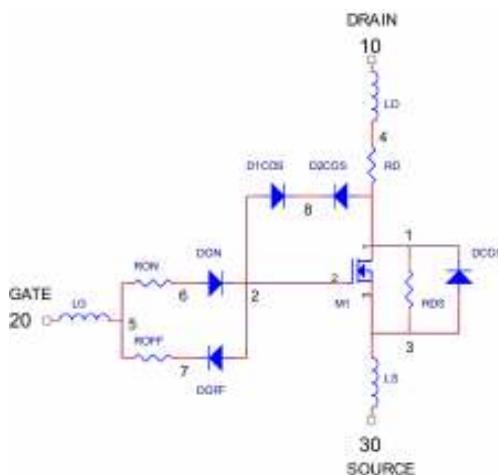


Figure 7 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the IXYSRF web site at www.ixysrf.com/spice.htm

Net List:

```

.SUBCKT 102N10A 10 20 30
* TERMINALS: D G S
* 1000 Volt 10 Amp 1.2 ohm N-Channel Power MOSFET
* REV.A 05-23-00
M1 1 2 3 3 DMOS L=1U W=1U
RON 5 6 0.5
DON 6 2 D1
ROF 5 7 .1
DOF 2 7 D1
D1CRS 2 8 D2
D2CRS 1 8 D2
CGS 2 3 3.0N
RD 4 1 1.5
DCOS 3 1 D3
RDS 1 3 5.0MEG
LS 3 30 .5N
LD 10 4 1N
LG 20 5 1N
.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=3.8)
.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)
.MODEL D2 D (IS=.5F CJO=400P BV=1000 M=.4 VJ=.6 TT=400N RS=10M)
.MODEL D3 D (IS=.5F CJO=900P BV=1000 M=.3 VJ=.4 TT=400N RS=10M)
.ENDS

```

Doc #9200-0223-0001 Rev 2
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