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Status	Product Specification
FAST Products	

# FAST 74F604

## Latch

### Dual Octal Latch (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F604	7.5ns	75mA

### FEATURES

- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs
- 3-State outputs
- Power supply current 75mA typical

### DESCRIPTION

The 74F604 multiplexed latch is ideal for storing data from two input buses, A or B, and providing data from either the A or B latches to the output bus. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/B) input determines whether the A or B latch contents are multiplexed to the eight 3-State outputs. Data entered from the B inputs are selected when SELECT A/B is Low; data from the A inputs are selected when SELECT A/B is High. Data enters

### ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
28-Pin Plastic DIP	N74F604N
28-Pin Plastic SOL	N74F604D

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0$ - $A_7$ , $B_0$ - $B_7$	Data inputs	1.0/0.033	20µA/20µA
SELECT A/B	Select input	1.0/0.033	20µA/20µA
LE	Latch Enable Input (active Low)	1.0/0.033	20µA/20µA
$Q_0$ - $Q_7$	Data outputs	150/40	3mA/24mA

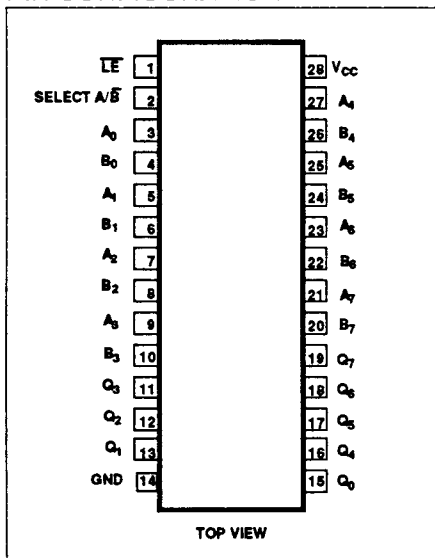
#### NOTE:

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

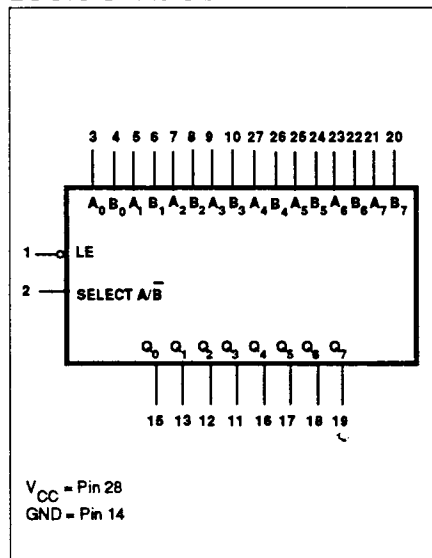
the latches when the Latch Enable (LE) input is Low and is latched on the LE rising

edge. The outputs are enabled when LE is High and disabled when LE is Low.

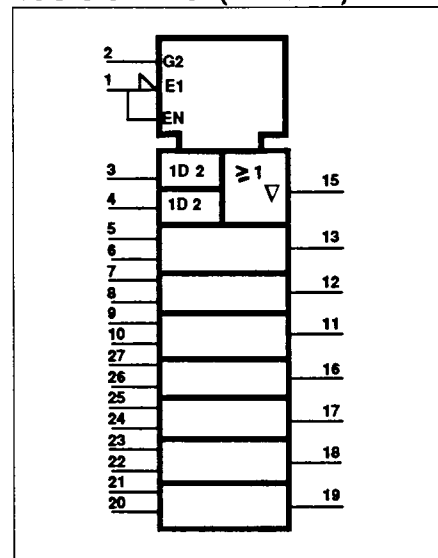
### PIN CONFIGURATION



### LOGIC SYMBOL



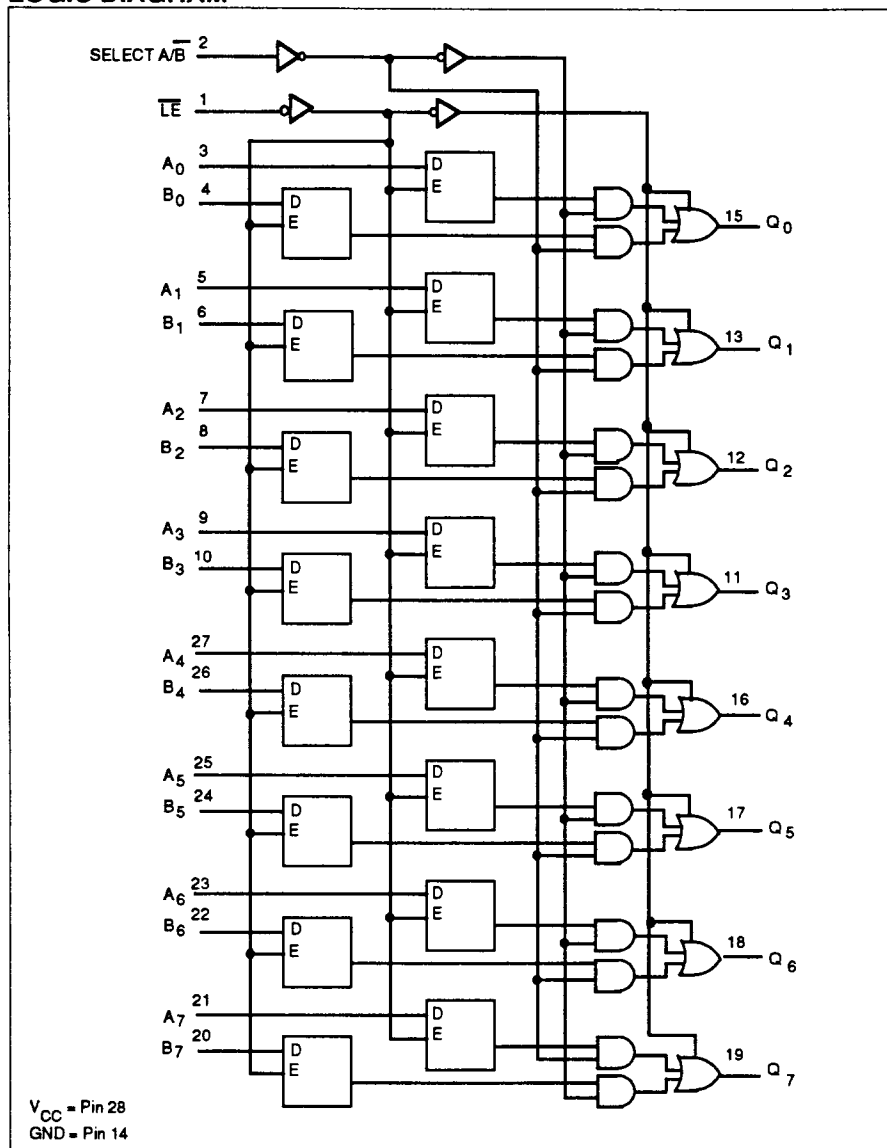
### LOGIC SYMBOL (IEEE/IEC)



Latch

FAST 74F604

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
$A_0-A_7$	$B_0-B_7$	SELECT A/B	LE	$Q_0-Q_7$
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z
X	X	L	H	B latched data
X	X	H	H	A latched data

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state
- ↑ = Low-to-High transition

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**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	48	mA
T <sub>A</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>STG</sub>	Storage temperature	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-3	mA
I <sub>OL</sub>	Low-level output current			24	mA
T <sub>A</sub>	Operating free-air temperature range	0		70	°C

**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			Min	Typ <sup>2</sup>	Max		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.4		V	
			±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.35	0.50	V
			±5%V <sub>CC</sub>		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = 0.0V, V <sub>I</sub> = 7.0V			100	µA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	µA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-20	µA	
I <sub>OZH</sub>	Off state output current, High-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V			50	µA	
I <sub>OZL</sub>	Off state output current, Low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V			-50	µA	
I <sub>OS</sub>	Short circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-60	-150	mA	
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX	A <sub>n</sub> , B <sub>n</sub> , SELECT A/B=4.5V, LE= ↑	60	82	mA	
			A <sub>n</sub> , B <sub>n</sub> , SELECT A/B=GND, LE= ↑	75	100	mA	
			A <sub>n</sub> , B <sub>n</sub> , SELECT A/B=GND, LE= GND	75	100	mA	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## Latch

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation delay SELECT A/B to $Q_n$ (B latch)	Waveform 1	5.0 6.0	7.0 8.5	9.0 10.5	4.5 5.5	10.0 11.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay SELECT A/B to $Q_n$ (A latch)	Waveform 2	6.0 4.0	8.0 6.5	10.0 8.5	5.5 3.5	11.5 9.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable time to High or Low level	Waveform 4 Waveform 5	5.0 5.0	7.5 7.5	9.5 9.5	4.5 4.5	10.5 11.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable time from High or Low leve	Waveform 4 Waveform 5	5.0 5.0	7.0 7.0	9.5 9.5	4.5 4.5	11.0 11.0	ns

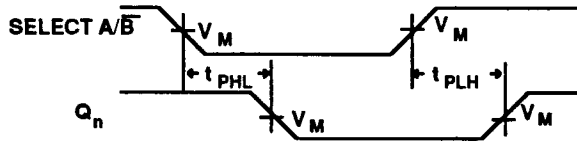
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $A_n, B_n$ to $\overline{LE}$	Waveform 3	1.0 2.0			2.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $A_n, B_n$ to $\overline{LE}$	Waveform 3	0 1.0			0 1.5		ns
$t_w(L)$	$\overline{LE}$ Pulse width, Low	Waveform 3	5.0			6.0		ns

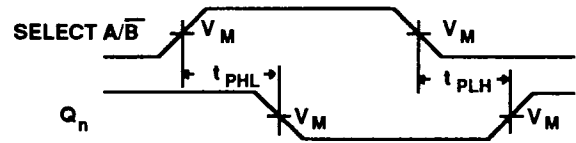
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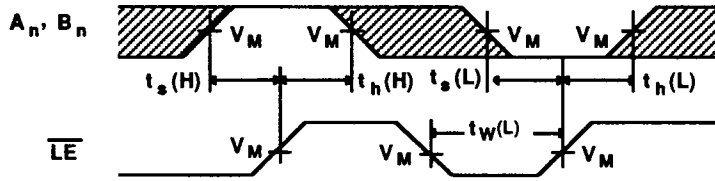
## AC WAVEFORMS



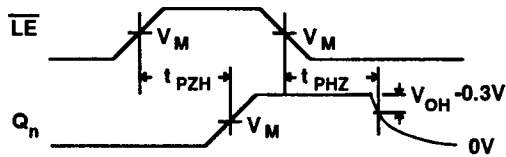
Waveform 1. Propagation Delay, SELECT A/B To Output (B latched data=Low, LE=H)



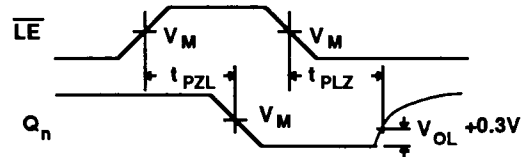
Waveform 2. Propagation Delay, SELECT A/B To Output (A latched data=Low, LE=H)



Waveform 3. Data Setup And Hold Times, Latch Enable pulse width



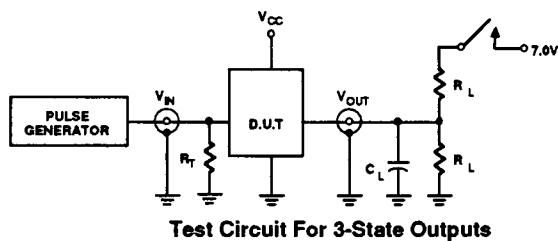
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms,  $V_M = 1.5V$ .  
The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT AND WAVEFORMS

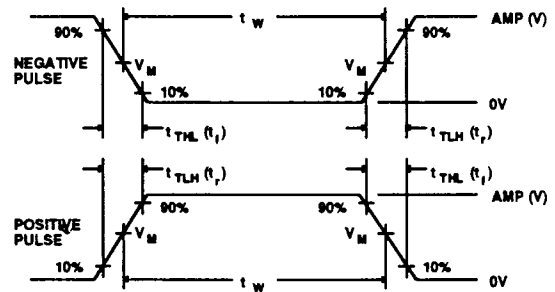


### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

### DEFINITIONS

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



$V_M = 1.5V$   
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1MHz	500ns	2.5ns	2.5ns