ICs for Carradio Applications

PLL Frequency Synthesizer, IF Counter, 7 bit ADC, 7 & 4 bit DAC

SDA 4335 Version V1

Target Specification 03.05.99

(33 pages incl. this page)

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SDA 4335 Revision History: Current Version: 03.05.99		
Previous Version:		
old Page	new Page	Subjects (major changes since last revision)

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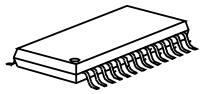
Version V1 **B6CA**

1 Overview

The SDA 4335 is a Car-Radio PLL frequency synthesizer implemented in Infineon BiCMOS technology B6CA. The device contains the PLL, 2 pin 61.5MHz Oscillator internally coupled to PLL, an IF Counter for AM & FM an 7 bit ADC, an 7 & 4 bit DAC and additonal 2 ports for input- or output-functions. Primary applications are in Car-Radio systems.



P-TSSOP-28

1.1 Features

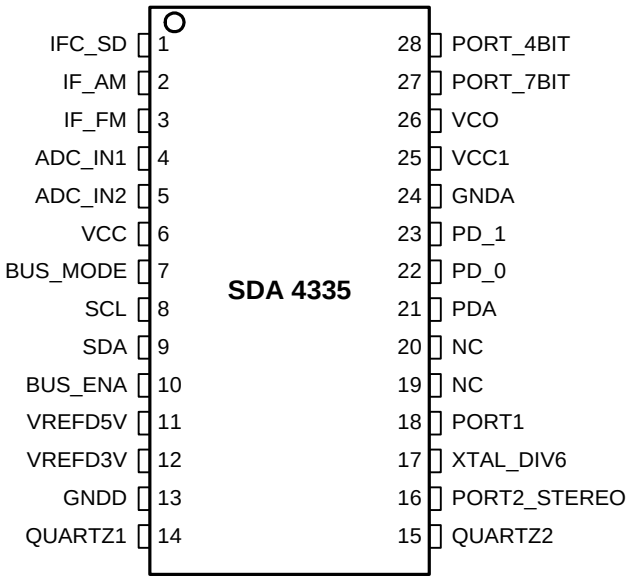
- Operation range 8 to 11 V
- I^2C Bus and 3Wire Bus operation selectable
- Bus interface with low threshold voltage Schmitt-Trigger inputs for interfacing 3V or 5V microprocessors
- 16 bit fully programmable R- and N-Counter
- Resolution e.g.100kHz, 50kHz, 25kHz, 12.5kHz, 10kHz, 6.25kHz, 6kHz, 5kHz, 3kHz, 1kHz.
- 4 programmable phase detector currents : 0.5mA, 1mA, 2mA, 4mA.
- Rail to rail Loop-amplifier
- 2 Chargepump-outputs for different timeconstants
- High running 2 pin crystal oscillator f_Q= 61.5MHz , adjustable via Bus
- Switchable output for 10.25MHz (500mVss @ load-capacitance 10pF)
- Multiplexed 7 bit ADC for ADC_IN1 and ADC_IN2. Result read out via bus (2 bytes).
- 7 bit DAC-output, range 0...VREFD5V
- 4 bit DAC-output, range 0...VREFD5V
- 3 free programmable output PORTS
- PORT 1: free programmable output
- PORT 2: for AM seek mode or input port for stereo-indicator
- PORT 3: IFC_SD for IF counter resolution or input port for station-detect
- Search tuning stop with IF counter measurement, result read out via bus or port.

	FM-mode	AM-mode
gatetime	320us...40.96ms	1ms...64ms
center-frequency (standard) (double)	10.40 MHz ... 11.19375 MHz or 20.80 MHz ... 22.3875 MHz	440kHz...471kHz
window-resolution (standard) (double)	+/- 6.25 kHz...100 kHz +/- 12.5 kHz...200 kHz	+/- 250Hz...4kHz

Type	Ordering Code	Package
SDA 4335		P-TSSOP-28

2 Circuit Description

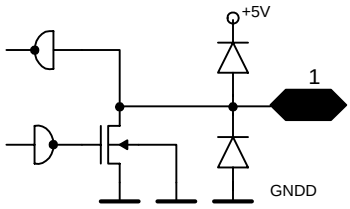
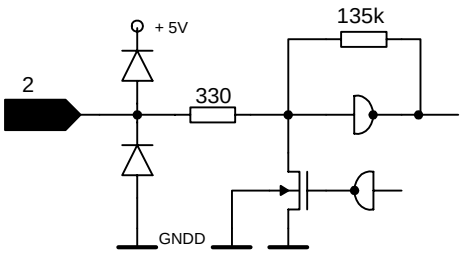
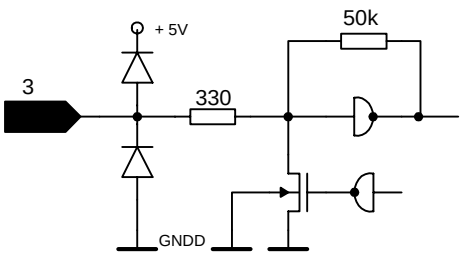
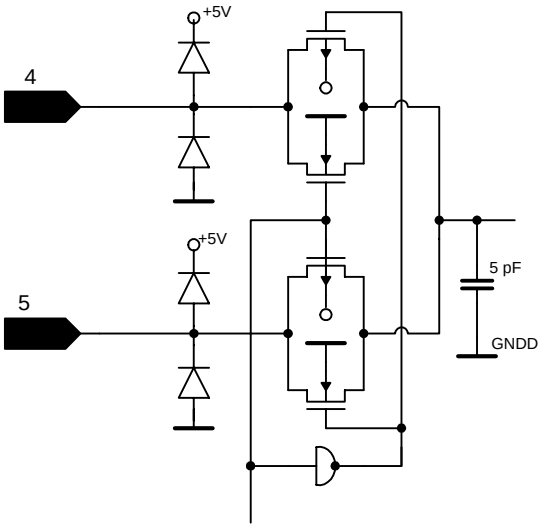
2.1 Pin Configuration

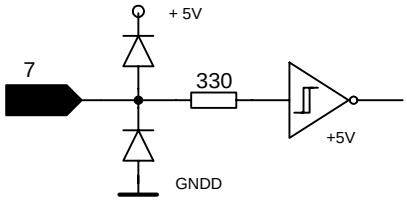
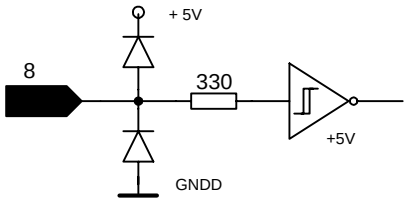
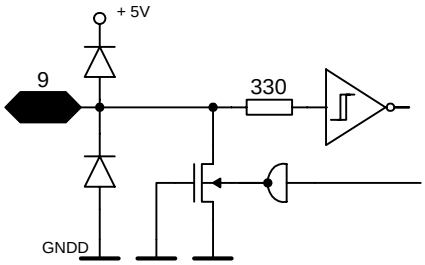
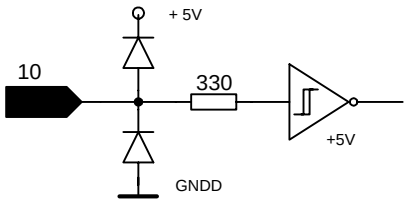


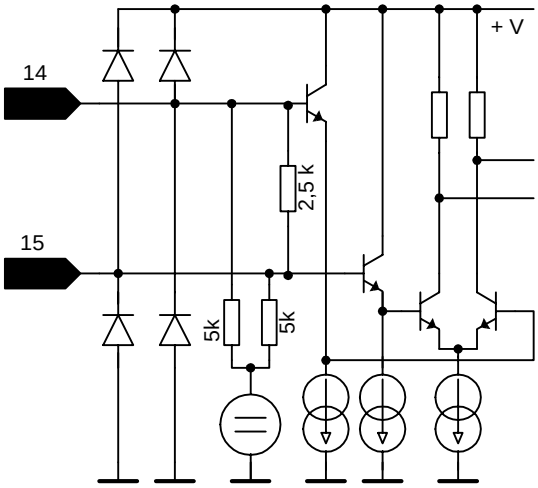
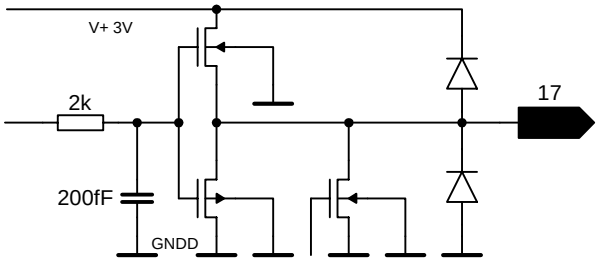
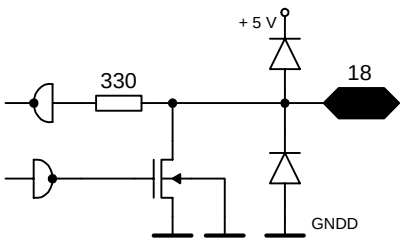
2.2 Pin Definitions and Functions

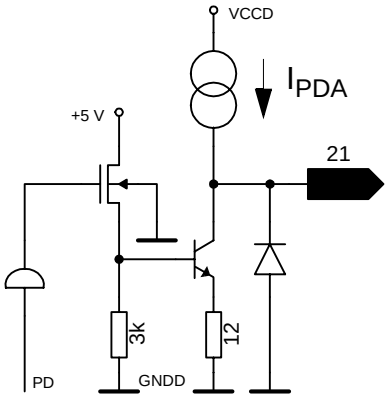
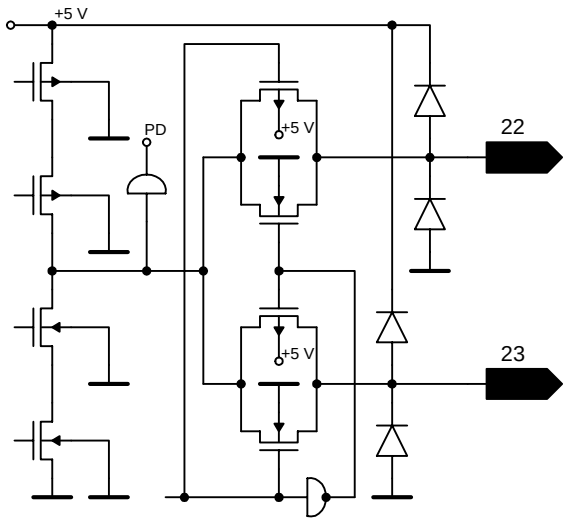
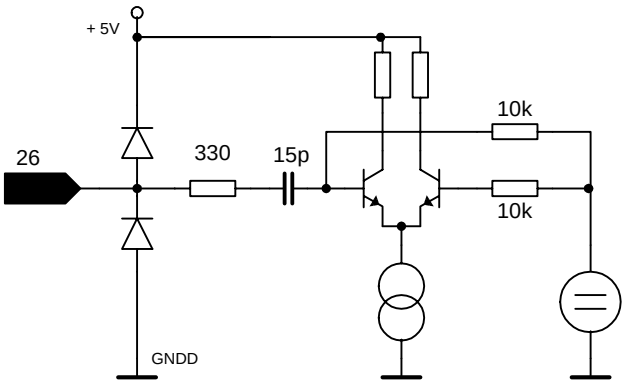
Pin No.	Symbol	Function
1	IFC_SD	PORT IF_Counter result output or Station-Detect input set by bus
2	IF_AM	IF_AM frequency input with counter request
3	IF_FM	IF_FM frequency input with counter request
4	ADC_IN1	PORT ADC1 Input
45	ADC_IN2	PORT ADC2 Input
6	VCC	Positive supply voltage (8...11V)
7	BUS_MODE	Data bus input: Bus-mode select Must be Low for I^2C-Bus-mode, must be High for 3 Wire -Bus-mode
8	SCL	Data bus input: Clock Clock input of the serial control interface with Schmitt-Trigger input stage
9	SDA	Data bus input / output: Bidirectional Data-input/output Data input of the serial control interface with Schmitt-Trigger input stage in write-mode. Data output in read-mode.
10	BUS_ENA	Bus input: Enable Enable input of the serial control interface with Schmitt-Trigger input stage. When EN=H the input signals CLK and DA are disabled. When EN=L the serial control interface is enabled. The received data are transferred to the registers with the positive edge of the EN_Q-signal.
11	VREFD5V	Reference voltage for analogue BiCMOS circuity
12	VREFD3V	Reference voltage for digital CMOS circuity
13	GNDD	Digital ground for CMOS circuity
14	QUARTZ1	Reference oscillator input1 / Crystal
15	QUARTZ2	Reference oscillator input2 / Crystal
16	PORT2_STEREO	Port2 open-drain output or Stereo detection input set by bus
17	XTAL_DIV6	Output crystal frequency divided by 6
18	PORT1	Port1 free programmable open-drain output
19	NC	Not connected (replaced by Digtal Alignment SDA 4336)
20	NC	Not connected (replaced by Digtal Alignment SDA 4336)
21	PDA	Phase detector output analogue (Tuningvoltage)
22	PD_0	Charge pump output Phase detector tristate charge pump output for PD_Select=Low
23	PD_1	Charge pump output Phase detector tristate charge pump output for PD_Select=High
24	GNDA	Analoge Ground for bipolar circuity
25	VCC1	25:Positive supply voltage for loop-amplifier of PLL (8...11V)
26	VCO	VCO frequency input. VCO input with sensitive preampifier for PLL
27	PORT_7BIT	Output port 7 bit DAC (Range: 0...VREFD5V)
28	PORT_4BIT	Output port 4 bit DAC (Range: 0...VREFD5V)

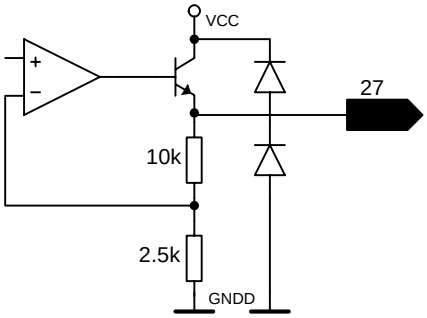
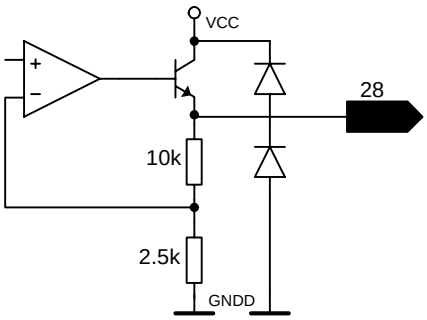
2.3 Internal input/output circuits

Pin No.	Symbol		Function
1	IFC_SD		1: IF_Counter output IF center or Station-Detect input
2	IF_AM		2: IF_AM input
3	IF_FM		3: IF_FM input
4 5	ADC_IN1 ADC_IN2		4: ADC Input_IN1 5: ADC Input_IN2
6	VCC		6: Positive supply voltage for serial bus and synthesizer

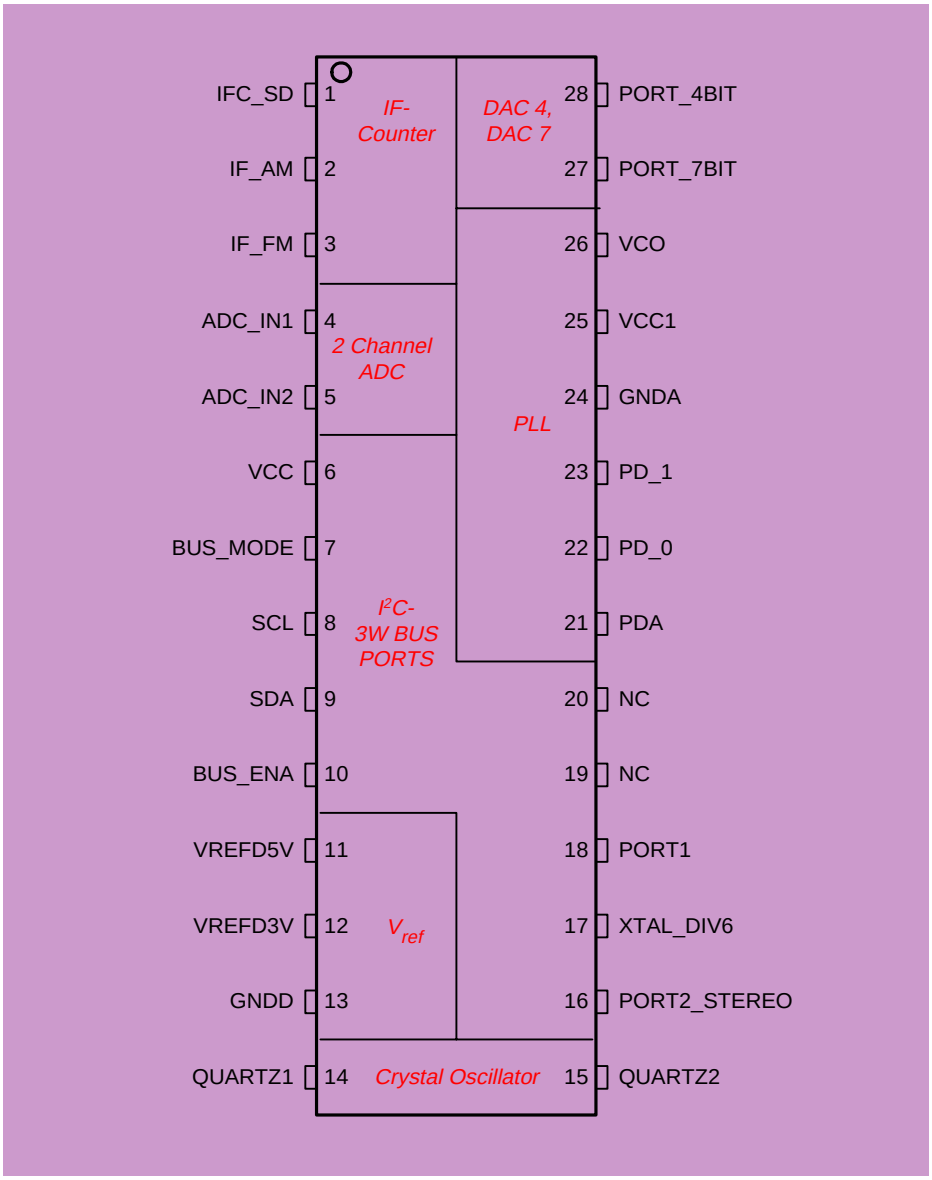
Pin No.	Symbol		Function
7	BUS_MODE		7: Bus mode input
8	SCL		8: Bus clock input
9	SDA		9: Data bus input / output
10	BUS_ENA		10: Bus enable input
11	VREFD5V		11: Reference voltage digital section 5V
12	VREFD3V		12: Reference voltage for digital section 3V
13	GNDD		13: Ground for serial bus and synthesizer

Pin No.	Symbol		Function
14	QUARTZ1		14: Reference oscillator input / Crystal
15	QUARTZ2		15: Reference oscillator input / Crystal
16	PORT2_STEREO		16: Port2 open-drain output or Stereo detection input set by bus
17	XTAL_DIV6		17: Crystal oscillator auxiliary output (10.25 MHz)
18	PORT1		18: Switch port output 2 (open drain)
19	NC		Not connected
20	NC		Not connected

Pin No.	Symbol		Function
21	PDA		21: PLL phase detector output analog (Tuning voltage)
22 23	PD_0 PD_1		22: PLL Charge pump output (Phase detector tristate charge pump output) 23: PLL Charge pump output (Phase detector tristate charge pump output)
24	GNDA		24: Ground for loop amplifier
25	VCC1		25: Positive power supply for loop-amplifier
26	VCO		26: VCO input

Pin No.	Symbol		Function
27	PORT_7BIT		27: Output port 7 bit
28	PORT_4BIT		28: Output port 4 bit

3 Block diagram



4 Circuit Description

The SDA 4335 is a FM car radio PLL synthesizer system with IF counter for STS, a 2 channel multiplexed 7 bit ADC, a 7 bit DAC- and a 4 bit DAC multifunctional output.
The serial bus is switchable between I^2C and 3 Wire bus mode.

4.1 7 bit A/D converter for ADC_IN1 and ADC_IN2 detector

The 7 bit A/D converter has two input channels and works as successive approximation converter. The conversion time for both input signals is t = 32 µs. The 7-bit digital-words from both channels (14 bit) are read out together via bus into two bytes with the read subadress 82H.
The input voltage range for both channels is 0...VREFD5V.

4.2 IF counter for STS

For FM-mode the center frequency is adjustable in 128 steps (6.25kHz for standard IF-frequency/ 12.5kHz for double IF-frequency) from 10.40MHz...11.19375MHz (standard) / 20.80MHz ... 22.3875MHz (double).
The gate-time is adjustable in 8 steps from 320us...40.96ms and the tolerance of the accepted count value, the window is adjustable in 5 steps from +/- (250Hz...4kHz).
For AM-mode the center frequency is adjustable in 128 steps (1kHz) from 384kHz ... 511kHz.
Mode is selectable by bus. In FM-mode the input IF_AM is going low with a internally NMOS Open drain transistor. In AM-mode the input IF_FM is going low with a internally NMOS Opendrain transistor.
The gate-time is adjustable in 7 steps from 1ms...64ms and the tolerance of the accepted count value, the window is adjustable in 5 steps from +/- (250Hz...4kHz).
The results IF_CENT and IF_WINDOW are read out via bus (read-subadress 82H). The result IF_CENT is optional avialable on pin IFC_SD set by bus.
If the IF frequency into the preselected window, IF_CENT goes from high to lo level.
The IF frequency is outside the preselected window, IF_CENT is high. The bit IF_WINDOW is a hint IF-frequency is to low (IF_WINDOW=high) or is to high (IF_WINDOW=low).
In addition to the frequency measurement, thresholds for ADC_IN1 and ADC_IN2 voltages can be programmed via bus (subaddress 0BH). IF_CENT will only go to low level in case fo ADC_IN1 and ADC_IN2 voltages are beyond the thresholds and the frequency is inside the window.
When setting the thresholds to zero ADC_IN1 and ADC_IN2 evaluation is disabled.

4.3 Crystal oscillator

A master crystal oscillator provides all necessary clock frequencies for the whole IC. A 61.5 MHz crystal is used in 3rd harmonic mode.
The oscillator frequency can fine tuned with a serial bus controlled 4 bit D/A converter.
The crystal frequency is used as reference frequency for the PLL oscillator and IF counter. It is also used as clock for the ADC. Finally the crystal frequency divided by 6 (10.25 MHz) is available at a pin as low pass filtered voltage. It can be disabled with the serial bus.

4.4 Output / input Ports

PORT1 is a NMOS Open drain output,
PORT2_STEREO and IFC_SD are NMOS Open drain outputs in port mode or inputs set by bus.
PORT_7BIT / PORT_4BIT are multifunctionaly DAC outputs with a output voltage range from V_{out}= 0...VREFD5V, with a resolution from 7 bit and 4 bit.

4.5 SOCCAR Bus

The SDA 4335 supports the I^2C bus protocol (2 wire) or 3 Wire bus protocol operation selectable by pin 7: BUS_MODE (I^2C=low, 3W=high). All bus pins (BUS_MODE, SCL, SDA, BUS_ENA) are Schmitt-triggered input buffer for 3V or 5V µC.
The bit stream begins with the most significant bit (MSB), is shifted in (write mode) on the low to high transition of CLK and is shifted out (read mode) on the high to low transition of CLK.

I²C bus mode

In this mode pin7 (BUS_MODE) = low and pin10 (BUS_ENA)=low. In this mode SDA is a bidirectional input / output pin.

Data Transition:

Data transition on the pin SDA must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as start or stop condition.

Start Condition (STA):

A start condition is defined by a high to low transition of the SDA line while SCL is at a stable high level.This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO):

A stop condition is defined by a low to high transition of the SDA while the SCL line is at a stable high level. This condition terminate the communication between the devices and forces the bus interface into the initial conditions.

Acknowlage (ACK):

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will pull the SDA line to low level to indicate it has receive the 8 bits of data correctly.

Data Transfer Write Mode:

To start the communication, the bus master must initiate a start condition, followed by the 8bit chip address (write). The chip address for the SDA 4335 is fixed as ”1100110” (MSB at first). The last bit (LSB=A0) of the chip address byte defines the typ of operation to be performed:
A0=1, a read operation is selected and A0=0, a write operation is selected. After this comparision the SDA 4335 will generate an ACK.
After this device addressing the desired sub address byte and data bytes must be followed. The subaddresses determines which one of the 9 data bytes (00H...07H, 0BH) is transmitted first. At the end of data transition the master must be generate the stop condition.

Data Transfer Read Mode:

To start the communication in the read mode, the bus master must initiate a start condition, fol lowed by the 8bit chip address (write: A0=0), followed by the sub address read (82H or 83H), followed by the chip address (read: A0=1). After that procedure the 16bit data register 82H or the 8bit data register 83H is read out. After the first 8 bit read out, the uP mandatory send LOW during the ACK-clock. After the second 8 bit read out the uP mandatory send HIGH during the ACK-clock. At the end of data transition the master must be generate the stop condition.

3W bus mode

In this mode pin4 (BUS_MODE) =high. Pin6 (SDA) is a bidirectional input / output pin in this mode. Pin8 (BUS_ENA) is used to activate the bus interface to allow the transfer of data to / from the device. When BUS_ENA is in an inactive high state, shifting is inhibited.

Data Transition:

Data transition on the pin SDA must only occur when the clock SCL is low. To transfer data to / from the device, BUS_ENA (which must start inactive high) is taken low, a serial transfer is made via SDA, CLK and BUS_ENA is taken back high. The bit stream needs neither the chip address.

Data Transfer Write Mode:

To start the communication, the BUS_ENA is taken low. The desired sub address byte and data bytes must be followed. The subaddresses determines which one of the 9 data bytes (00H...07H, 0BH) is transmitted first. At the end of data transition the BUS_ENA must be high.

Data Transfer Read Mode:

To start the communication in the read mode, the BUS_ENA is taken low, followed by the sub address read (82H or 83H). After that the device is ready to read out the 16bit data register 82H or the 8bit data register 83H. At the end of data transition the BUS_ENA must be high.

4.6 PLL Synthesizer

R / N Counter

The SDA 4335 has 2 identical 16bit counter for R and N path. Input frequency for the R-counter is the buffered XTAL-frequency (61.5MHz). Tuning steps can be selected by the 16bit R-counter from f_R= 6.25kHz...100kHz. Input frequency for the N-counter is the buffered LO-frequency (in FM mode 98.2MHz...118.7MHz).

Three State Phase Comparator

The phase comparator generates a phase error signal according to phase difference between f_R (R counter output) and f_N (N counter output).This phase error signal drives the charge pump current generator. Polarity is fixed positiv for this application note.

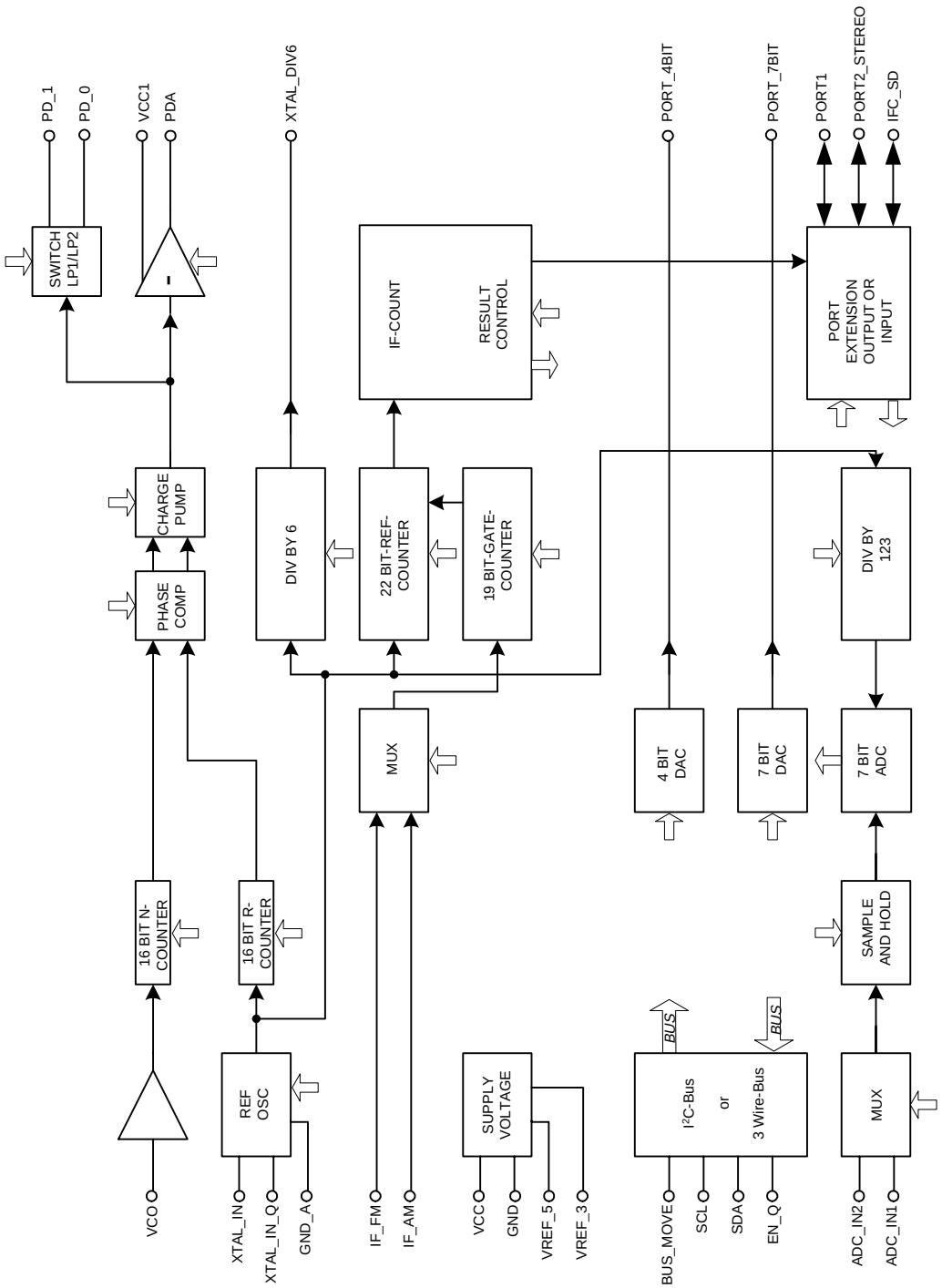
Charge Pump

The charge pump generates signed pulses of current. 4 current values and 2 outputs are available.

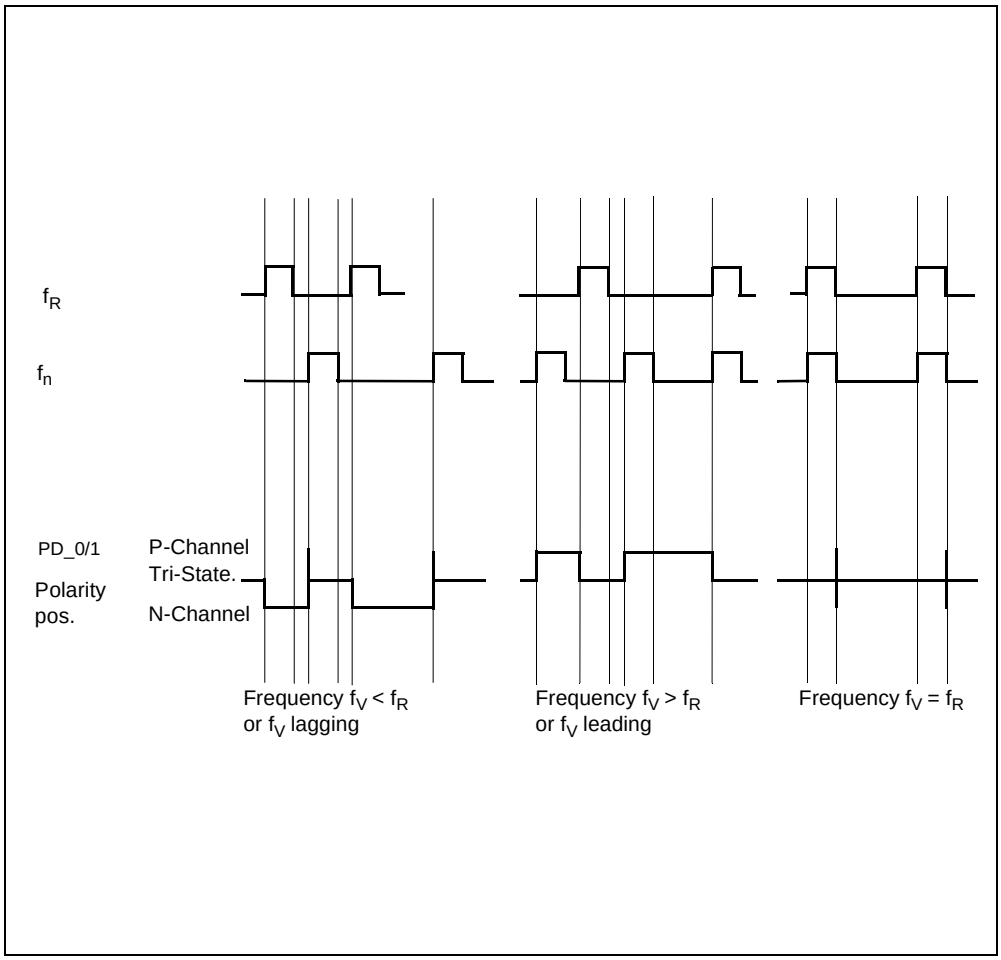
Loop Amp

The integrated rail to rail loop amplifier allows an active loop filter design with external components. Two modes are availiable with status bit D11: high speed and normal mode.

5 Functional Block Diagram



6 Phase detector outputs



6.1 Bus Interface

Pin Function

Pin name	BUS_MODE	BUS_ENA	SCL	SDA
Function	Bus mode select	Enable	Serial clock	Serial data
I2C-mode	Low	High=Inactiv, Low=Activ	Clock input	Data in / out
3Wire mode	High			

6.1.1 Bus Data Format

I²C Bus Write Mode

	MSB	CHIP ADDRESS (WRITE)					LSB		MSB	SUB ADDRESS (WRITE) 00H...07H, 0BH						LSB		MSB	DATA IN X...0 (X=7 or 15)						LSB		
STA	1	1	0	0	1	1	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	DX	...	D5	D4	D3	D2	D1	D0	ACK	STO

I²C Bus Read Mode

	MSB	CHIP ADDRESS (WRITE)					LSB		MSB	SUB ADDRESS (READ) 82H / 83H							LSB			MSB	CHIP ADDRESS (READ)						LSB	
STA	1	1	0	0	1	1	0	0	ACK	1	0	0	0	0	0	1	0	ACK	STA	1	1	0	0	1	1	0	1	ACK

MSB	DATA OUT FROM SUB ADD 82H							LSB		MSB	DATA OUT FROM SUB ADD 82H								LSB		
R15	R14	R13	R12	R11	R10	R9	R8	ACK[1]		R7	R6	R5	R4	R3	R2	R1	R0	ACK[2]		STO
MSB	DATA OUT FROM SUB ADD 83H							LSB													
R7	R6	R5	R4	R3	R2	R1	R0	ACK[2]		STO											

1): mandatory LOW send by uP, 2): mandatory HiGH send by uP

3W Bus Write Mode

MSB	SUB ADDRESS (WRITE) 00H...07H, 0BH						LSB	MSB	DATA IN X...0 (X=7 or 15)						LSB
S7	S6	S5	S4	S3	S2	S1	S0	DX	...	D5	D4	D3	D2	D1	D0

3W Bus Read Mode

MSB	SUB ADDRESS (READ) 82H						LSB	MSB	DATA OUT FROM SUB ADD 82H (MSB)							LSB	MSB	DATA OUT FROM SUB ADD 82H (LSB)							LSB
1	0	0	0	0	0	1	0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
MSB	SUB ADDRESS (READ) 83H						LSB	MSB	DATA OUT FROM SUB ADD 83H (MSB)							LSB									
1	0	0	0	0	0	1	1	R7	R6	R5	R4	R3	R2	R1	R0										

Chipaddress Organisation

Chip Address (only I²C mode)								
MSB							LSB	Function
1	1	0	0	1	1	0	0	Chip Address Write
1	1	0	0	1	1	0	1	Chip Address Read

Subaddress

Sub Addresses of Data Registers Write									
MSB	Bin						LSB	Hex	Function
0	0	0	0	0	0	0	0	00H	Status
0	0	0	0	0	0	0	1	01H	R_Counter
0	0	0	0	0	0	1	0	02H	N_Counter
0	0	0	0	0	0	1	1	03H	DAC7
0	0	0	0	0	1	0	0	04H	IF_COUNT_P1
0	0	0	0	0	1	0	1	05H	IF_COUNT_P2
0	0	0	0	0	1	1	0	06H	Specials
0	0	0	0	0	1	1	1	07H	DAC4
0	0	0	0	1	0	1	1	0BH	COMP_PRESET

Sub Address of Data Register Read									
MSB	Bin						LSB	Hex	Function
1	0	0	0	0	0	1	0	82H	Result ADC_IN2, ADC_IN1, IF_Window and IF_Center
1	0	0	0	0	0	1	1	83H	Result_Misc

Data Byte Specification

Status Subaddress 00H	
Bit	Function
MSB D15	not used (must be=0)
D14	PORT2_STEREO
D13	PORT1
D12	Stereo-Flag
D11	Loopamp current
D10	not used (must be=0)
D9	not used (must be=0)
D8	AM / FM
D7	ADC_Single
D6	ADC_Mode
D5	ADC_ON
D4	DAC4
D3	PD_Select
D2	CP_Current 2
D1	CP_Current 1
D0 LSB	CP_Mode

R_Counter Subaddress 01H	
Bit	Function
MSB D15	2^{15}
D14	2^{14}
D13	2^{13}
D12	2^{12}
D11	2^{11}
D10	2^{10}
D9	2^{9}
D8	2^{8}
D7	2^{7}
D6	2^{6}
D5	2^{5}
D4	2^{4}
D3	2^{3}
D2	2^{2}
D1	2^{1}
D0 LSB	2^{0}

N_Counter Subaddress 02H	
Bit	Function
MSB D15	2^{15}
D14	2^{14}
D13	2^{13}
D12	2^{12}
D11	2^{11}
D10	2^{10}
D9	2^{9}
D8	2^{8}
D7	2^{7}
D6	2^{6}
D5	2^{5}
D4	2^{4}
D3	2^{3}
D2	2^{2}
D1	2^{1}
D0 LSB	2^{0}

COMP_PRESET Subaddress 0BH	
Bit	Function
MSB D15	not used
D14	V_IN1_2^{6}
D13	V_IN1_2^{5}
D12	V_IN1_2^{4}
D11	V_IN1_2^{3}
D10	V_IN1_2^{2}
D9	V_IN1_2^{1}
D8	V_IN1_2^{0}
D7	not used
D6	V_IN2_2^{6}
D5	V_IN2_2^{5}
D4	V_IN2_2^{4}
D3	V_IN2_2^{3}
D2	V_IN2_2^{2}
D1	V_IN2_2^{1}
D0 LSB	V_IN2_2^{0}

DAC7 Subaddress 03H	
Bit	Function
MSB D7	Enable
D6	DAC7_6
D5	DAC7_5
D4	DAC7_4
D3	DAC7_3
D2	DAC7_2
D1	DAC7_1
D0 LSB	DAC7_0

IF_Count_P1 Subaddress 04H	
Bit	Function
MSB D7	Enable
D6	Station_ Detect
D5	Win_2
D4	Win_1
D3	Win_0
D2	Gate_2
D1	Gate_1
D0 LSB	Gate_0

IF_Count_P2 Subaddress 05H	
Bit	Function
MSB D7	CF_Mode
D6	CF_6
D5	CF_5
D4	CF_4
D3	CF_3
D2	CF_2
D1	CF_1
D0 LSB	CF_0

Specials Subaddress 06H	
Bit	Function
MSB D7	XTAL_DIV6
D6	not used
D5	not used
D4	not used
D3	XTAL_3
D2	XTAL_2
D1	XTAL_1
D0 LSB	XTAL_0

IF_DAC4 Subaddress 07H	
Bit	Function
MSB D7	not used
D6	not used
D5	not used
D4	not used
D3	DAC4_3
D2	DAC4_2
D1	DAC4_1
D0 LSB	DAC4_0

Results ADC_IN1, ADC_IN2 and IF counter Subaddress 82H (read address)	
Bit	Function
MSB D15	IF_window
D14	ADC_IN2_2^6
D13	ADC_IN2_2^5
D12	ADC_IN2_2^4
D11	ADC_IN2_2^3
D10	ADC_IN2_2^2
D9	ADC_IN2_2^1
D8	ADC_IN2_2^0
D7	IF_center
D6	ADC_IN1_2^6
D5	ADC_IN1_2^5
D4	ADC_IN1_2^4
D3	ADC_IN1_2^3
D2	ADC_IN1_2^2
D1	ADC_IN1_2^1
D0 LSB	ADC_IN1_2^0

Result Misc Subaddress 83H	
Bit	Function
MSB D7	IF_Window
D6	IF_Center
D5	ADC_IN1_Comp
D4	ADC_IN2_Comp
D3	Res
D2	Res
D1	Station_Detect
D0 LSB	Stereo_Flag

Status, Subaddress 00H																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0					0	0										these bits must be = 0
0	1		0													opendrain Port2_Stereo output = high level (port-mode)
0	0		0													opendrain Port2_Stereo output = low level (port-mode)
0	x		1													opendrain Port2_Stereo is input for Stereoflag
0		1														opendrain Port1 output = high level
0		0														opendrain Port1 output = low level
0				1												Loopamp currentsource high ($I_{LOOPAMP}$=2.4mA) for high speed tuning
0				0												Loopamp currentsource low ($I_{LOOPAMP}$=1.2mA)
0							1									AM-Mode
0							0									FM-Mode
0								0	0	1						7 bit AD Converter enabled for single mode, stop
0								1	0	1						7 bit AD Converter enabled for single mode start. To restart single mode write the same bits once more.
0								0	1	1						7 bit AD Converter enabled for continuos mode run.
0								x	x	1						7 bit AD Converter enabled for single or continous mode
0								x	x	0						7 bit AD Converter disabled for single and continous mode
0											1					DAC4 enabled (see subaddress 07H)
0											0					DAC4 disabled (see subaddress 07H)
0												1				Phase detector select; PD_1=ON, PD_0=OFF
0												0				Phase detector select; PD_1=OFF, PD_0=ON
0													1	1		Chargepump current I_{cp3} = 4mA
0													1	0		Chargepump current I_{cp2} = 2mA

0													0	1		Chargepump current I_{cp1} = 1mA
0													0	0		Chargepump current I_{cp0} = 500uA
0															1	Chargepump enabled
0															0	Chargepump disabled

Subaddress 01H, R_Counter and Subaddress 02H, N_Counter																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Divider by 65535
0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	Divider by 2000
0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	0	Divider by 1230
0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	Divider by 1000
0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	Divider by 615
0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	Divider by 100
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	Divider by 10
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	Divider by 2

Subaddress 03H, DAC7								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								DAC7 enabled
0	x	x	x	x	x	x	x	DAC7 disabled
1	1	1	1	1	1	1	1	DAC7_127 (full scale)
1	1	0	0	0	0	1	1	DAC7_66 (MSB+3*LSB)
1	1	0	0	0	0	1	0	DAC7_65 (MSB+2*LSB)
1	1	0	0	0	0	0	1	DAC7_64 (MSB+LSB)
1	1	0	0	0	0	0	0	DAC7_63 (MSB)
1	0	1	1	1	1	1	1	DAC7_62 (MSB-LSB)
1	0	1	1	1	1	1	0	DAC7_61 (MSB-2*LSB)
1	0	1	1	1	1	0	1	DAC7_60 (MSB-3*LSB)
1	0	1	1	1	1	0	0	DAC7_59 (MSB-4*LSB)
1	0	0	0	0	0	1	0	DAC7_2 (zero+2*LSB)
1	0	0	0	0	0	0	1	DAC7_1 (zero+LSB; LSB=39mV)
1	0	0	0	0	0	0	0	DAC7_0 zero

Subaddress 04H, IF_Count_P1								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								IF_Count enabled
0								IF_Count disabled
	1							Port IFC_SD is input for station_detect to start IF_COUNT externally, if the station detetect goes to high
	0							Port IFC_SD is output for result IF_CENTER
								FM_MODE / AM_MODE
		1	0	0				Window= ±100kHz* / 4kHz
		0	1	1				Window= ±50kHz* / 2kHz
		0	1	0				Window= ±25kHz* / 1kHz
		0	0	1				Window= ±12.5kHz* / 500Hz
		0	0	0				Window= ±6.25kHz* / 250Hz
					1	1	1	Gatetime= 40.96ms/not used
					1	1	0	Gatetime= 20.48ms / 64ms
					1	0	1	Gatetime= 10.24ms / 32ms
					1	0	0	Gatetime= 5.12ms / 16ms
					0	1	1	Gatetime= 2.56ms / 8ms
					0	1	0	Gatetime= 1.28ms / 4ms
					0	0	1	Gatetime= 640us / 2ms
					0	0	0	Gatetime= 320us / 1ms

* Valid for D7=0 in subaddress 05H in FM_Mode
Multiply window value with 2 for D7=1 in subaddress 05H
(e. g. D7=0 Window= ± 6.25 kHz
D7=1 Window= ± 12.5 kHz)

Subaddress 05H, IF_Count_P2, FM_Mode Centerfrequency = CF, CF_FM$_{step}$= 6.25kHz/12.5kHz								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								Centerfrequency CF1
0								Centerfrequency CF0
1	1	1	1	1	1	1	1	CF1= 22.3875 MHz
0	1	1	1	1	1	1	1	CF0= 11.1937 MHz
1	1	0	0	0	0	0	0	CF1= 22.600 MHz
0	1	0	0	0	0	0	0	CF0= 10.800 MHz
1	0	1	1	0	0	0	1	CF1= 21.4125 MHz
0	0	1	1	0	0	0	1	CF0= 10.70625 MHz
1	0	1	1	0	0	0	0	CF1= 21.400 MHz
0	0	1	1	0	0	0	0	CF0= 10.700 MHz
1	0	1	0	1	1	1	1	CF1= 21.3875 MHz
0	0	1	0	1	1	1	1	CF0= 10.69375 MHz
1	0	1	0	0	0	0	0	CF1= 21.200 MHz
0	0	1	0	0	0	0	0	CF0= 10.600 MHz
1	0	0	1	0	0	0	0	CF1= 21.000 MHz
0	0	0	1	0	0	0	0	CF0= 10.500 MHz
1	0	0	0	0	0	0	0	CF1= 20.800 MHz
0	0	0	0	0	0	0	0	CF0= 10.400 MHz

Centerfrequencies FM for

D7=1 CF1= 20.800 MHz +n*12.5 kHz, CF_{Step}=12.5 kHz

D7=0 CF0= 10.400 MHz +n*6.25 kHz, CF_{Step}=6.25 kHz

n=0...127

Subaddress 05H, IF_Count_P2, AM_MODE Centerfrequency = CF, CF_AM$_{step}$= 1kHz)								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0								Centerfrequency CFO
0	1	0	1	0	1	1	1	CF_AM= 471kHz
0	1	0	1	0	1	1	0	CF_AM= 470kHz
0	1	0	1	0	1	0	1	CF_AM= 469kHz
0	1	0	1	0	1	0	0	CF_AM= 468kHz
0	1	0	1	0	0	1	1	CF_AM= 467kHz
0	1	0	1	0	0	1	0	CF_AM= 466kHz
0	1	0	1	0	0	0	1	CF_AM= 465kHz
0	1	0	1	0	0	0	0	CF_AM= 464kHz
0	1	0	0	1	1	1	1	CF_AM= 463kHz
0	1	0	0	1	1	1	0	CF_AM= 462kHz
0	1	0	0	1	1	0	1	CF_AM= 461kHz
0	1	0	0	1	1	0	0	CF_AM= 460kHz
0	1	0	0	1	0	1	1	CF_AM= 459kHz
0	1	0	0	1	0	1	0	CF_AM= 458kHz
0	1	0	0	1	0	0	1	CF_AM= 457kHz
0	1	0	0	1	0	0	0	CF_AM= 456kHz
0	1	0	0	0	1	1	1	CF_AM= 455kHz
0	1	0	0	0	1	1	0	CF_AM= 454kHz
0	1	0	0	0	1	0	1	CF_AM= 453kHz
0	1	0	0	0	1	0	0	CF_AM= 452kHz
0	1	0	0	0	0	1	1	CF_AM= 451kHz
0	1	0	0	0	0	1	0	CF_AM= 450kHz
0	1	0	0	0	0	0	1	CF_AM= 449kHz
0	1	0	0	0	0	0	0	CF_AM= 448kHz
0	0	1	1	1	1	1	1	CF_AM= 447kHz
0	0	1	1	1	1	1	0	CF_AM= 446kHz
0	0	1	1	1	1	0	1	CF_AM= 445kHz
0	0	1	1	1	1	0	0	CF_AM= 444kHz
0	0	1	1	1	0	1	1	CF_AM= 443kHz
0	0	1	1	1	0	1	0	CF_AM= 442kHz
0	0	1	1	1	0	0	1	CF_AM= 441kHz
0	0	1	1	1	0	0	0	CF_AM= 440kHz

Centerfrequencies AM for

D7=0 CF_AM=384kHz+n*1kHz, CF_{Step}=1kHz

n=0...127

Subaddress 06H, Specials								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	x	x	x					not used
1								XTAL_DIV6 enabled
0								XTAL_DIV6 disabled
				1	1	1	1	XTAL_adjust C_L = 15 pF
				1	1	1	0	XTAL_adjust C_L = 14pF
				1	1	0	1	XTAL_adjust C_L = 13 pF
				1	1	0	0	XTAL_adjust C_L = 12 pF
				1	0	1	1	XTAL_adjust C_L = 11 pF
				1	0	1	0	XTAL_adjust C_L = 10 pF
				1	0	0	1	XTAL_adjust C_L = 9 pF
				1	0	0	0	XTAL_adjust C_L = 8 pF
				0	1	1	1	XTAL_adjust C_L = 7 pF
				0	1	1	0	XTAL_adjust C_L = 6 pF
				0	1	0	1	XTAL_adjust C_L = 5 pF
				0	1	0	0	XTAL_adjust C_L = 4 pF
				0	0	1	1	XTAL_adjust C_L = 3 pF
				0	0	1	0	XTAL_adjust C_L = 2 pF
				0	0	0	1	XTAL_adjust C_L = 1pF
				0	0	0	0	XTAL_adjust C_L = 0pF

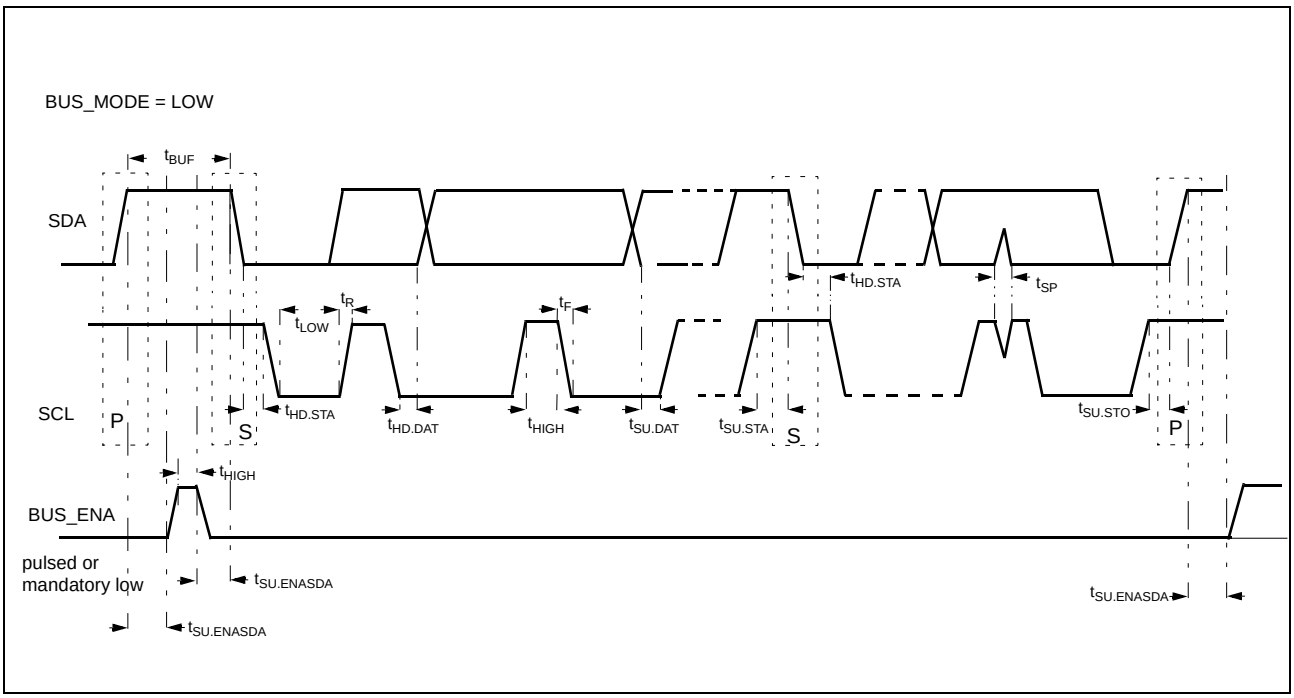
Subaddress 07H, IF_DAC4								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
x	x	x	x					not used
				1	1	1	1	DAC4_15 (full scale)
				1	1	1	0	DAC4_14
				1	1	0	1	DAC4_13
				1	1	0	0	DAC4_12
				1	0	1	1	DAC4_11
				1	0	1	0	DAC4_10 (MSB+2*LSB)
				1	0	0	1	DAC4_9 (MSB+LSB)
				1	0	0	0	DAC4_8 (MSB)
				0	1	1	1	DAC4_7
				0	1	1	0	DAC4_6
				0	1	0	1	DAC4_5
				0	1	0	0	DAC4_4
				0	0	1	1	DAC4_3 (zero+3*LSB)
				0	0	1	0	DAC4_2 (zero+2*LSB)
				0	0	0	1	DAC4_1 (zero+LSB; LSB=333mV)
				0	0	0	0	DAC4_0 zero

Subaddress 0BH, Comp preset																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
X								X								not used
	$IN1P2^6$	$IN1P2^5$	$IN1P2^4$	$IN1P2^3$	$IN1P2^2$	$IN1P2^1$	$IN1P2^0$									Preset value IN1
									$IN2P2^6$	$IN2P2^5$	$IN2P2^4$	$IN2P2^3$	$IN2P2^2$	$IN2P2^1$	$IN2P2^0$	Preset value IN2

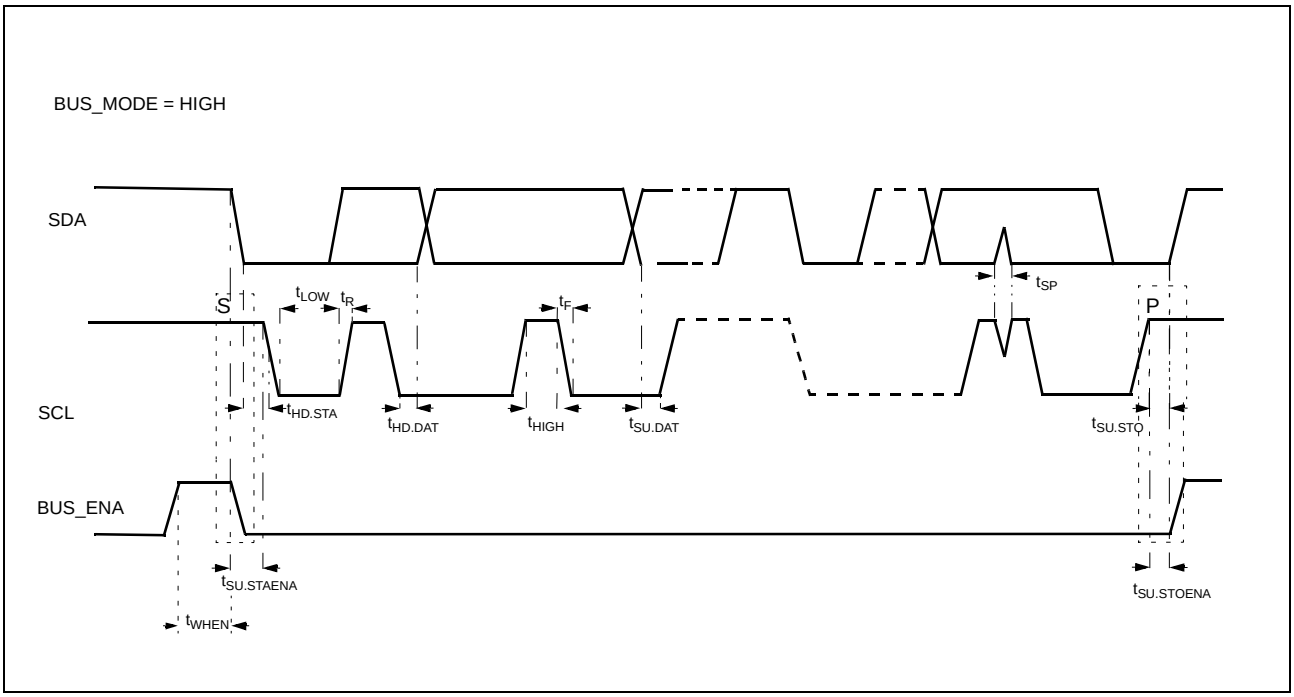
Subaddress 82H, Read Results from ADC_IN1, ADC_IN2 and IF counter																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1								1								IF_counter result: IF frequency is outside the desired window. IF frequency is lower as the desired IF frequency.
0								1								IF_counter result: IF frequency is outside the desired window.IF frequency is higher as the desired IF frequency.
x								0								IF_counter result: IF frequency is inside the desired window
	IN2_2^6	IN2_2^5	IN2_2^4	IN2_2^3	IN2_2^2	IN2_2^1	IN2_2^0									Result ADC_IN2 byte IN2_6...IN2_0
									IN1_2^6	IN1_2^5	IN1_2^4	IN1_2^3	IN1_2^2	IN1_2^1	IN1_2^0	Result ADC_IN1 byte IN1_6...IN1_0

Subaddress 83H, Read Results from MISC									
MSB							LSB	Function	
D7	D6	D5	D4	D3	D2	D1	D0		
1	1							IF_counter result: IF frequency is outside the desired window. IF frequency is lower as the desired IF frequency.	
0	1							IF_counter result: IF frequency is outside the desired window. IF frequency is higher as the desired IF frequency.	
X	0							IF_counter result: IF frequency is inside the desired window.	
		1						IN1_Voltage is higher than the preseted value (D8 .. D14) in 0BH	
		0						IN1_Voltage is lower than the preseted value (D8 .. D14) in 0BH	
			1					IN2_Voltage is higher than the preseted value (D0 .. D6) in 0BH	
			0					IN2_Voltage is lower than the preseted value (D0 .. D6) in 0BH	
				1	1			not used	
						1		Start IF_counter on the rising edge from low to high	see also D7 & D6 in Subadress 04H, IF_Count_P1
						0		Standby IF_counter	
							X	Input signal Stereo_Flag from PORT2_STEREO (x=0 or 1)	

6.1.2 I²C Bus Timing



3W-Bus Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
LOW level input voltage (SDA, SCL, BUS_ENA, BUS_MODE)	V_{IL}	-0.5	0.90	V
HIGH level input voltage (SDA, SCL, BUS_ENA, BUS_MODE)	V_{IH}	2.10	5.50	V
Pulse widh of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
LOW level output voltage 3mA sink current (SDA)	V_{OL}	0	0.40	V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10pF to 400pFwith up to 3mA	t_{OF}	$20+0.1C_b$ [3]	250	ns
SCL clock frequency	f_{SCL}	0	400	kHz
Bus free time between a STOP and START condition [1]	t_{BUF}	1.3		us
Hold time (repeated) START condition. After this period, the first clock pulse is generated. [1]	$t_{HO.STA}$	0.6		us
LOW period of the SCL clock	t_{LOW}	1.3		us
HIGH period of the SCL clock	t_{HIGH}	0.6		us
Set-up time for a repeated START condition [1]	$t_{SU.STA}$	0.6		us
Data hold time	$t_{HD.DAT}$	0		ns
Data set -up time	$t_{SU.DAT}$	100		ns
Rise, fall time of both SDA and SCL signals	t_R, t_F	$20+0.1C_b$ [3]	300	ns
Set-up time for STOP condition [1]	$t_{SU.STO}$	0.6		us
Capacitive load for each bus line	C_b		400	pF
Setup time SCL to BUS_ENA [2]	$t_{SU.SCLEN}$	0.6		us
H-pulsewidth (BUS_ENA)	t_{WHEN}	0.6		us

[1] only in I^2C bus mode
[2] only in 3W bus mode
[3] C_b= capacitance of one bus line in pF.
Note that the maximum t_F for the SDA and SCL bus lines quoted at 300ns is longer than the specified maximum t_{OF} for the output stages (250ns).This allows series protection resistors to be connected between the SDA / SCL pins and the SDA /SCL bus lines without exceeding the maximum specified t_F.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

The maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

Parameter	Symbol	Limit Values		Units
		min.	max.	
ESD-Protection all bipolar pins HBM (R=1.5kΩ , C=100pF)	V_{ESD}	- 2	2	kV
ESD-Protection all CMOS pins HBM (R=1.5kΩ , C=100pF)	V_{ESD}	t.b.d.	t.b.d.	kV
Total power dissipation	P_{tot}		150	mW
Ambient temperature	T_A	- 40	85	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	- 40	125	°C
Thermal resistance P-TSSOP-28 (sys-air)	T_{thSA}		114	K/W

All values are referred to ground (pin), unless stated otherwise.
All currents are designated according to the source and sink principle, i.e. if the device pin is to be regarded as a sink (the current flows into the stated pin to internal ground), it has a negative sign, and if it is a source (the current flows from Vs across the designated pin), it has a positive sign.

7.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min	max		
Supply voltage	V_{VCC}	8	11	V	
Current consumption	I_{vcc}		30	mA	
Ambient temperature	T_A	- 40	85	°C	

7.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

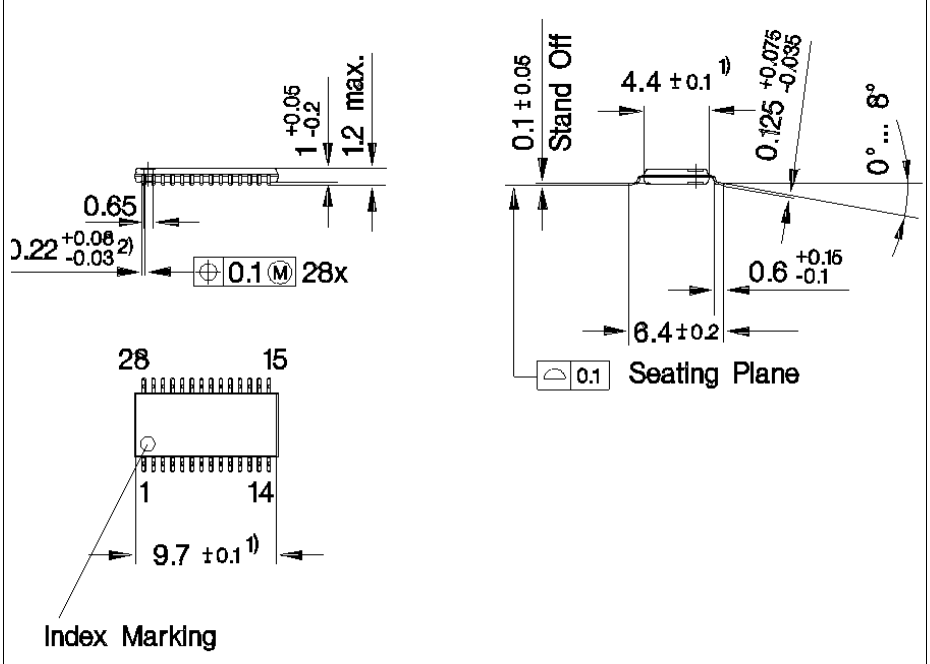
Parameter T_A **= 25 °C,** V_{VCC} **= 8.5V**	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Power supply						
Total current consumption	I_{VCC}		20		mA	
Crystal oscillator						
Operating frequency	$f_{16\text{-}17}$		61.5		MHz	3rd harmonic
Negative input impedance	$Z_{16\text{-}17}$		- 250		Ω	f = 61.5 MHz
Negative input impedance	$Z_{16\text{-}17}$		1.4		kΩ	f = 20.5 MHz
Input impedance crystal	R_{cr}			tbd	Ω	3rd harmonic
Spurious harmonics crystal	a_{sp}			- 20	dB	f < 200 MHz
Bus controlled adjust range	Δf_{adj}		± 40		ppm	see diagram SUB06h
Bus controlled output XTAL_DIV6	$V_{XTAL\_DIV6\_ON}$		500		mV_{pp}	f = 10.25 MHz, C_{load} = 10pF
	$V_{XTAL\_DIV6\_ON}$		1.5		V_{DC}	f = 10.25 MHz, C_{load} = 10pF
	$V_{XTAL\_DIV6\_OFF}$	60			dB	Signal supression f=10.25 MHz
	$V_{XTAL\_DIV6\_OFF}$			50	mV_{DC}	C_{load} = 10pF
Chargepump output PD_1, PD_0 (Loopfilter input)						
DC voltage	V_{PD_1} V_{PD_0}		2.5		V	locked
DC current	± $I_{PD\_1\_3}$ ± $I_{PD\_0\_3}$	3.2	4	4.8	mA	see Status, Subaddress 00H, bit D1, D2 $V_{PD\_0/1}$ = 2.5V
DC current	± $I_{PD\_1\_2}$ ± $I_{PD\_0\_2}$	1.6	2	2.4	mA	
DC current	± $I_{PD\_1\_1}$ ± $I_{PD\_0\_1}$	0.8	1	1.2	mA	
DC current	± $I_{PD\_1\_0}$ ± $I_{PD\_0\_0}$	400	500	600	uA	
Tristate output current	±$I_{PD\_1\_OFF}$ ±$I_{PD\_0\_OFF}$		0.1	10	nA	$V_{PD\_0/1}$ = 2.5V , guaranteed by design

Parameter T_A = 25 °C, V_{VCC} = 8.5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Loop amplifier tuningvoltage output (Loopfilter output)						
LOW output voltage	V_{PDA_L}	0	tbd.	400	mV	I_{TUNE} = 100 uA
HIGH output voltage	V_{PDA_H}	V_{VCC}-0.5V	tbd.	V_{CC}	mV	I_{TUNE} = -100 uA
HIGH output current source LOW output current source	I_{PDA_H} I_{PDA_L}		-2.4 -1.2		mA	V_{TUNE} = 4V, V_{PD_1} = 0V, V_{PD_0} = 0V (see Status, Subaddress 00H, bit D11)
IF_Counter						
input sensitivity AM	v_{IF_1}	50	tbd.		mV	f_{IF_1} = 440...471kHz
input impedance AM	Z_{IF_1}		180		kΩ	f_{IF_1} = 455kHz
input sensitivity FM	v_{IF_0}	50	tbd.		mV	f_{IF_0} = 10.60...10.80MHz
input impedance FM	Z_{IF_0}		10		kΩ	f_{IF_0} = 10.70MHz
PLL for synthesizer (see PLL Synthesizer on page 16)						
PLL / VCO step size (programmable via R-counter)	f_{ref}	6.25		100	kHz	$f_{crystal}$ = 61.5 MHz
N-counter divide ratio	N	2		65535		16-Bit
R-counter divide ratio	R	2		65535		16-Bit
input sensitivity	v_{VCO}	50	tbd.		mV	f_{VCO} = 70...120MHz
input impedance	Z_{VCO}		2.5		kΩ	f_{VCO} = 120MHz
ADC converter ADC_IN1 / IN2						
input voltage range	$v_{ADC\_IN1/2}$	0		VREFD5V	V	tbd.
Sampling capacitance	C_S		5		pF	
least significant bit	v_{LSB}		39, 37		mV	
zero offsetfailure	V_{ZERO}		tbd.		mV	
full scale	V_{FS}	tbd.	VREFD5V	tbd.	V	
nonlinearity	ΔV			+/-1.5	LSB	
coverting time for both cannels	f_{CONV}		32		us	
DAC_7 converter PORT_7BIT						
output voltage range	V_{PORT_7BIT}	0		5,40	V	tbd.
least significant bit	V_{LSB}		39.37		mV	
zero offsetfailure	V_{ZERO}		tbd.		mV	
full scale	V_{FS}	tbd.	VREFD5V	tbd.	V	
nonlinearity	ΔV			+/-1.5	LSB	
output current	I_{PORT_7BIT}			50	uA	
output capacitance	C_{PORT_7BIT}			10	pF	

Parameter T_A = 25 °C,V_{VCC} = 8.5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
DAC_4 converter PORT_4BIT						tbd.
output voltage range	V_{PORT_7BIT}	0		5,40	V	
least significant bit	V_{LSB}		333.33		mV	
zero offsetfailure	V_{ZERO}		tbd.		mV	
full scale	V_{FS}	tbd.	VREFD5V	tbd.	V	
nonlinearity	ΔV			+/-1.5	LSB	
output current	I_{PORT_4BIT}			50	uA	
output capacitance	C_{PORT_4BIT}			10	pF	
Port outputs, PORT1, PORT2_STEREO, IFC_SD (see Output / input Ports on page 14)						
LOW output voltage	V_P	0	100	400	mV	I_P = 1 mA
HIGH Leackage current	I_{P_LEACK}	0		100	nA	V_P = 5 V
I2C / 3-Wire-bus (BUS_MODE, SCL, SDA, BUS_ENA) (see I2C Bus Timing on page 27 and Bus Data Format on page 19)						
H-input voltage	V_{IH}	2.10		5.50	V	
L-input voltage	V_{IL}	-0.5		0.90	V	
Hysteresis of Schmitt trigger inputs (BUS_MODE, SCL, SDA, BUS_ENA)	V_{hys}		0.30		V	
Input capacity	C_I			5	pF	

8 Package Outlines

P-TSSOP-28
(Plastic Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side