FAIRCHILD SEMICONDUCTOR®

January 2004

FDC699P

P-Channel 2.5V PowerTrench® MOSFET

General Description

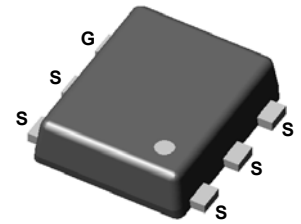
This P-Channel 2.5V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 12V).

Applications

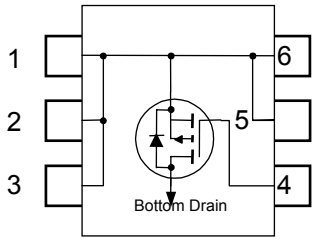
- Battery management
- Load Switch
- Battery protection

Features

- –7 A, –20 V $R_{DS(ON)}$ = 22 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 30 mΩ @ V_{GS} = –2.5 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- Fast switching speed
- FLMP SuperSOT-6 package: Enhanced thermal performance in industry-standard package size



SuperSOT-6™ FLMP



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Drain Current – Continuous	(Note 1a)	–7	A
	– Pulsed		–40	
P_D	Power Dissipation	(Note 1a)	2	W
		(Note 1b)	1.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	60	°C/W
		(Note 1b)	111	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		0.5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.699	FDC699P	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = – 250 μA, Referenced to 25°C		–12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V			–1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.6	–0.9	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = – 250 μA, Referenced to 25°C		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –7 A V_{GS} = –2.5 V, I_D = –6 A V_{GS} = –4.5 V, I_D = –7 A, T_J =125°C		14 21 17	22 30 31	mΩ
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –7 A		30		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = – 10 V, V_{GS} = 0 V, f = 1.0 MHz		2640		pF
C_{oss}	Output Capacitance			560		pF
C_{rss}	Reverse Transfer Capacitance			280		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		3.6		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω		16	28	ns
t_r	Turn–On Rise Time			11	19	ns
$t_{d(off)}$	Turn–Off Delay Time			75	120	ns
t_f	Turn–Off Fall Time			41	65	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –7 A, V_{GS} = –5 V		27	38	nC
Q_{gs}	Gate–Source Charge			5		nC
Q_{gd}	Gate–Drain Charge			7		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.6	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.6 A (Note 2)		–0.7	–1.2	V
t_{rr}	Reverse Recovery Time	I_F = –7 A, d_{iF}/d_t = 100 A/μs		28		ns
Q_{rr}	Reverse Recovery Charge			14		nC

Notes: 1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

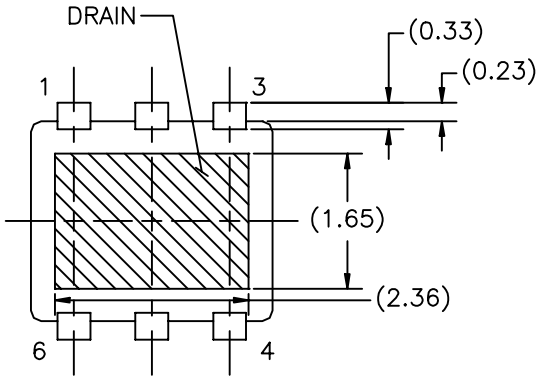
a) 60°C/W when mounted on a 1in^2 pad of 2 oz copper

b) 111°C/W when mounted on a minimum pad of 2 oz copper

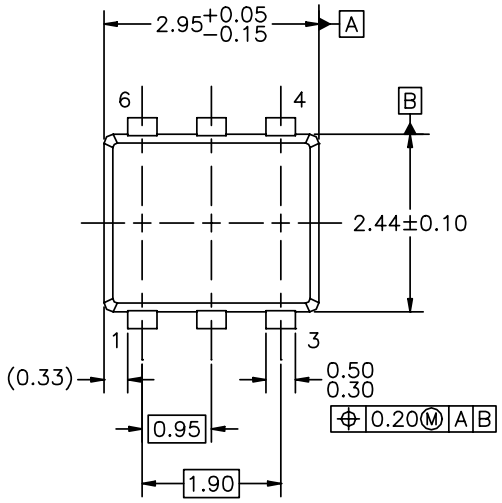
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

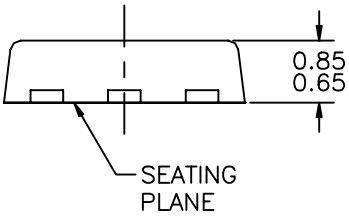
Dimensional Outline and Pad Layout

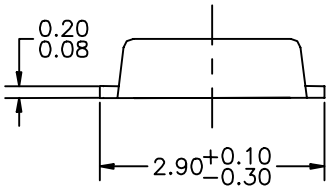


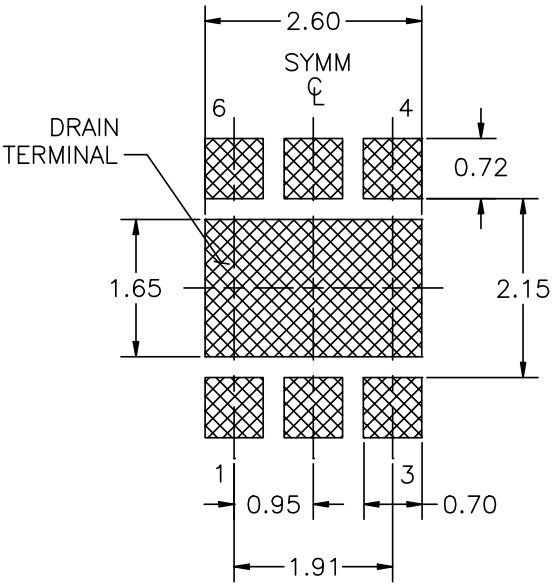
Bottom View



Top View







Recommended Landing Pattern

Typical Characteristics

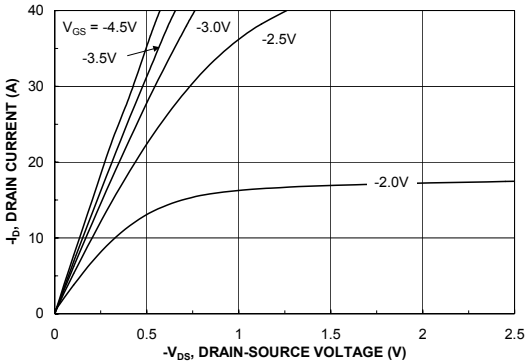


Figure 1. On-Region Characteristics.

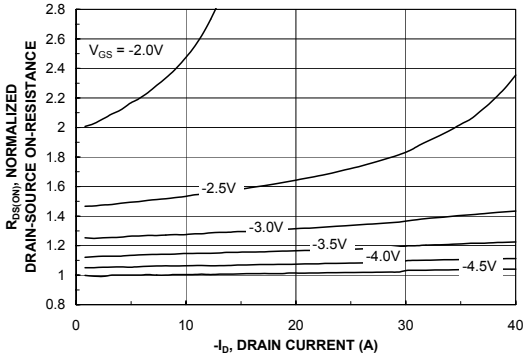


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

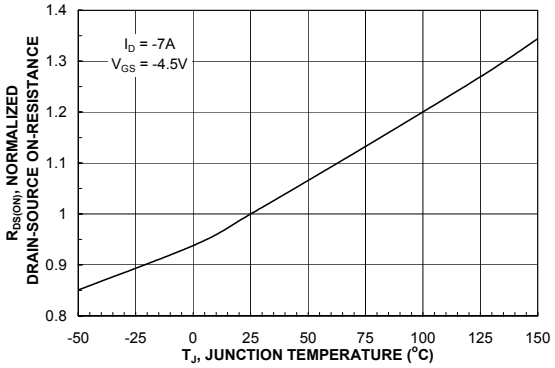


Figure 3. On-Resistance Variation withTemperature.

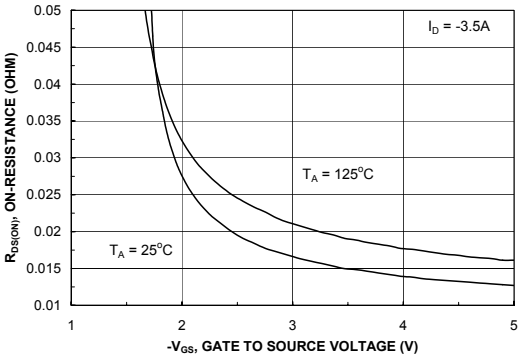


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

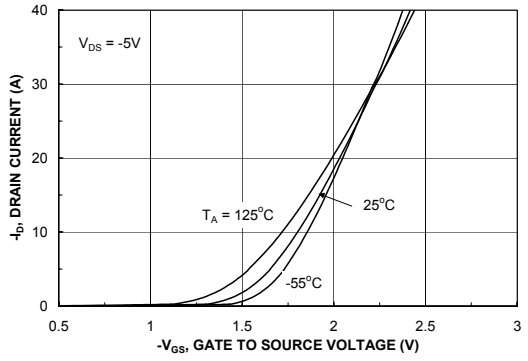


Figure 5. Transfer Characteristics.

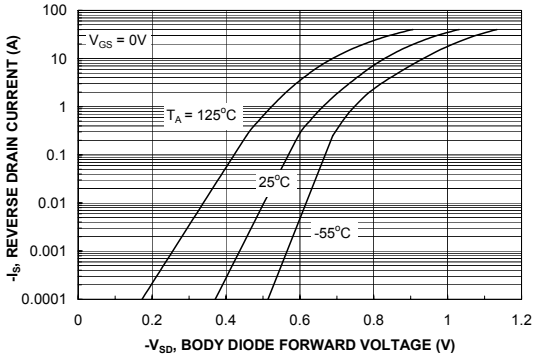


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

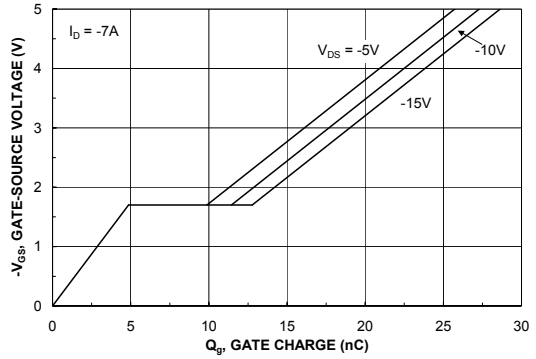


Figure 7. Gate Charge Characteristics.

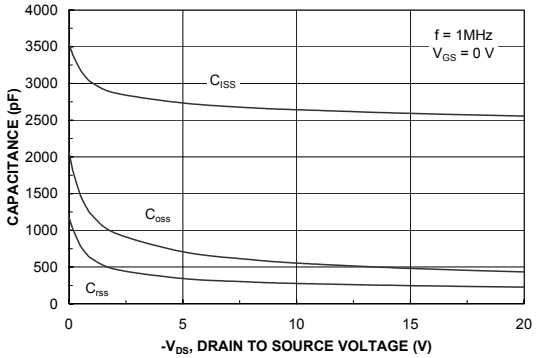


Figure 8. Capacitance Characteristics.

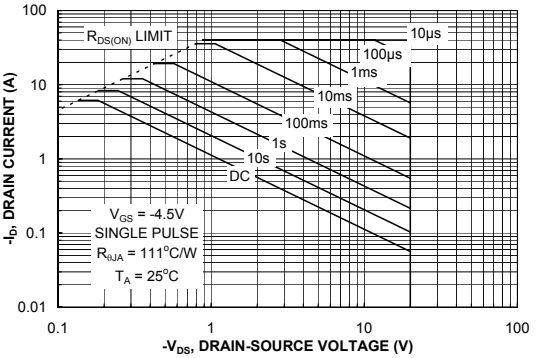


Figure 9. Maximum Safe Operating Area.

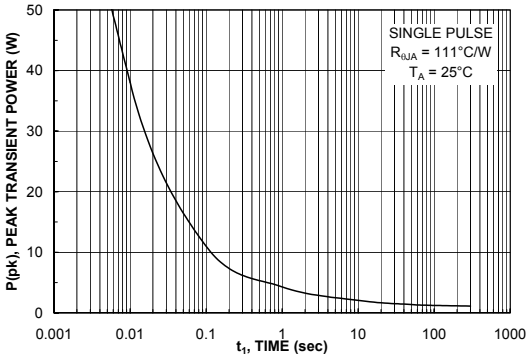


Figure 10. Single Pulse Maximum Power Dissipation.

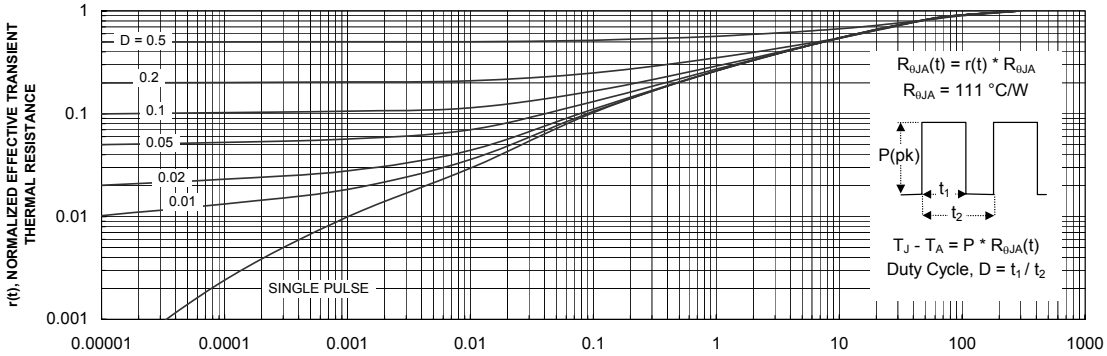


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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FDC699P

P-Channel 2.5V Power Mosfet MOSFET Recommend FDC699P_F077

Contents

General description

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Applications

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- Load Switch
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Product status/pricing/packaging BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
FDC699P	Not recommended for new designs		$0.45	SSOT-6 FLMP	6	TAPE REEL	Line 1: &E&**Y** (Binary Calendar Year Coding) Line 2: .699
FDC699P_F077	Full Production	Full Production	$0.57	SSOT-6 FLMP	6	TAPE REEL	Line 1: &E&**Y** (Binary Calendar Year Coding) Line 2: .699

* Fairchild 1,000 piece Budgetary Pricing
** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a Fairchild distributor to obtain samples

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product FDC699P is available. Click here for more information .

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Models

Package & leads	Condition	Temperature range	Software version	Revision date
PSPICE				
SSOT-6 FLMP-6	Electrical	25°C to 125°C	Orcad 9.1	Jan 6, 2004

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Qualification Support

Click on a product for detailed qualification data

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