CXD2507AQ

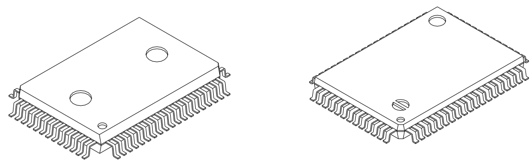
CD Digital Signal Processor

Description

The CXD2507AQ is a digital signal processor for CD players and is equipped with the following functions.

64 pin QFP (Plastic)

-L01 -L121



Features

- Digital PLL
- EFM frame sync protection
- SEC strategy-based error correction
- Subcode demodulation, CRC checking
- Digital spindle servo
- Servo auto-sequencer
- Asymmetry compensation circuit
- Digital audio interface output
- 16K RAM
- Double-speed playback capability
- New microcomputer interface circuit

Absolute Maximum Ratings

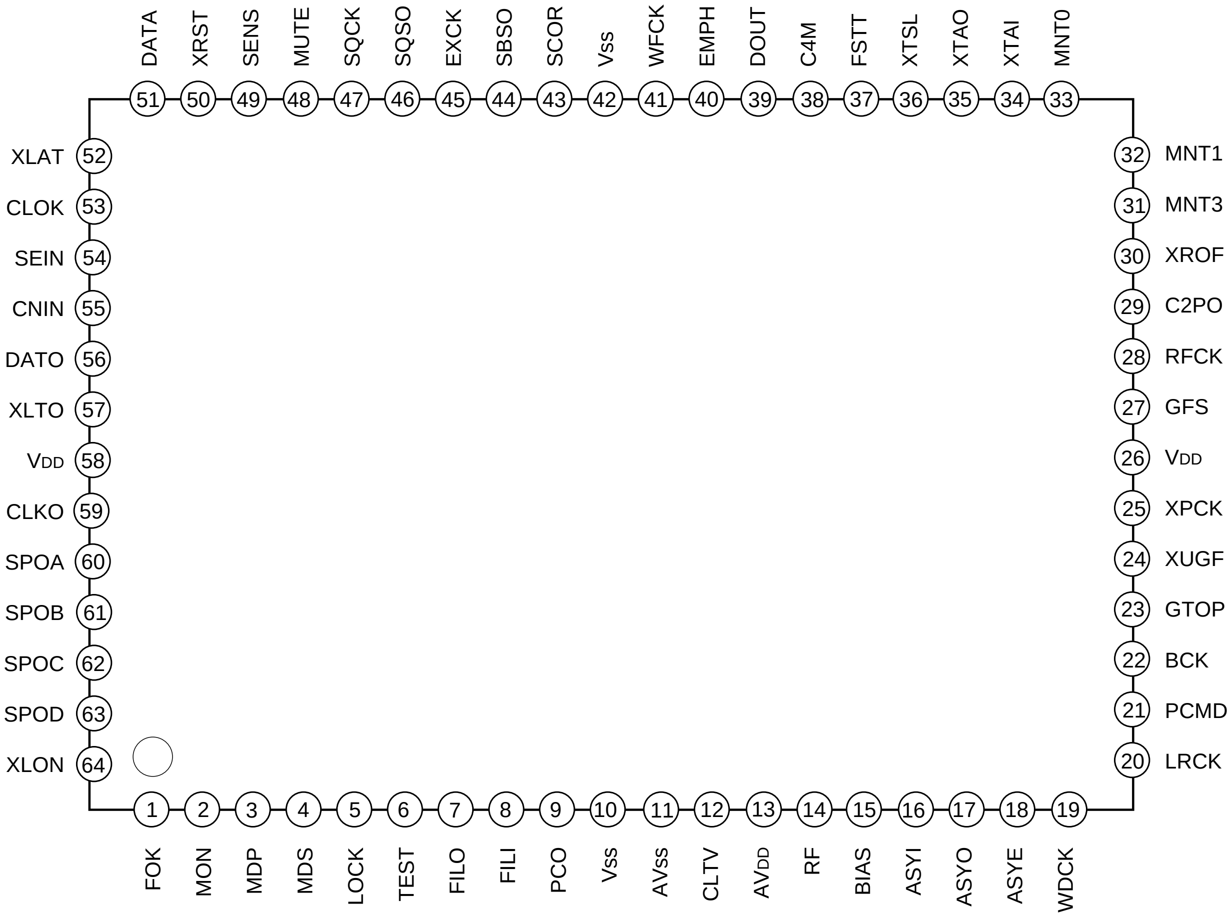
• Supply voltage	V_{DD}	–0.3 to +7.0	V
• Supply voltage variation	$V_{SS} – AV_{SS}$	–0.3 to +0.3	V
	$V_{DD} – AV_{DD}$	–0.3 to +0.3	V
• Input voltage	V_I	–0.3 to +7.0	V
	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage	V_O	–0.3 to +7.0	V
• Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Conditions

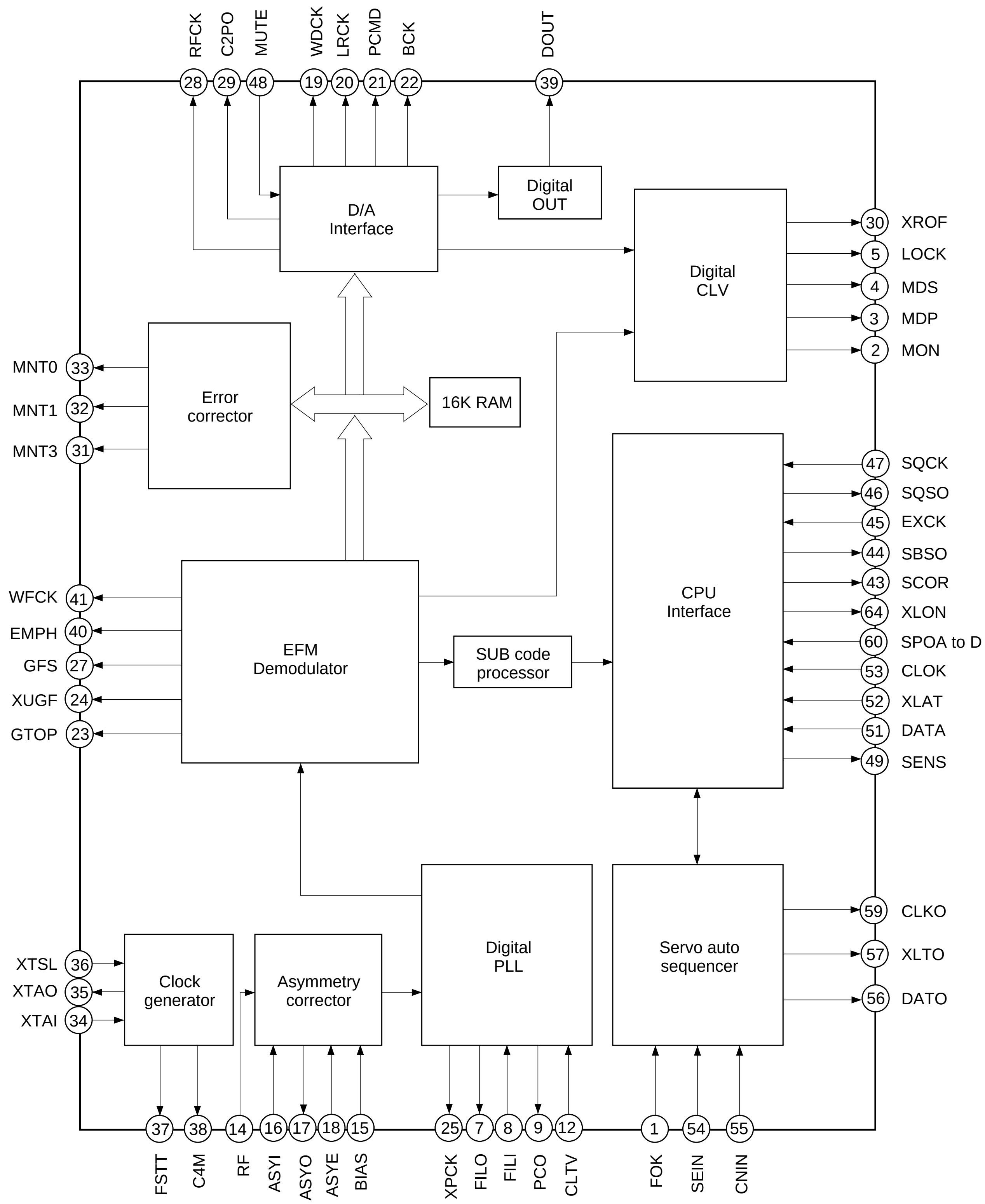
• Supply voltage	V_{DD}	4.5 to 5.5V (double-speed playback)		
		3.5 to 5.5V (normal-speed playback)		
		3.0 to 5.5V (low power consumption, special playback mode) *		
• Operating temperature	Topr	–20 (min.)	75 (max.)	°C

* When the internal operation of the LSI is set to double-speed mode and the crystal oscillation frequency is halved, normal-speed playback results.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O		Description
1	FOK	I		Focus OK input. Used for SENS output and the servo auto sequencer.
2	MON	O	1, 0	Spindle motor on/off control output.
3	MDP	O	1, Z, 0	Spindle motor servo control.
4	MDS	O	1, Z, 0	Spindle motor servo control.
5	LOCK	O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
6	TEST	I		TEST pin. Normally GND.
7	FILO	O	Analog	Master PLL (slave = digital PLL) filter output.
8	FILI	I		Master PLL filter input.
9	PCO	O	1, Z, 0	Master PLL charge pump output.
10	V_{SS}	—	—	GND.
11	AV_{SS}	—	—	Analog GND.
12	CLTV	I		Master VCO control voltage input.
13	AV_{DD}	—	—	Analog power supply (+5V).
14	RF	I		EFM signal input.
15	BIAS	I		Constant current input of asymmetry circuit.
16	ASYI	I		Asymmetry comparator voltage input.
17	ASYO	O	1, 0	EFM full-swing output (low = Vss, high = V_{DD}).
18	ASYE	I		Low: asymmetry circuit off; high: asymmetry circuit on.
19	WDCK	O	1, 0	D/A interface. Word clock f = 2Fs.
20	LRCK	O	1, 0	D/A interface. LR clock f = Fs.
21	PCMD	O	1, 0	D/A interface. Serial data (two's complement, MSB first).
22	BCK	O	1, 0	D/A interface. Bit clock.
23	GTOP	O	1, 0	GTOP output.
24	XUGF	O	1, 0	XUGF output.
25	XPCK	O	1, 0	XPLCK output.
26	V_{DD}	—	—	Power supply (+5V).
27	GFS	O	1, 0	GFS output.
28	RFCK	O	1, 0	RFCK output.
29	C2PO	O	1, 0	C2PO output.
30	XROF	O	1, 0	XRAOF output.
31	MNT3	O	1, 0	MNT3 output.
32	MNT1	O	1, 0	MNT1 output.
33	MNT0	O	1, 0	MNT0 output.
34	XTAI	I		16.9344MHz crystal oscillation circuit input, or 33.8688MHz input.
35	XTAO	O	1, 0	16.9344MHz crystal oscillation circuit output.
36	XTSL	I		Crystal selection input. Set low when the crystal is 16.9344MHz, high when 33.8688MHz.

Pin No.	Symbol	I/O		Description
37	FSTT	O	1, 0	2/3 frequency divider output for Pins 34 and 35.
38	C4M	O	1, 0	4.2336MHz output.
39	DOUT	O	1, 0	Digital Out output.
40	EMPH	O	1, 0	Outputs high signal when the playback disc has emphasis, low signal when no emphasis.
41	WFCK	O	1, 0	WFCK output.
42	V_{SS}	—	—	GND.
43	SCOR	O	1, 0	Outputs high signal when either subcode sync S0 or S1 is detected.
44	SBSO	O	1, 0	Sub P to W serial output.
45	EXCK	I		SBSO readout clock input.
46	SQSO	O	1, 0	SubQ 80-bit serial output.
47	SQCK	I		SQSO readout clock input.
48	MUTE	I		High: mute; low: release
49	SENS	O	1, 0	SENS output to CPU.
50	XRST	I		System reset. Reset when low.
51	DATA	I		Serial data input from CPU.
52	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
53	CLOK	I		Serial data transfer clock input from CPU.
54	SEIN	I		Sense input from SSP.
55	CNIN	I		Track jump count signal input.
56	DATO	O	1, 0	Serial data output to SSP.
57	XLTO	O	1, 0	Serial data latch output to SSP. Latched at the falling edge.
58	V_{DD}	—	—	Power supply (+5V).
59	CLKO	O	1, 0	Serial data transfer clock output to SSP.
60	SPOA	I		Microcomputer extended interface (input A).
61	SPOB	I		Microcomputer extended interface (input B).
62	SPOC	I		Microcomputer extended interface (input C).
63	SPOD	I		Microcomputer extended interface (input D).
64	XLON	O	1, 0	Microcomputer extended interface (output).

Notes)
- PCMD is two's complement output of MSB first.
- GTOP is used to monitor the frame sync protection status.
- XUGF is the negative pulse for the frame sync derived from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy. This signal has a cycle of 136µ.
- C2PO represents the data error status.
- XRAOF is generated when the 16K RAM exceeds the ±4F jitter margin.

Electrical Characteristics

DC Characteristics

($V_{DD} = AV_{DD} = 5.0V \pm 5\%$, $V_{SS} = AV_{SS} = 0V$, Topr = –20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		$0.7V_{DD}$			V	*1
	Low level input voltage	V_{IL} (1)				$0.3V_{DD}$	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	$0.8V_{DD}$			V	*2
	Low level input voltage	V_{IL} (2)				$0.2V_{DD}$	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	V_{SS}		V_{DD}	V	*3
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –4mA	V_{DD} – 0.8		V_{DD}	V	*4
	Low level output voltage	V_{OL} (1)	I_{OL} = 4mA	0		0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –2mA	V_{DD} – 0.8		V_{DD}	V	*5
	Low level output voltage	V_{OL} (2)	I_{OL} = 4mA	0		0.4	V	
Output voltage (3)	High level output voltage	V_{OH} (4)	I_{OH} = –0.28mA	V_{DD} – 0.5		V_{DD}	V	*6
	Low level output voltage	V_{OL} (4)	I_{OL} = 0.36mA	0		0.4	V	
Input leak current		I_{LI}	V_I = 0 to 5.25V			±5	µA	*1, *2, *3
Tri-state pin output leak current		I_{LO}	V_O = 0 to 5.25V			±5	µA	*7

Applicable pins

*1 XTSL, DATA, XLAT

*2 CLOK, XRST, EXCK, SQCK, MUTE, FOK, SEIN, CNIN, ASYE

*3 CLTV, FILI, RF

*4 MDP, PCO

*5 ASYO, DOUT, FSTT, C4M, C16M, SBSO, SQSO, SCOR, EMPH, MON, LOCK, WDCK, DATO, CLKO, XLTO, SENS, MDS, LRCK, WFCK, PCMD, BCK, GTOP, XUGF, XPCK, GFS, RFCK, XROF, MNT0, MNT1, MNT3

*6 FILO

*7 MDS, MDP, PCO

AC Characteristics

1) XTAI and VCOI pins

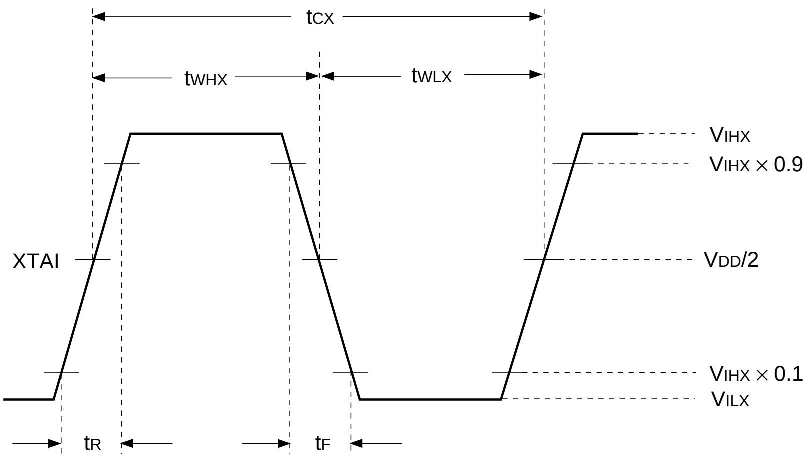
(1) When using self-oscillation (Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(2) When inputting pulses to XTAI and VCOI

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1,000	ns
Input high level	V_{IHX}	V_{DD} – 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



(3) When inputting sine waves to XTAI and VCOI pins via a capacitor

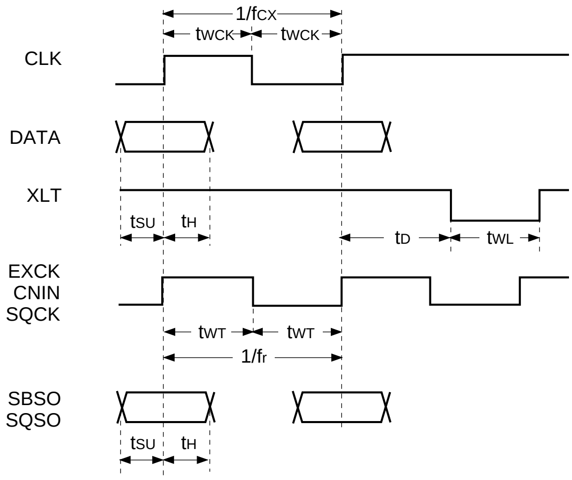
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_1	2.0		V_{DD} + 0.3	Vp-p

2) CLOK, DATA, XLAT, CNIN, SQCK EXCK pins

($V_{DD} = AV_{DD} = 5.0V \pm 5\%$, $V_{SS} = AV_{SS} = 0V$, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65*	MHz
EXCK SQCK pulse width	t_{WT}	750*			ns



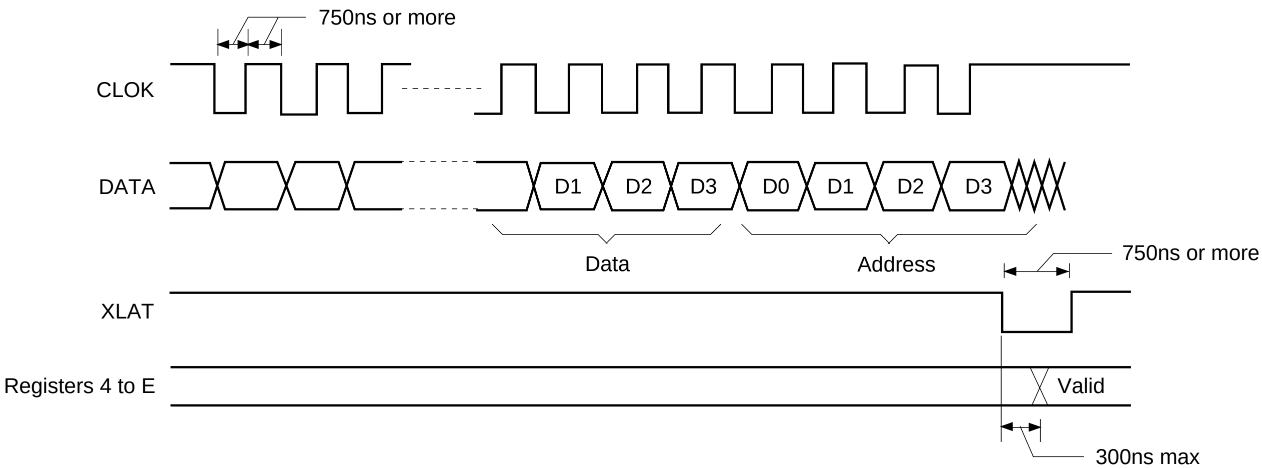
* In low power consumption and special playback mode, when SL0 = SL1 = 1, the maximum operating frequency for SQCK is 300kHz and the minimum pulse width is 1.5µs.

Description of Functions

1. CPU Interface and Instructions

• CPU interface

This interface uses DATA, CLOK, and XLAT to set the modes. The interface timing chart is shown below.



• Information on each address and the data is provided in Table 1-1.

• The internal registers are initialized by a reset when XRST = 0; the initialization data is shown in Table 1-2.

Note) When XLAT is low, EXCK and SQCK must be set high.

CD2507 Command Table

Register name	Command	Address D3	Address D2	Address D1	Address D0	Data 1 D3	Data 1 D2	Data 1 D1	Data 1 D0	Data 2 D3	Data 2 D2	Data 2 D1	Data 2 D0	Data 3 D3	Data 3 D2	Data 3 D1	Data 3 D0	Data 4 D3	Data 4 D2	Data 4 D1	Data 4 D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C)	0	1	0	1	0.18ms	0.09ms	0.05ms	0.02ms	—	—	—	—	—	—	—	—	—	—	—	—
	Brake (B)					0.36ms	0.18ms	0.09ms	0.05ms												
6	KICK (D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CD-ROM	DOUT MUTE	DOUT ON/OFF	WSEL	—	—	—	—	—	—	—	—	—	—	—	—
9	Function specification	1	0	0	1	0	DSPB ON/OFF	0	0	0	0	0	0	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	—	—	—	—	—	—	—	—	—	—	—	—
B	Serial bus CTRL	1	0	1	1	SL1	SL0	CPUSR	0	—	—	—	—	—	—	—	—	—	—	—	—
C	Servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	DCLV PWMmod	TB	TP	CLVS Gain	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	—	—	—	—	—	—	—	—	—	—	—	—
F	TEST mode	1	1	1	1	Don't Use				—	—	—	—	—	—	—	—	—	—	—	—

Values shown as "0" in the above table must be sent as "0".

Table 1-1

CXD2507 Reset Initialization

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C) Brake (B)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—
6	KICK (D)	0	1	1	0	0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequencer (N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—
9	Function specification	1	0	0	1	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—
B	Serial bus CTRL	1	0	1	1	0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—
C	Servo coefficient setting	1	1	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
F	TEST mode	1	1	1	1	Don't Use				—	—	—	—	—	—	—	—	—	—	—	—

Table 1-2

1-1. The meaning of the data for each address is explained below.

$4X commands

Command	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS-ON	0	1	1	1
1 TRACK JUMP	1	0	0	RXF
10 TRACK JUMP	1	0	1	RXF
2N TRACK JUMP	1	1	0	RXF
N TRACK MOVE	1	1	1	RXF

RXF = 0 FORWARD
RXF = 1 REVERSE

- When the FOCUS-ON command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the TRACK JUMP/MOVE commands ($48 to $4F) are canceled, $25 is sent and the auto sequence is interrupted.

$5X commands

Auto sequence timer setting

Setting timers: A, E, C, B

Command	D3	D2	D1	D0
Blind (A, E), Over flow (C)	0.18ms	0.09ms	0.05ms	0.02ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.05ms

Ex.) D2 = D0 = 1, D3 = D1 = 0 (Initial reset)
A = E = C = 0.11ms
B = 0.23ms

$6X commands

Auto sequence timer setting

Setting timer: D

Command	D3	D2	D1	D0
KICK (D)	11.6ms	5.8ms	2.9ms	1.45ms

Ex.) D3 = 0, D2 = D1 = D0 = 1 (Initial reset)
D = 10.15ms

$7X commands

Auto sequence TRACK JUMP/MOVE count setting (N)

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set N when a 2N TRACK JUMP and an N TRACK MOVE are executed for auto sequence.

- The maximum track count is 65,535, but note that with 2N track jumps the maximum track jump count is determined by the mechanical limitations of the optical system.
- The number of track jump is counted according to the signals input from CNIN pin.

$8X commands

Command	D3	D2	D1	D0
MODE specification	CDROM	DOUT MUTE	DOUT ON-OFF	WSEL

Command bit	C2PO timing	Processing
CDROM = 1	1-3	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	1-3	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT MUTE = 1	Digital out output is muted. (DA output is not muted.)
DOUT MUTE = 0	When no other mute conditions are set, digital out is not muted.

Command bit	Processing
DOUT ON-OFF = 1	Digital out is output from the DOUT pin.
DOUT ON-OFF = 0	Digital out is not output from the DOUT pin.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock*	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

* In normal-speed playback, channel clock = 4.3218MHz.

$9X commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Function specifications	0	DSPB ON-OFF	0	0	0	0	0	0

Command bit	Processing
DSPB = 0	Normal-speed playback
DSPB = 1	Double-speed playback

$AX commands

Command	Data 1			
	D3	D2	D1	D0
Audio CTRL	0	0	Mute	ATT

Command bit	Meaning
Mute = 0	Mute off if other mute conditions are not set.
Mute = 1	Mute on.

Command bit	Meaning
ATT = 0	Attenuation off.
ATT = 1	–12dB

$BX commands

Command	D3	D2	D1	D0
Serial bus CTRL	SL1	SL0	CPUSR	0

This command switches the method of interfacing with the CPU. With the CDL500 Series, the number of signal lines between the CPU and the DSP can be reduced in comparison with the CDL40 Series. Also, the error rate can be measured with the CPU.

Command bits		Processing
SL1	SL0	
0	0	Same interface mode as the CDL40 Series.
0	1	SBSO is output from SQSO pin. In other words, subcodes P to W are read out from SQSO. Input the read clock to SQCK.
1	0	SENS is output from SQSO pin.
1	1	Each output signal is output from SQSO pin. Input the read clock to SQCK. (See to Timing Chart 1-4.)

Command bits	Processing
CPUSR = 1	XLON pin is high.
CPUSR = 0	XLON pin is low.

$CX commands

Command	D3	D2	D1	D0
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0
CLV CTRL ($DX)				Gain CLVS

• CLVS mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

• CLVP mode gain setting: GMDP, GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

$DX commands

Command	D3	D2	D1	D0
CLV CTRL	DCLV PWM MD	TB	TP	CLVS Gain

See the $CX command.

Command bit	Explanation (See Timing Chart 1-5.)
DCLV PWM MD = 1	CLV PWM mode specified. Both MDS and MDP are used.
DCLV PWM MD = 0	CLV PWM mode specified. Ternary MDP values are output.

Command bit	Explanation
TB = 0	Bottom hold in CLVS mode at cycle of RFCK/32
TB = 1	Bottom hold in CLVS mode at cycle of RFCK/16
TP = 0	Peak hold in CLVS mode at cycle of RFCK/4
TP = 1	Peak hold in CLVS mode at cycle of RFCK/2

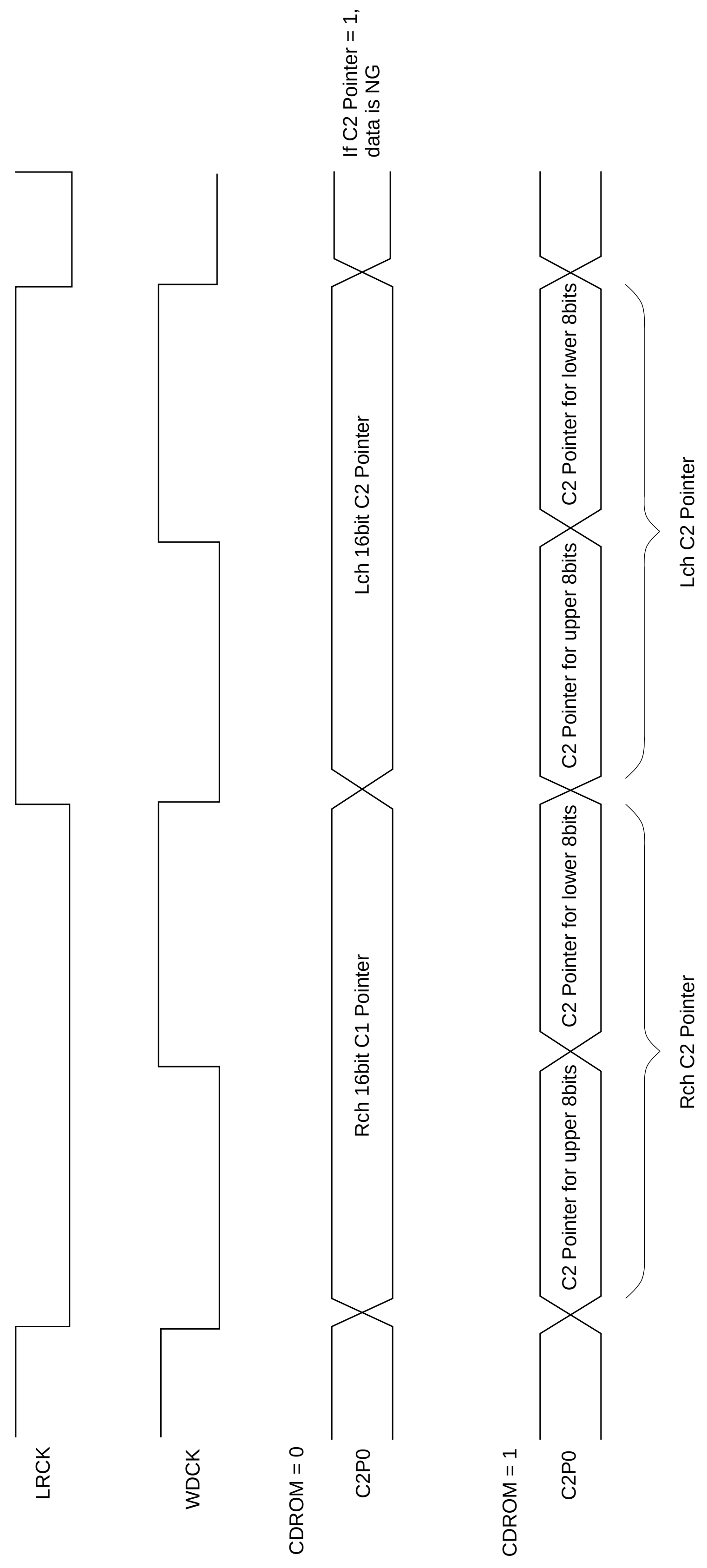
$EX commands

Command	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0

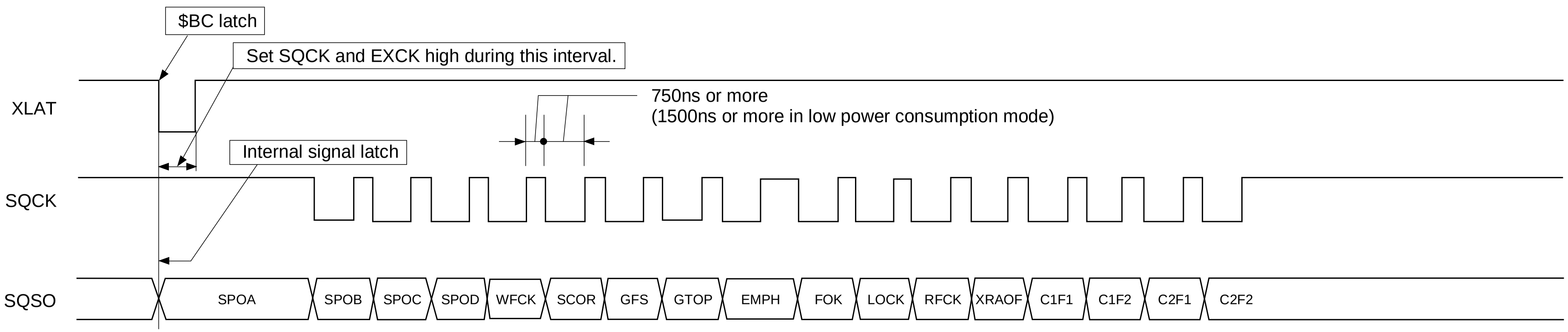
CM3	CM2	CM1	CM0	Mode	Explanation
0	0	0	0	STOP	See Timing Chart 1-6.
1	0	0	0	KICK	See Timing Chart 1-9.
1	0	1	0	BRAKE	See Timing Chart 1-8.
1	1	1	0	CLVS	
1	1	1	1	CLVP	
0	1	1	0	CLVA	

STOP : Spindle motor stop mode
KICK : Spindle motor forward rotation mode
BRAKE : Spindle motor reverse rotation mode
CLVS : Rough servo mode. When RF-PLL circuit lock is disengaged, this mode is used to pull the disc rotations within the RF-PLL capture range.
CLVP : PLL servo mode.
CLVA : Automatic CLVS/CLVP switching mode. This mode is normally used during playback.

Timing Chart 1-3



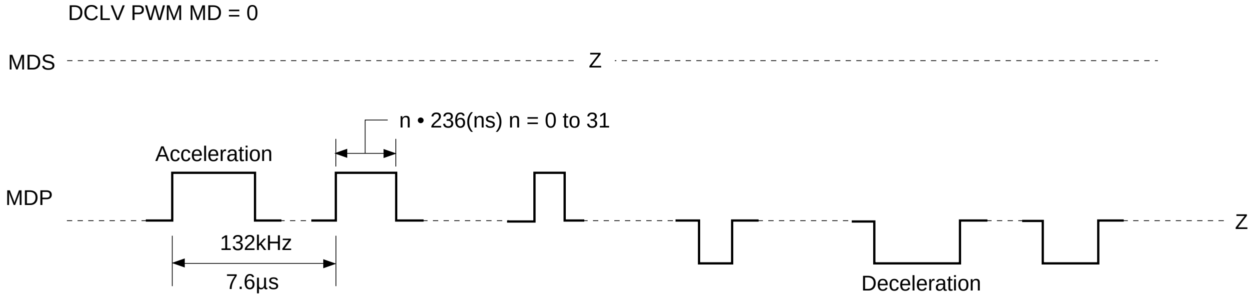
Timing Chart 1-4

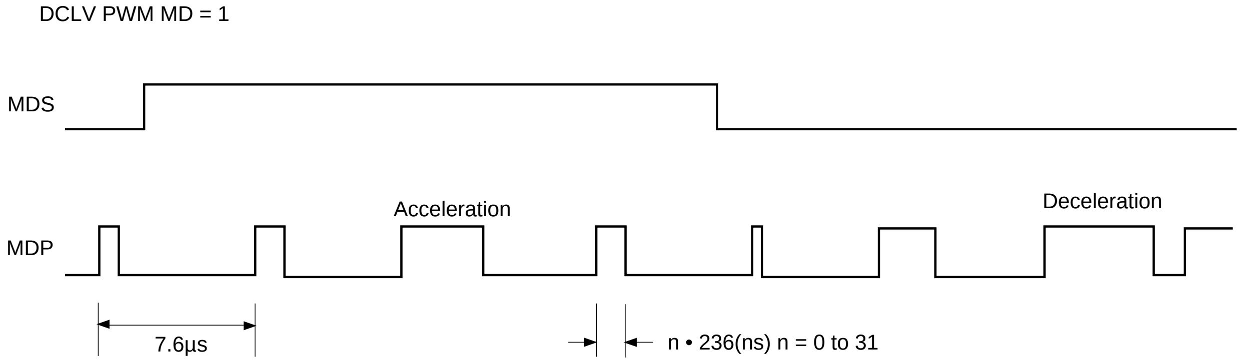


C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single error correction
1	1	Irretrievable error

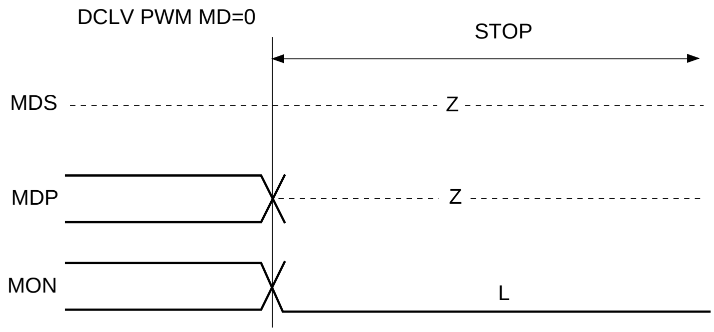
C2F1	C2F2	C2 correction status
0	0	No Error
1	0	Single error correction
1	1	Irretrievable error

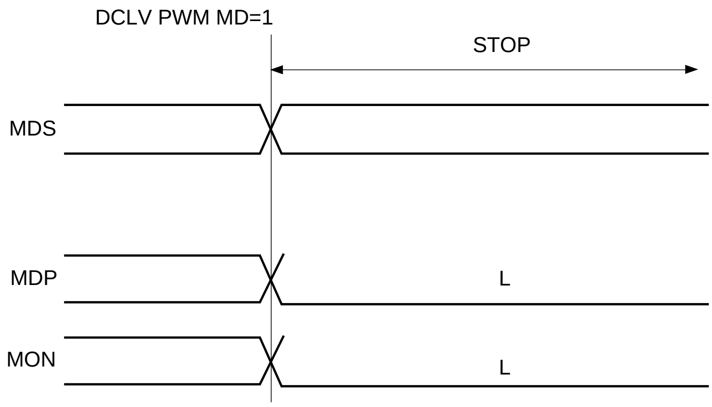
Timing Chart 1-5



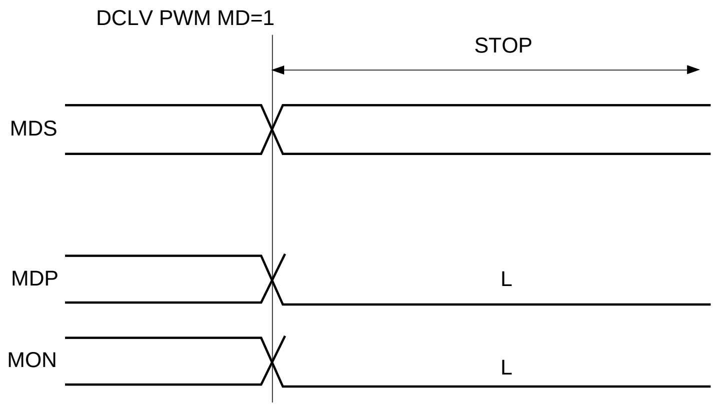


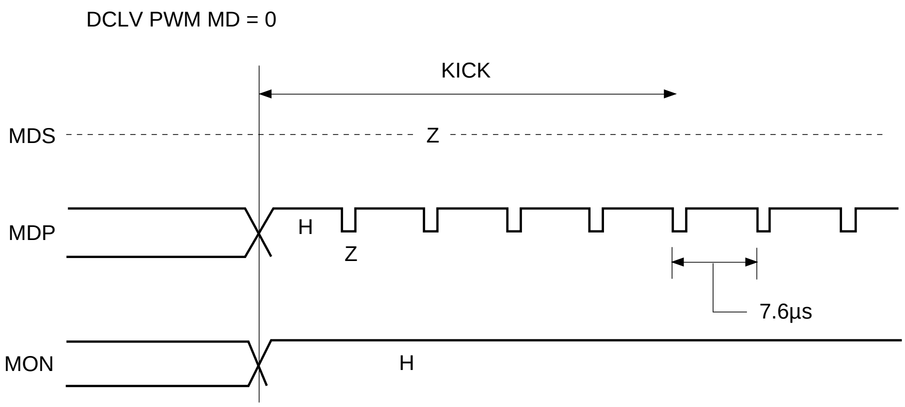
Timing Chart 1-6

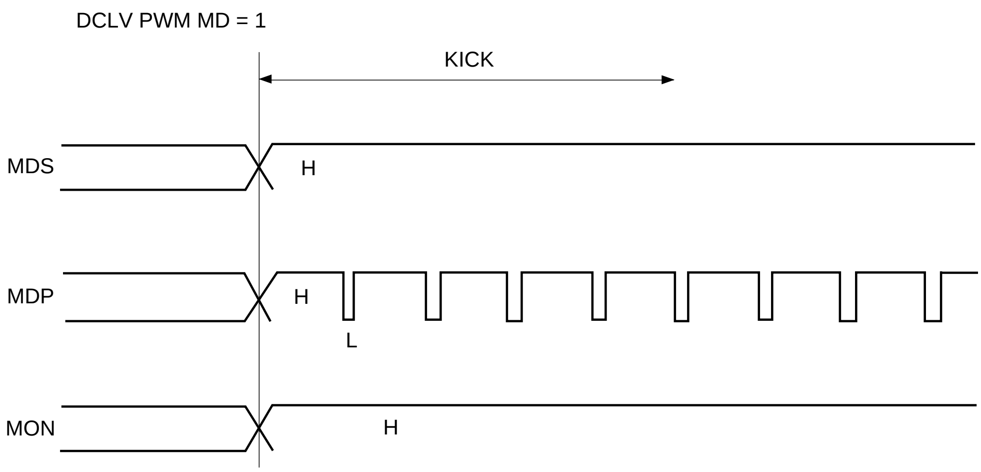




Timing Chart 1-7

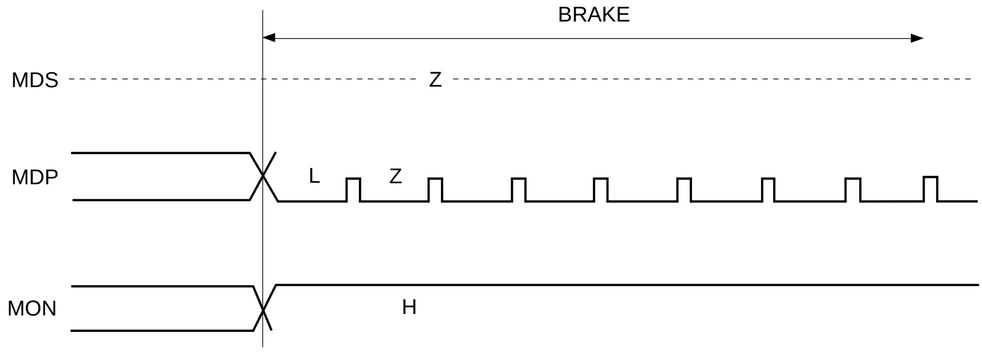




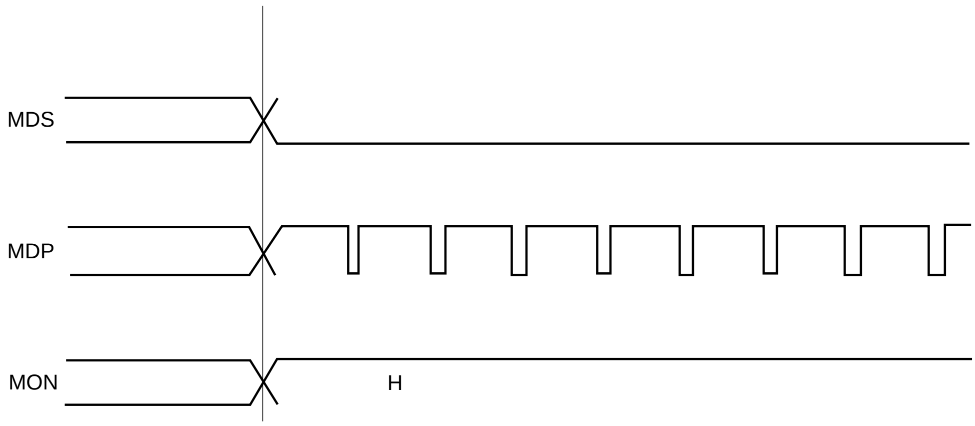


Timing Chart 1-8

DCLV PWM MD = 0



DCLV PWM MD = 1



1-2. Description of SENS Output

The following signals are output from SENS, depending on the microcomputer serial register value (latching not required).

Microcomputer serial register value (latching not required)	SENS output	Meaning
$0X, 1X, 2X, 3X	SEIN	SEIN, a signal input to the CXD2507 from the SSP, is output.
$4X	XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
$5X	FOK	Outputs the signal input to the FOK pin. Normally, FOK (from RF) is input. High for "focus OK".
$6X	SEIN	SEIN, a signal input to CXD2507 from the SSP, is output.
$AX	GFS	High when the played back frame sync is obtained with the correct timing.
$EX	$\overline{\text{OV64}}$	Low when the EFM signal, after passing through the sync detection filter, is lengthened by 64 channel clock pulses or more.
$7X, 8X, 9X, BX, CX, DX, FX	Low	The SENS pin is fixed low.

Note that the SENS output can be read from the SQSO pin when SL1=1 and SL0=0. (See the $BX commands.)

2. Subcode Interface

This section explains the subcode interface.

There are two methods for reading out a subcode externally. The 8-bit subcodes P to W can be read from SBSO by inputting EXCK to the CXD2507.

Sub Q can be read out after the CRC check of the 80 bits of information in the subcode frame. This accomplished, after checking SCOR and CRCF, by inputting 80 clock pulses to SQCK and reading data from SQSO pin.

2-1. P to W Subcode Read

Data can be read out by inputting EXCK immediately after WFCK falls. (See Fig. 2-1.)

Also, SBSO can be read out from SQSO pin when SL1 = 0 and SL0 = 1. (See the $BX commands.)

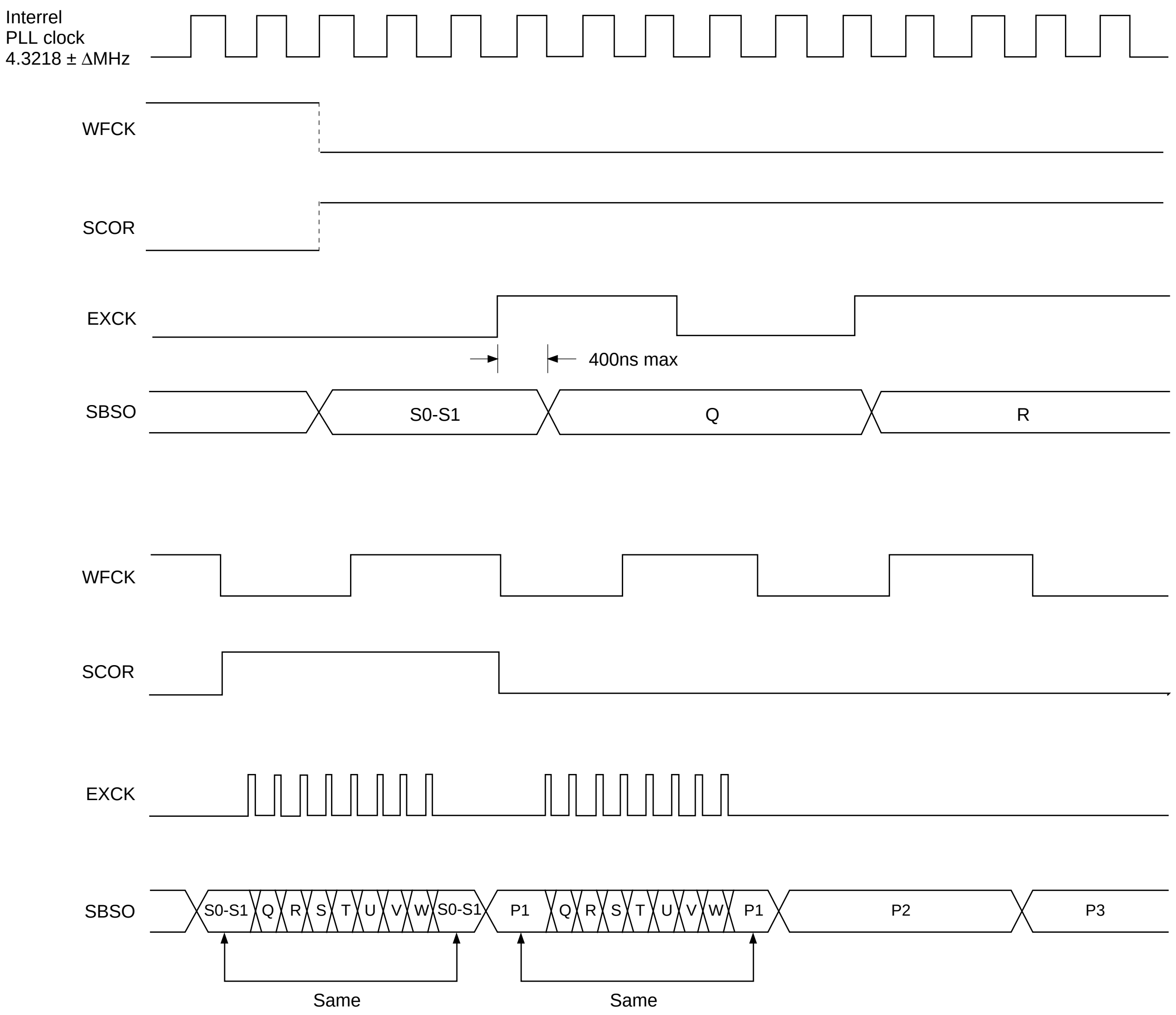
2-2. 80-bit Sub Q Read

Fig. 2-2 shows the peripheral block of the 80-bit Sub Q register.

- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, the 80 bits are loaded into the parallel/serial register.

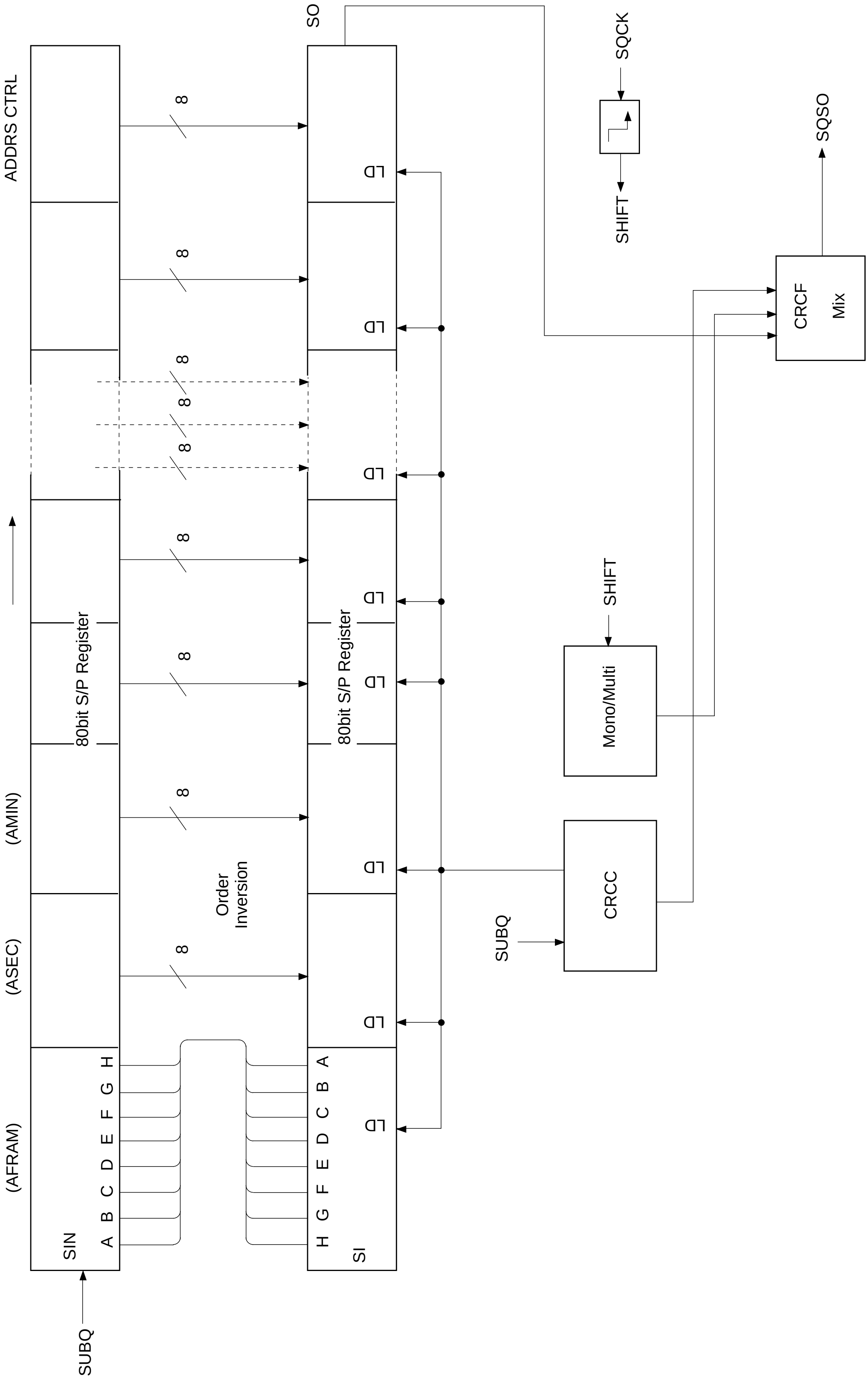
  When SQSO goes high 400µs or more later (monostable multivibrator time constant) after the subcode is read out, the CPU determines that new data (which passed the CRC check) has been loaded.
- In the CXD2507, when 80-bit data is loaded, the order of the MSB and LSB is inverted for each byte. As a result, although the sequence of bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the fact that the 80-bit data has been loaded is confirmed, SQCK is input so that the data can be read. In the CXD2507, the SQCK input is detected, and the retriggerable monostable multivibrator for low is reset.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration of SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the S/P register is not loaded into the P/S register.
- While the monostable multivibrator is being reset, data can not be loaded in the 80-bit parallel/serial register. In other words, while reading out with a clock cycle shorter than the monostable multivibrator time constant, the register will not be rewritten by CRCOK and others.
- Fig. 2-3 shows Timing Chart.
- Although a clock is input from SQCK pin to actually perform these operations, the high and low intervals for this clock should be between 750ns and 120µs.

Timing Chart 2-1

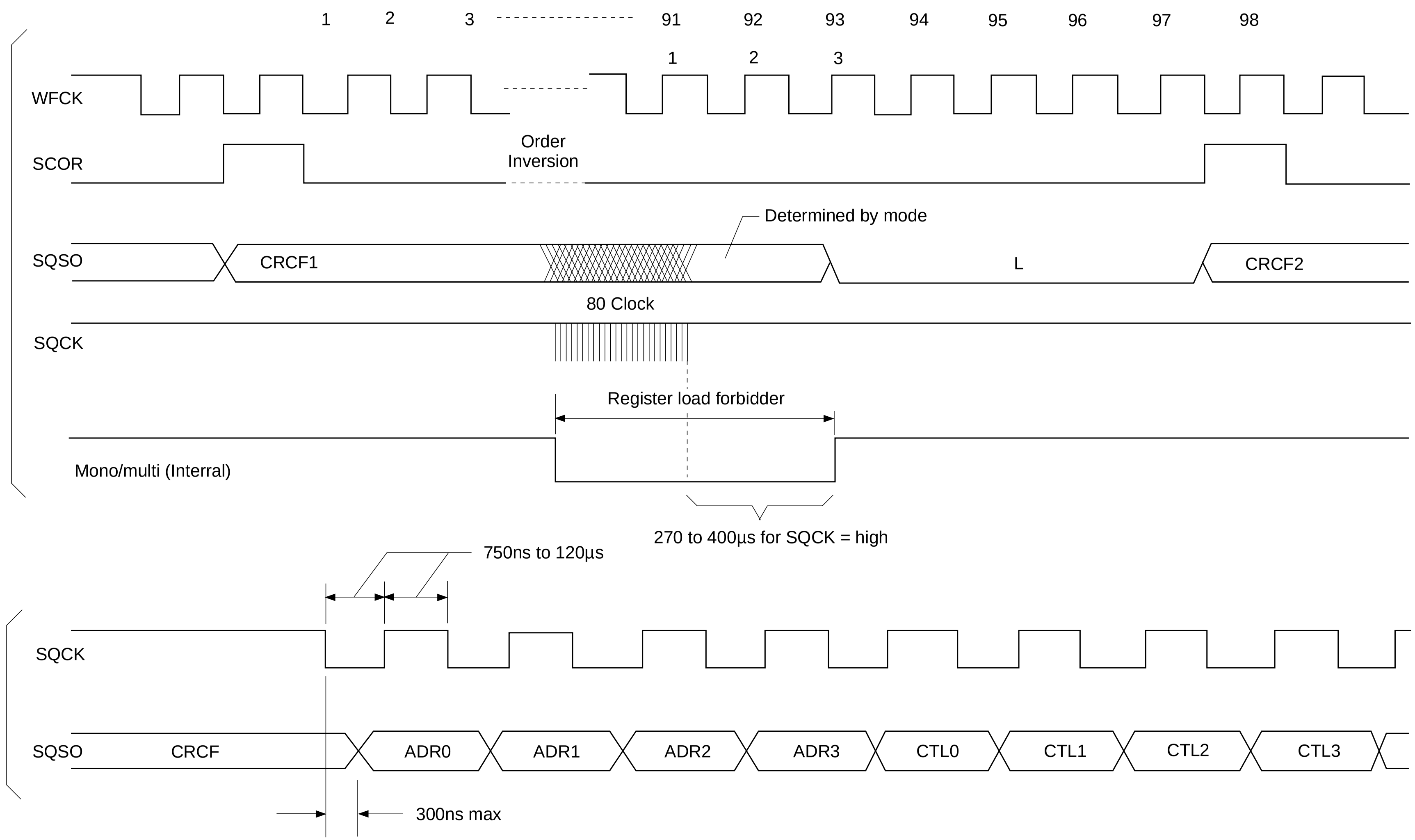


Subcode P.Q.R.S.T.U.V.W Read Timing

Block Diagram 2-2



Timing Chart 2-3



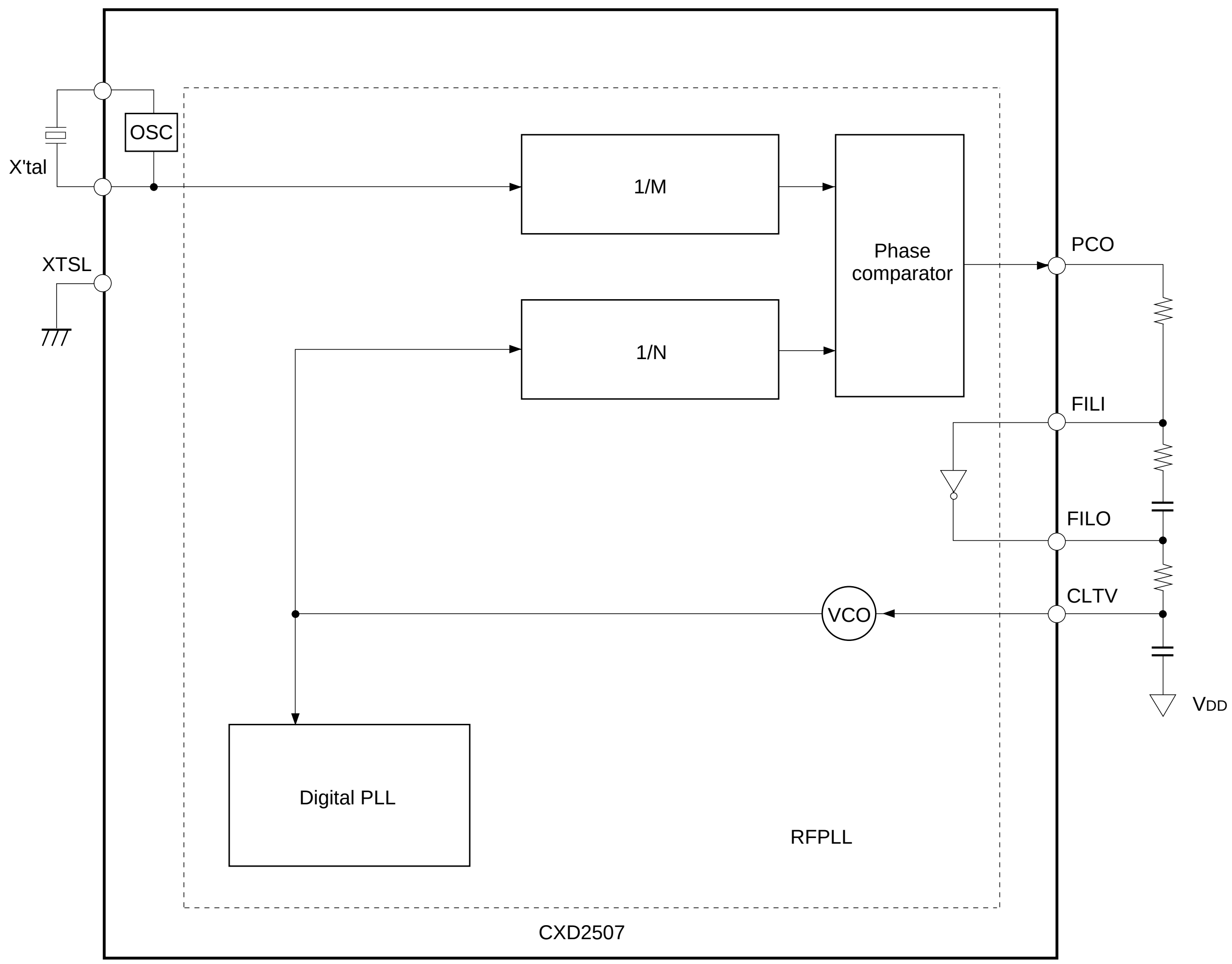
3. Description of Other Functions

3-1. Channel Clock Regeneration by Digital PLL Circuit

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system. Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is channel clock, is required.
  In an actual player, the fluctuation in the spindle rotation alters the width of the EFM signal pulses, making a PLL necessary for regenerating channel clock.

  The block diagram of this PLL is shown in Fig. 3-1.
  The CXD2507 has a built-in two-stage PLL as shown in the diagram.
- The first-stage PLL generates a high-frequency clock needed by the second-stage digital PLL.
- The second-stage PLL is a digital PLL that regenerates actual channel clock, and has a ±250kHz (normal state) or more capture range.

Block Diagram 3-1



3-2. Frame Sync Protection

- In a CD player operating at normal speed, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to know which data is the data within a frame.
  Conversely, if the frame sync can not be recognized, the data is processed as error data because it can not be recognized what the data is. As a result, recognizing the frame sync properly is extremely important for improving playability.

- There are two window widths: one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter is fixed to 3. In other words, when the frame sync is being played back normally and then can not be detected due to scratches, a maximum of 13 frames are inserted. If frame sync can not be detected for 13 frames or more, the window is released and the frame sync is resynchronized.
  In addition, immediately after the window is released and resynchronization is executed, if a proper frame sync can not be detected within 3 frames, the window is released immediately.

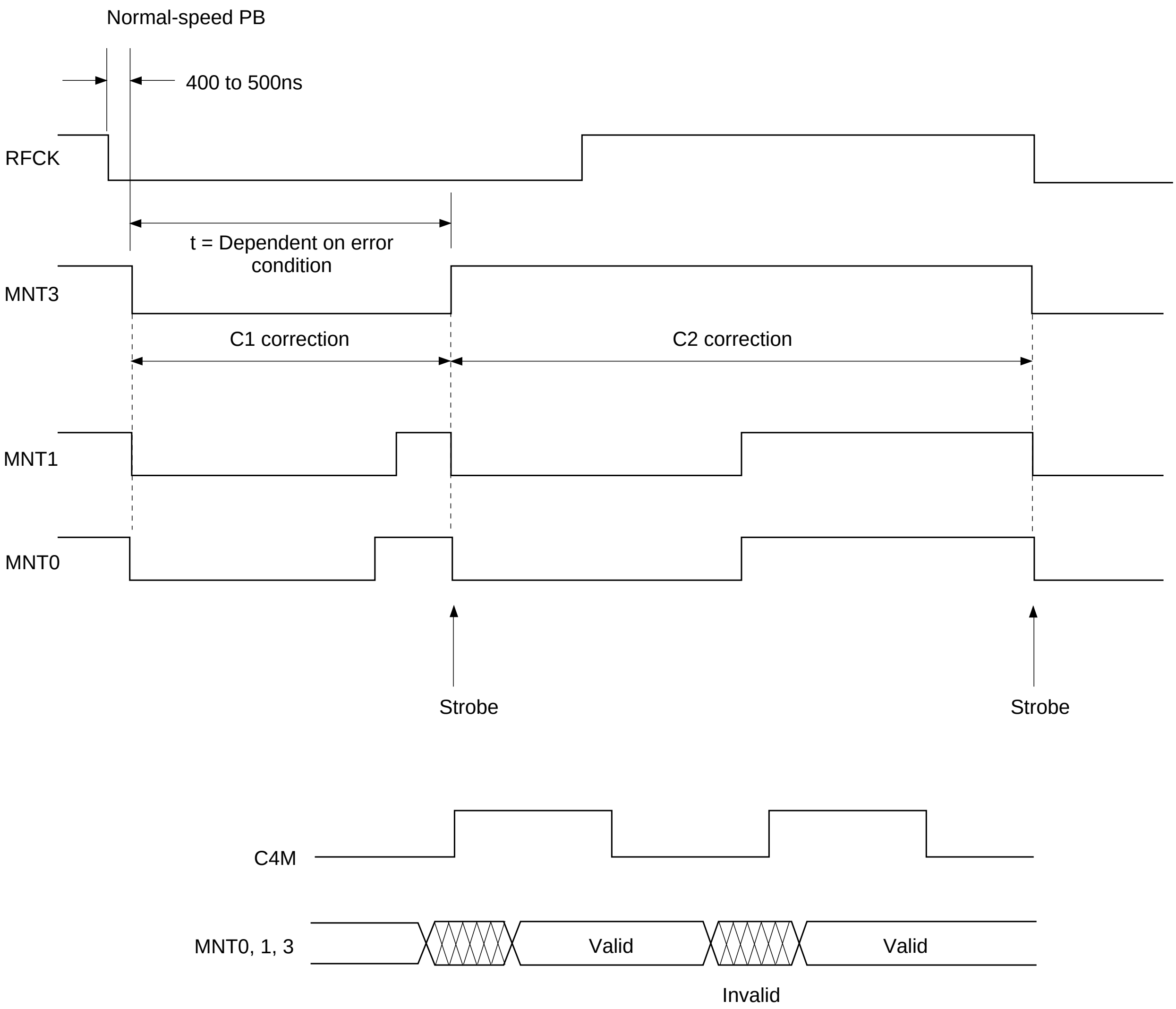
3-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed-Solomon codes with a minimum distance 5.
- The CXD2507 SEC strategy provides excellent playability through powerful frame sync protection and C1 and C2 error corrections.
- The correction status can be monitored outside the LSI.
  See Table 3-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held for that data, or an average value interpolation was made.

MNT3	MNT1	MNT0	Description
0	0	0	No C1 errors
0	0	1	One C1 errors corrected
0	1	1	C1 correction impossible
1	0	0	No C2 errors
1	0	1	One C2 errors corrected
1	1	0	C2 correction impossible

Table 3-2

Timing Chart 3-3

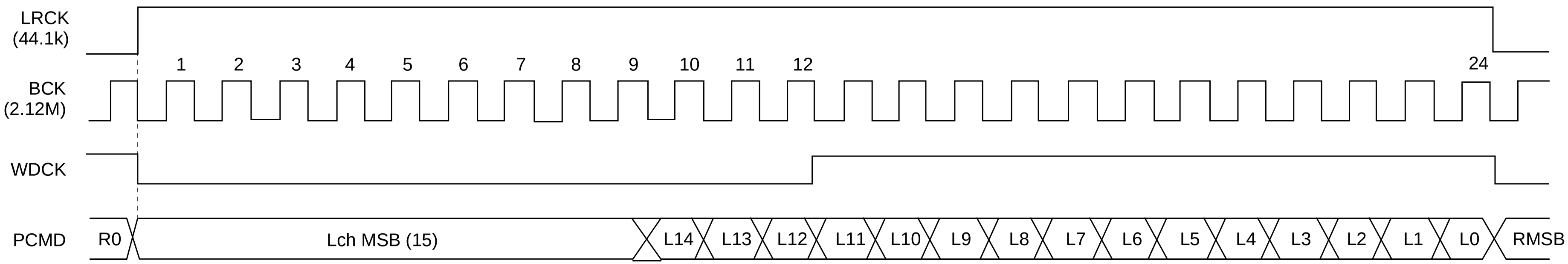


3-4. DA Interface

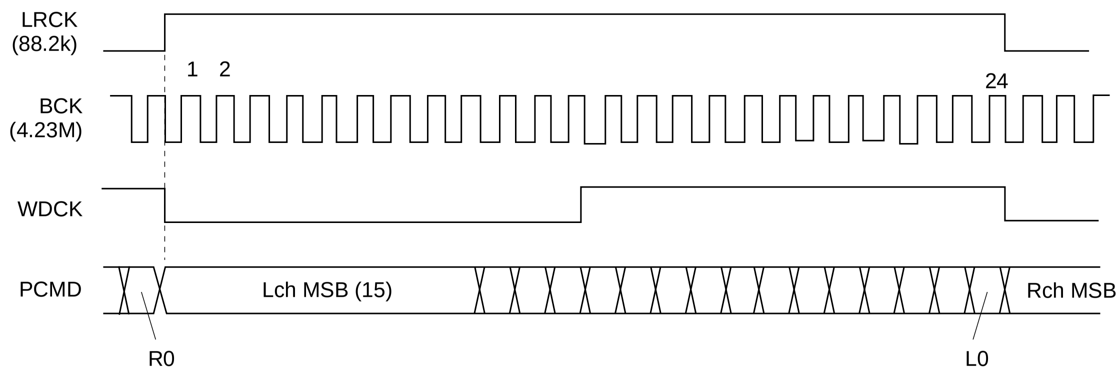
- The CXD2507 DA interface is as described below.
  This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first. When LRCK is high, the data is for the left channel.

Timing Chart 3-4

48bit slot Normal-Speed Playback



48bit slot Double-Speed Playback



3-5. Digital Out

There are three digital out formats: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD2507 supports type 2 form 1.

Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bit 0 to 3) of channel status.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
32 48 176	0															

bit0 to 3 – Sub Q control bits that matched twice with CRCOK

Table 3-5

3-6. Servo Auto Sequencer

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1 track jump, 2N track jumps, and N track move are executed automatically.

SSP (servo signal processor LSI) is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the SSP, but they can be sent to the CXD2507.

Connect the CPU, RF and SSP as shown in Fig. 3-6.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is designed to prevent the transfer of erroneous data to the SSP when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

(a) Auto Focus ($47)

Focus search up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Figure. 3-7. The auto focus is executed after focus search up, and the pickup should be lowered beforehand (focus search down). In addition, blind E of register 5 is used to eliminate FZC chattering. In other words, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

Connection diagram for using auto sequencer (example)

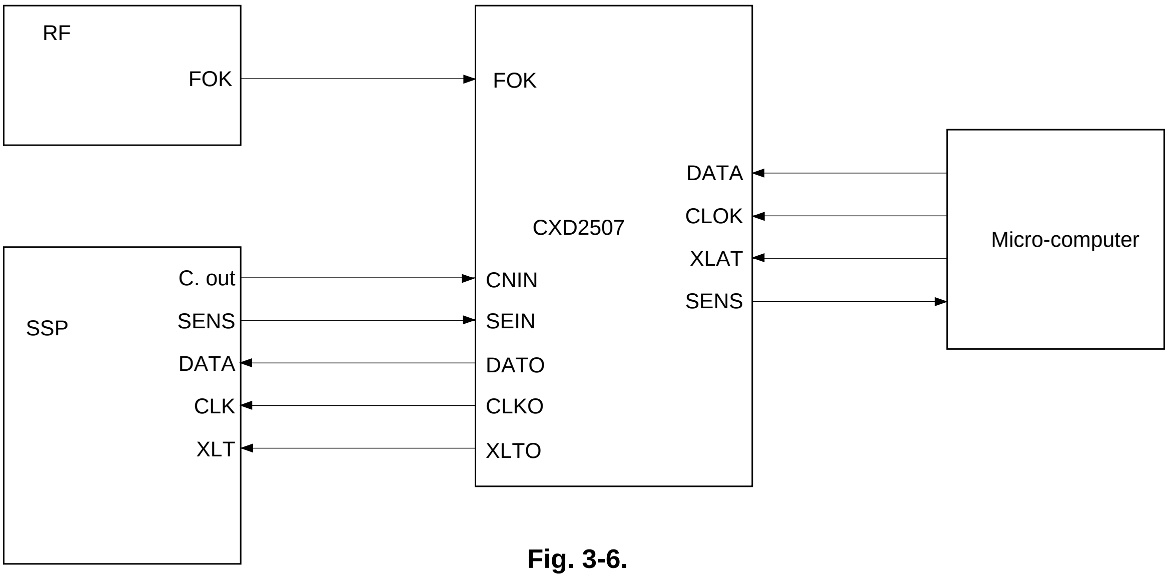


Fig. 3-6.

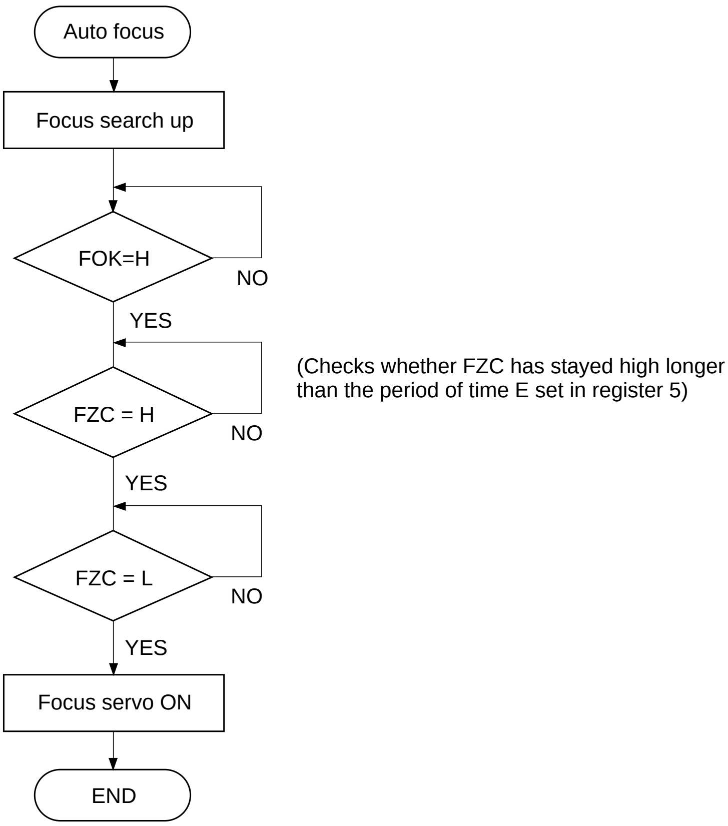


Fig. 3-7-(a). Auto Focus Flow Chart

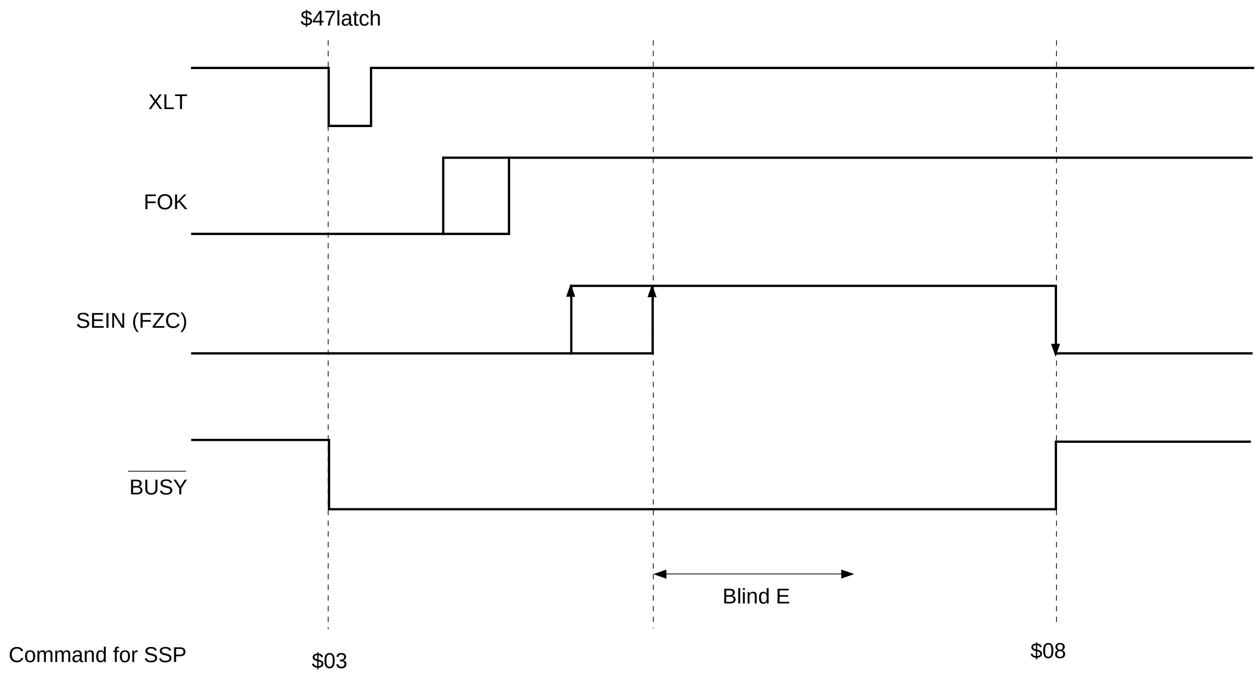


Fig. 3-7-(b). Auto Focus Timing Chart

(b) Track Jump

1, 10, and 2N-track jumps are performed respectively. Always use this when focus, tracking, and the sled servo are on. Note that tracking gain up and braking on ($17) should be sent beforehand because they are not performed.

- 1-track jump

  When $48 ($49 for REV) is received from the CPU, an FWD (REV) 1-track jump is performed in accordance with Fig. 3-8. Set blind A and brake B with register 5.

- 10-track jump

  When $4A ($4B for REV) is received from the CPU, an FWD (REV) 10-track jump is performed in accordance with Fig. 3-9. The principal difference between the 10-track jump and the 1-track jump is whether to kick the sled or not. In addition, after kicking the actuator, 5 tracks have been counted through CNIN, and the brake is applied to the actuator. Then, the actuator speed is found to have slowed up enough (determined by the CNIN cycle becoming longer than the overflow C set in register 5), and the tracking and sled servos are turned on.

- 2N-track jump

  When $4C ($4D for REV) is received from the CPU, an FWD (REV) 2N-track jump is performed in accordance with Fig. 3-10. The track jump count "N" is set in register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. CNIN is used for counting the number of jumps.

  Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set in register 6.

- N-track move

  When $4E ($4F for REV) is received from the CPU, an FWD (REV) N-track move is performed in accordance with Fig. 3-11. N can be set to a maximum of 2^{16} tracks. CNIN is used for counting the number of jumps. This N-track move uses a method in which only the sled is moved, and is suited for moves over thousands of tracks.

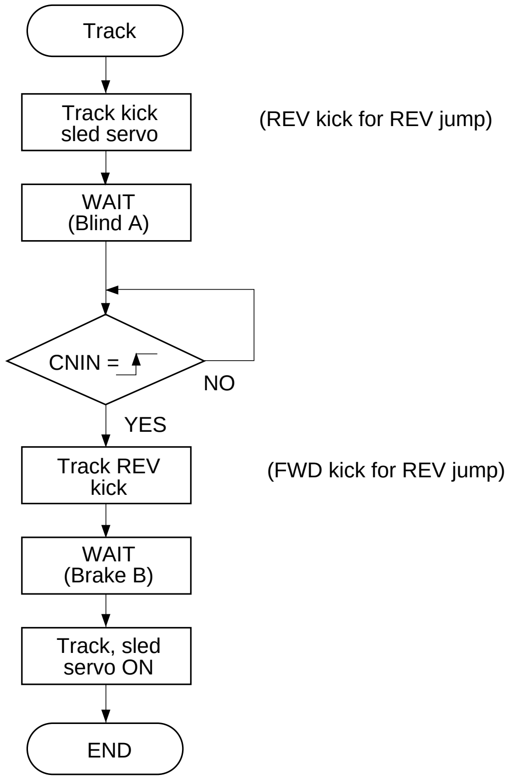


Fig. 3-8-(a). 1-Track Jump Flow Chart

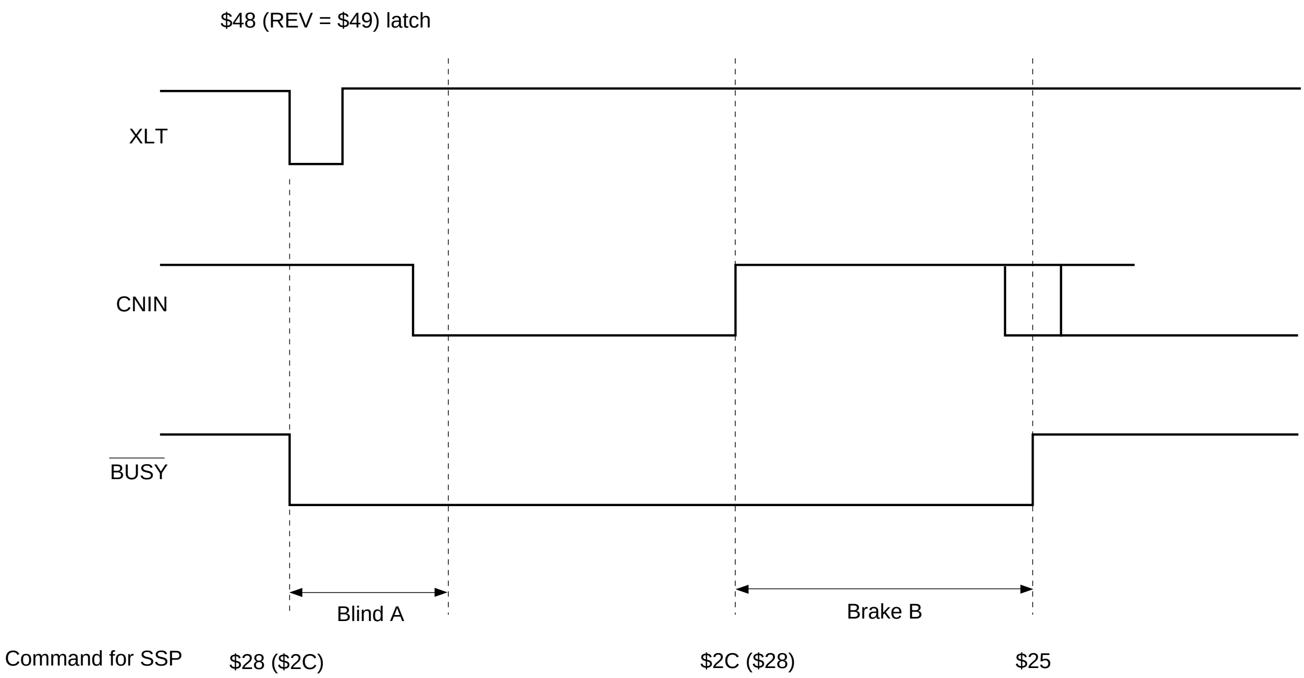


Fig. 3-8-(b). 1-Track Jump Timing Chart

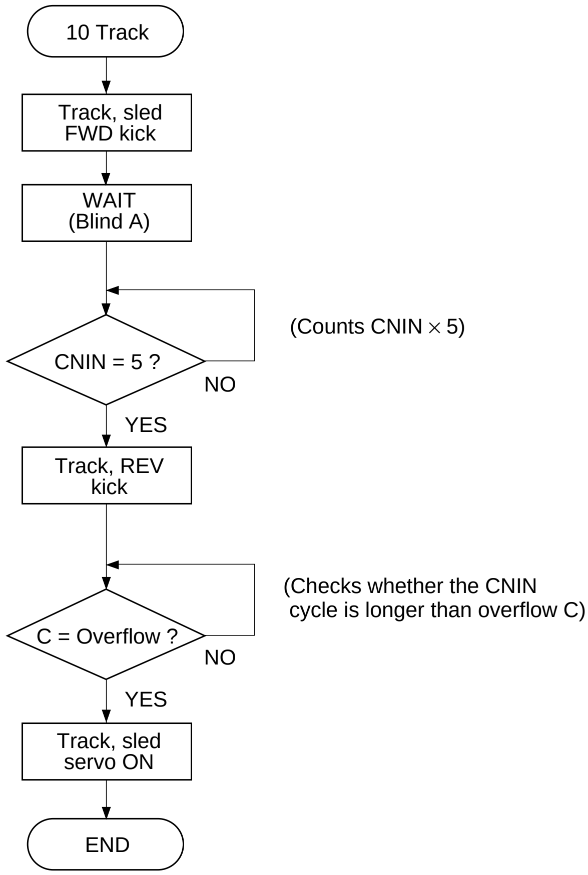


Fig. 3-9-(a). 10-Track Jump Flow Chart

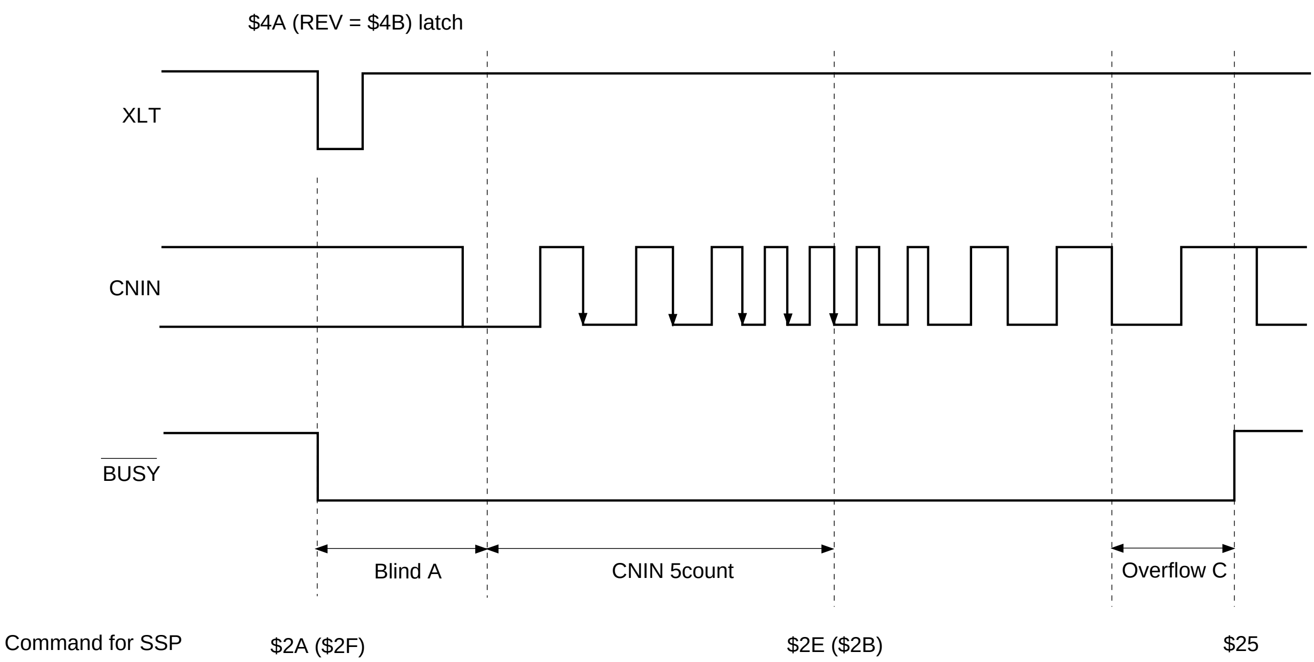


Fig. 3-9-(b). 10-Track Jump Timing Chart

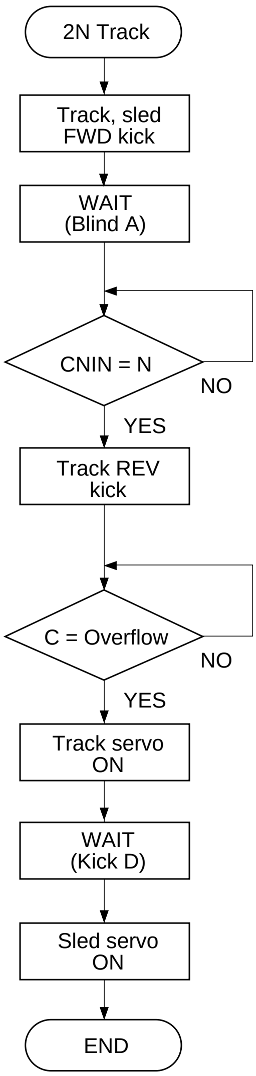


Fig. 3-10-(a). 2N-Track Jump Flow Chart

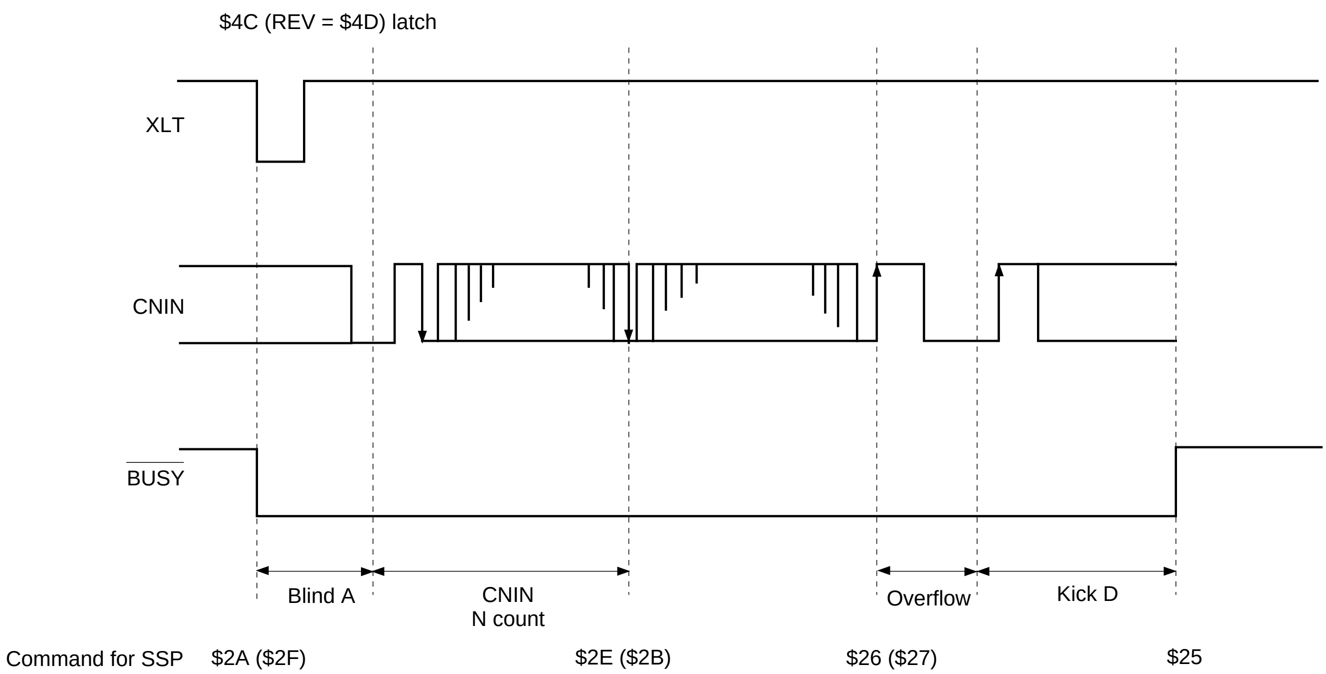


Fig. 3-10-(b). 2N-Track Jump Timing Chart

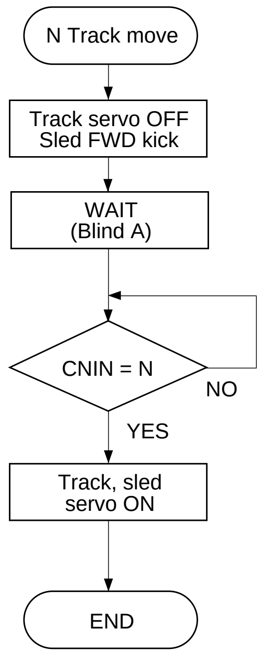


Fig. 3-11-(a). N-Track Move Flow Chart

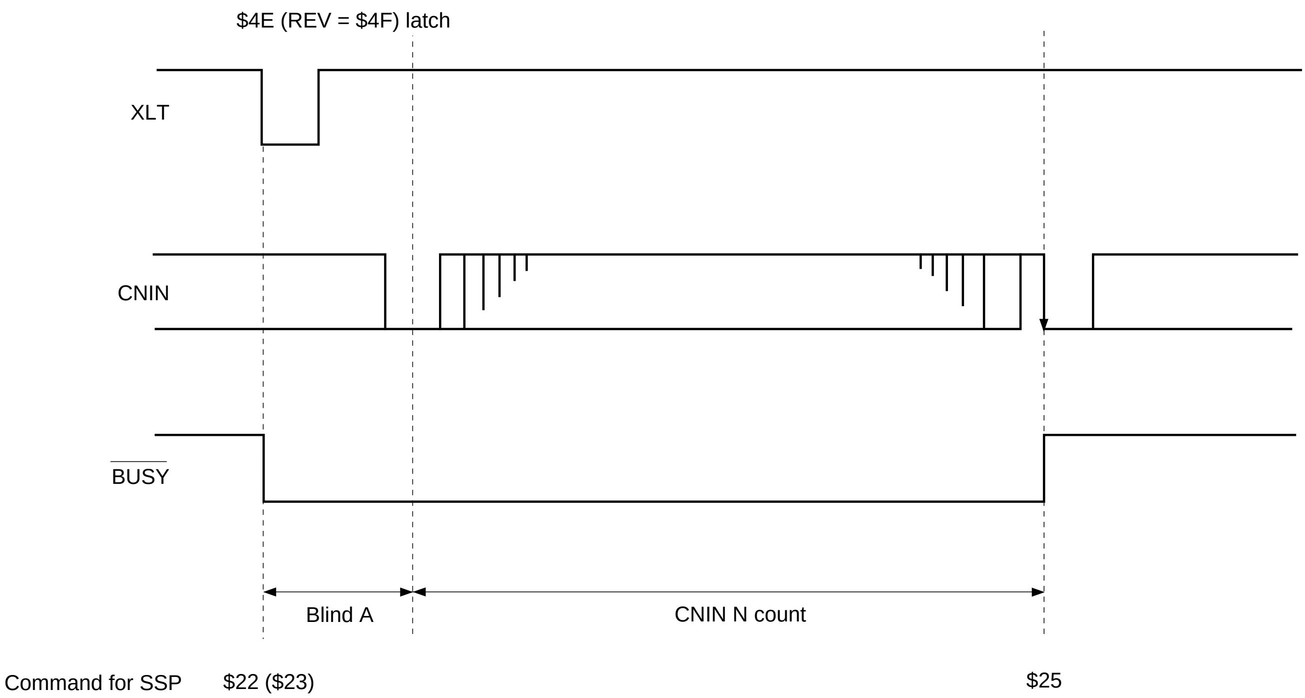


Fig. 3-11-(b). N-Track Move Timing Chart

3-7. Digital CLV

Fig. 3-12 shows the Block Diagram. Digital CLV makes PWM output in CLVS and CLVP with the MDS error and MDP error signal sampling frequency increased to 130kHz during normal speed operation.
In addition, the digital spindle servo can set the gain.

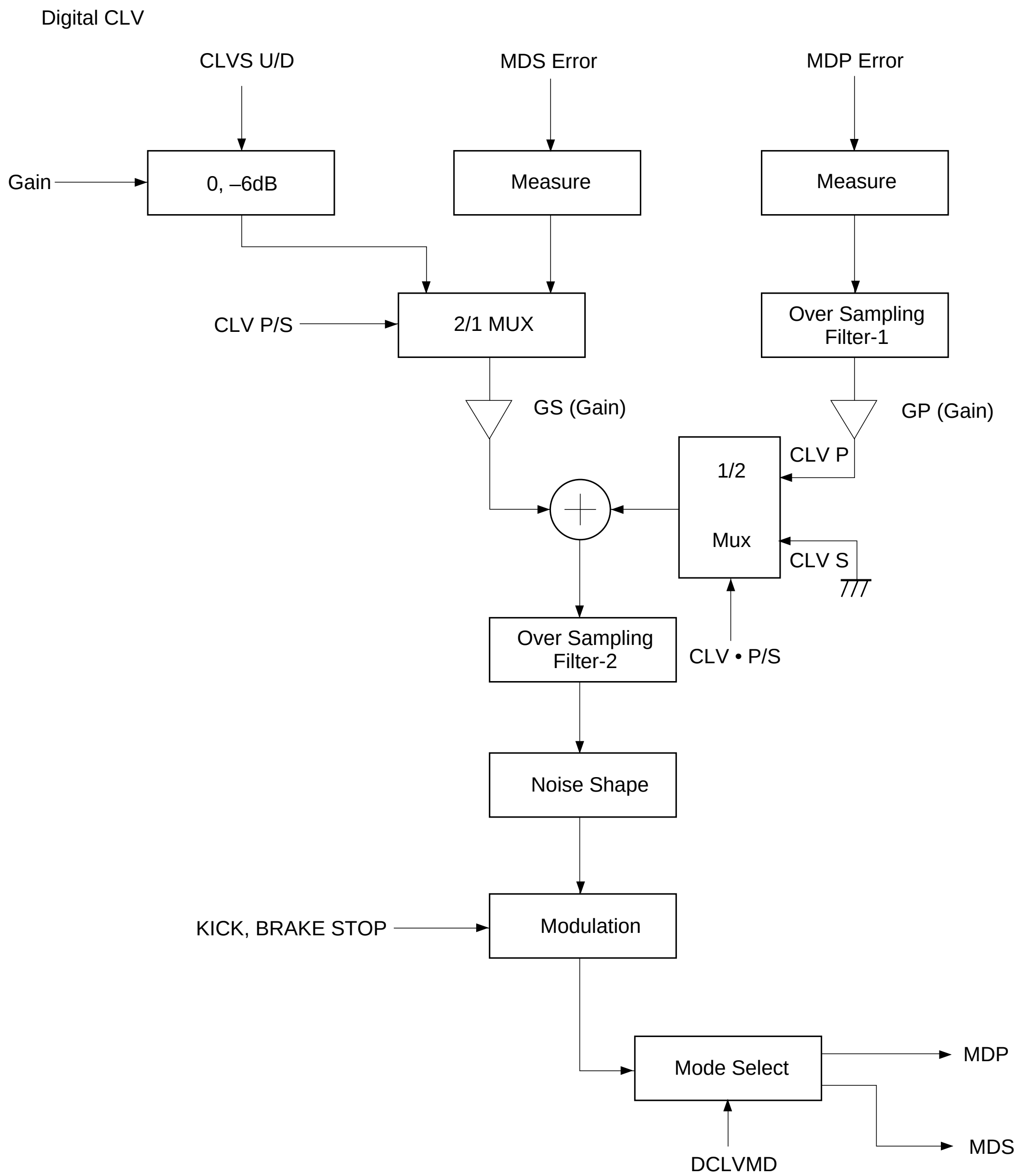


Fig. 3-12. Block Diagram

3-8. Asymmetry Compensation

Fig. 3-13 shows the Block Diagram and Circuit Example.

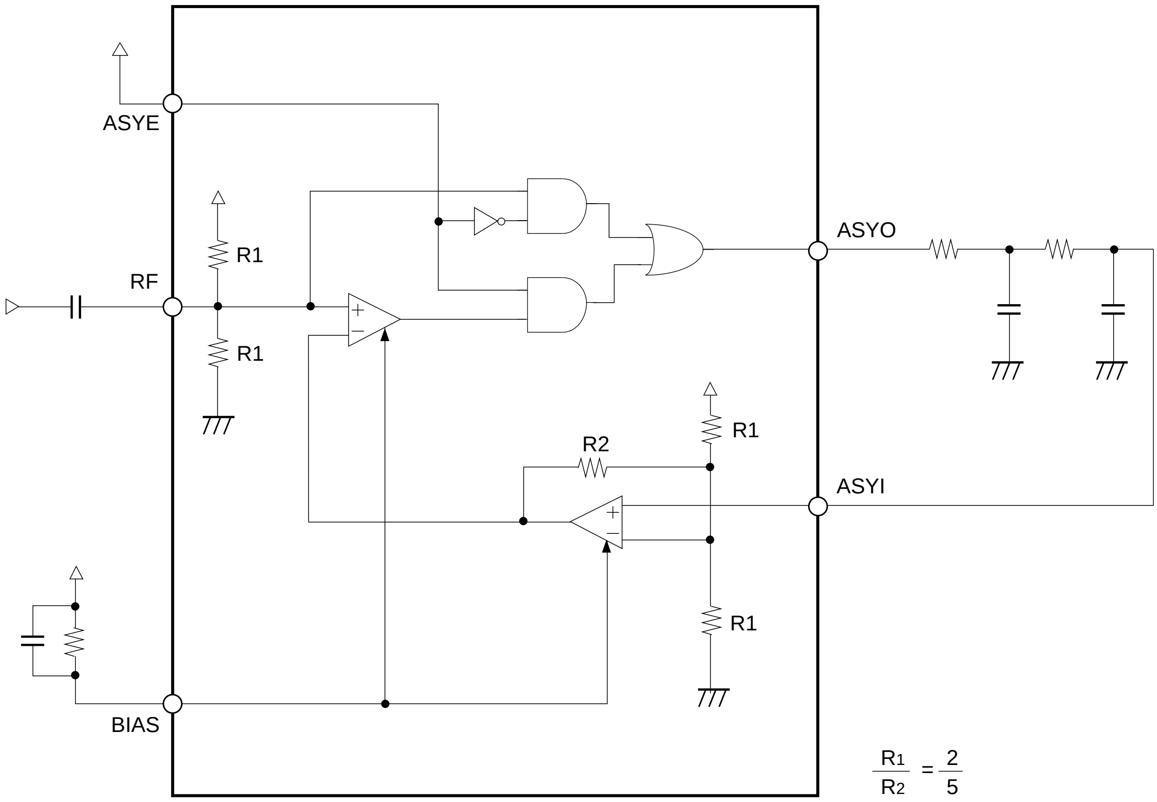
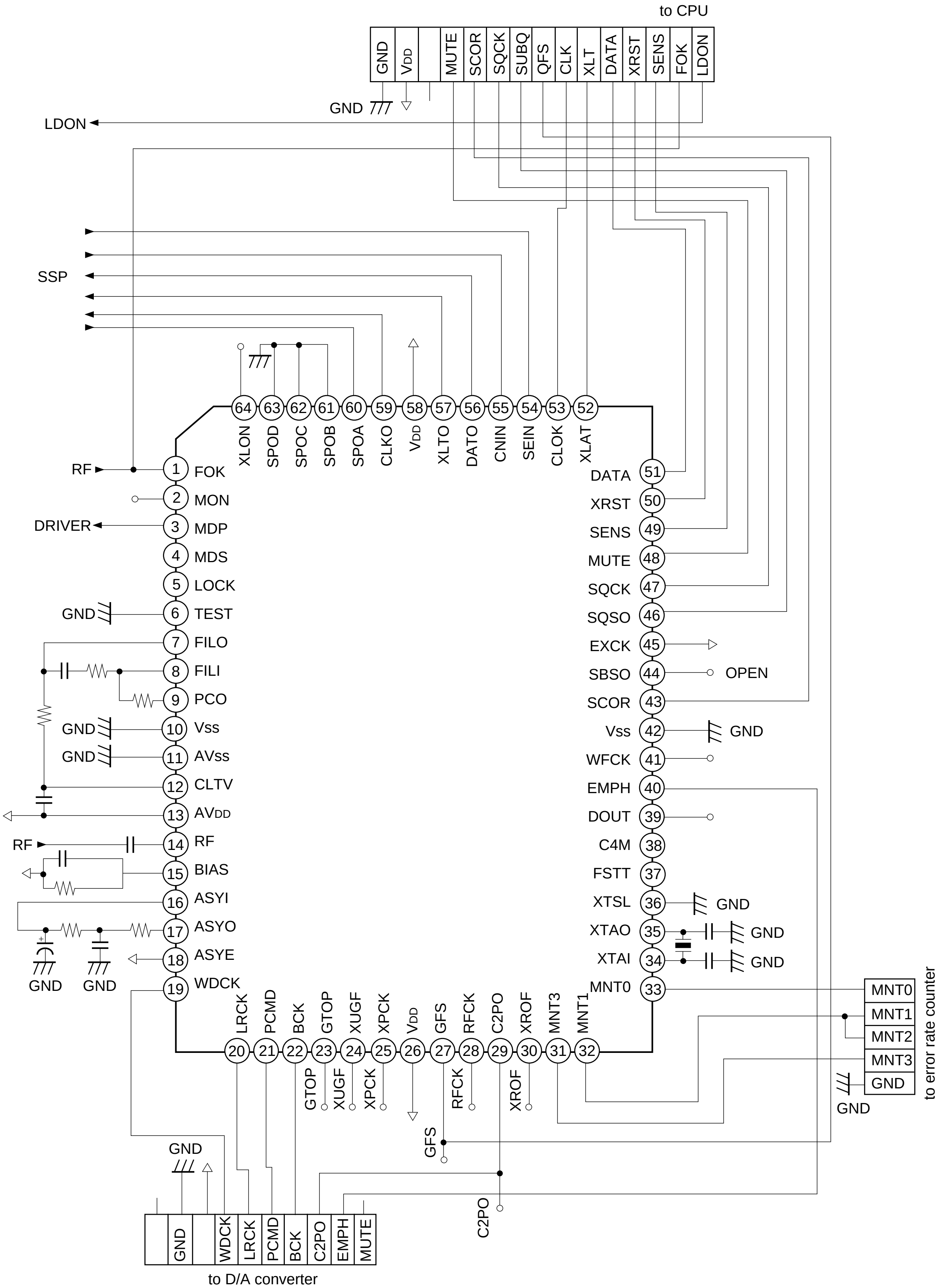


Fig. 3-13. Example of Asymmetry Correction Application Circuit

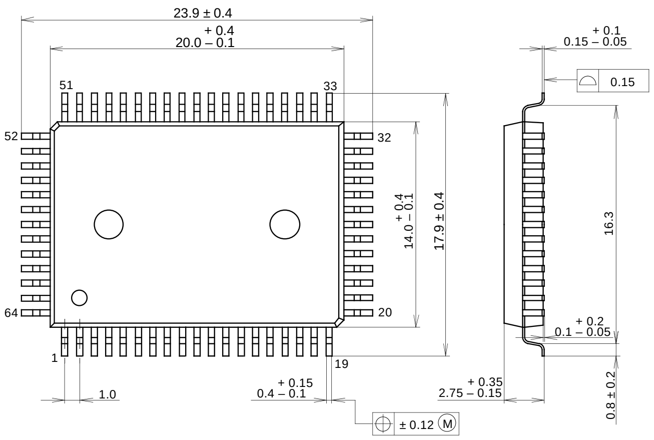
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

64PIN QFP(PLASTIC)

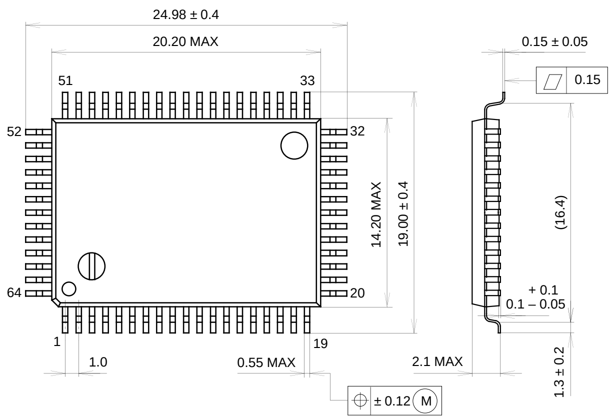


PACKAGE STRUCTURE

SONY CODE	QFP–64P–L01
EIAJ CODE	∗QFP064–P–1420
JEDEC CODE	——

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER /42 ALLOY
PACKAGE WEIGHT	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L121
EIAJ CODE	∗QFP064-P-1420-AX
JEDEC CODE	——

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.5g