LIQUID CRYSTAL DISPLAY (LCD) DRIVER

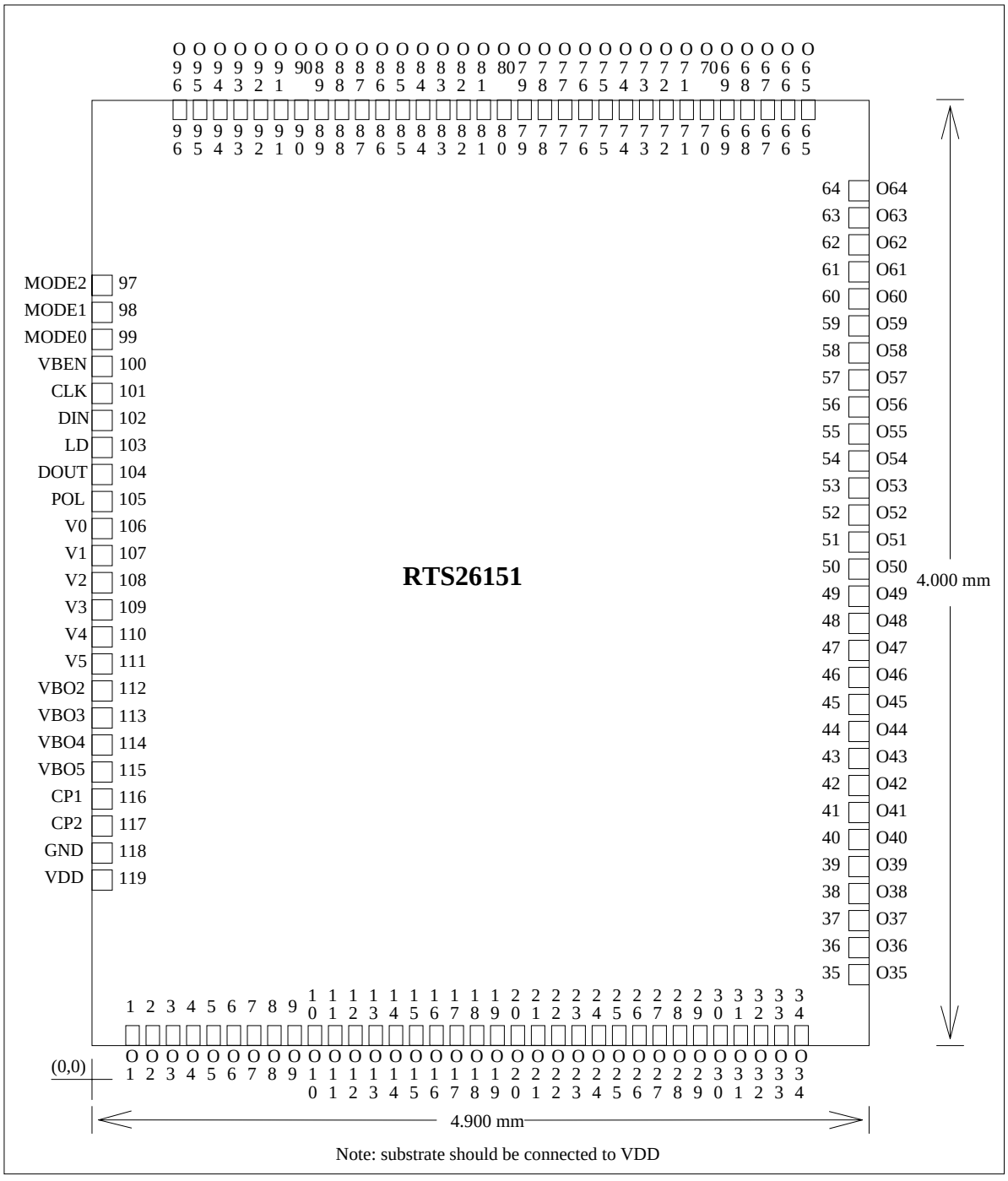
Features

- Operating voltage range: 2.4V - 5.0V
- LCD driver operating (bias) voltage: up to 15V
- Synchronous mode for serial data interface
- Built-in voltage booster (up to 20V when operating at 5V)
- Cascaded function for system expansion
- 96 pins which can be assigned as commons, segments, or both
  - 96-COM
  - 64-COM × 32-SEG
  - 48-COM × 48-SEG
  - 32-COM × 64-SEG
  - 16-COM × 80-SEG
  - 96-SEG

General Description

RTS26151 is a LCD driver system that is integrated with a 96-bit shift-register, a 96-bit latch-register, level control logic and an output driver with built-in voltage booster in a single chip. Designed with CMOS technology to provide a low-current consumption solution, RTS26151 can also be cascaded with multiple chips to become a high resolution LCD display system.

Pad Arrangement



Note: substrate should be connected to VDD

Pad Location

Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	O1	186.5	87.0	**51**	O51	4817.5	2255.5
2	O2	434.5	84.5	**52**	O52	4817.5	2384.0
3	O3	576.0	83.5	**53**	O53	4808.0	2508.5
4	O4	705.5	84.5	**54**	O54	4815.0	2635.5
5	O5	837.0	84.5	**55**	O55	4817.5	2759.0
6	O6	965.0	84.5	**56**	O56	4812.5	2884.0
7	O7	1095.0	83.5	**57**	O57	4815.0	3011.0
8	O8	1221.5	83.5	**58**	O58	4815.0	3135.0
9	O9	1350.5	83.5	**59**	O59	4815.0	3260.0
10	O10	1483.5	84.5	**60**	O60	4812.5	3387.5
11	O11	1616.0	83.5	**61**	O61	4817.5	3516.0
12	O12	1742.0	84.5	**62**	O62	4815.0	3634.0
13	O13	1875.0	85.5	**63**	O63	4812.5	3756.0
14	O14	1997.5	83.0	**64**	O64	4815.0	3891.5
15	O15	2129.0	84.5	**65**	O65	4369.5	3916.0
16	O16	2256.0	83.0	**66**	O66	4237.0	3915.5
17	O17	2388.5	82.0	**67**	O67	4105.0	3912.5
18	O18	2515.0	83.0	**68**	O68	3973.0	3914.0
19	O19	2642.5	81.0	**69**	O69	3847.0	3910.5
20	O20	2775.5	82.0	**70**	O70	3715.0	3909.0
21	O21	2906.0	81.0	**71**	O71	3594.0	3910.5
22	O22	3032.5	84.5	**72**	O72	3459.0	3910.5
23	O23	3160.0	83.0	**73**	O73	3329.0	3914.0
24	O24	3290.5	83.5	**74**	O74	3197.0	3915.5
25	O25	3419.5	84.5	**75**	O75	3069.5	3914.0
26	O26	3552.0	85.5	**76**	O76	2944.0	3915.5
27	O27	3681.0	82.0	**77**	O77	2813.5	3912.5
28	O28	3810.0	85.5	**78**	O78	2683.0	3912.5
29	O29	3935.5	84.5	**79**	O79	2554.0	3910.5
30	O30	4068.5	83.5	**80**	O80	2417.0	3912.5
31	O31	4202.0	84.5	**81**	O81	2290.5	3914.0
32	O32	4331.0	82.0	**82**	O82	2158.0	3912.5
33	O33	4483.5	85.5	**83**	O83	2031.0	3914.0
34	O34	4632.0	84.5	**84**	O84	1900.5	3912.5
35	O35	4814.0	201.5	**85**	O85	1778.0	3909.0
36	O36	4817.5	357.0	**86**	O86	1644.5	3910.5
37	O37	4815.0	503.0	**87**	O87	1518.5	3909.0
38	O38	4812.5	625.0	**88**	O88	1390.0	3909.0
39	O39	4812.5	751.0	**89**	O89	1258.5	3907.5
40	O30	4820.0	875.0	**90**	O90	1128.0	3906.0
41	O41	4815.0	999.0	**91**	O91	996.0	3909.0
42	O42	4817.5	1125.0	**92**	O92	870.0	3907.5
43	O43	4815.0	1252.0	**93**	O93	736.5	3915.5
44	O44	1817.5	1375.5	**94**	O94	609.0	3914.0
45	O45	4815.0	1503.0	**95**	O95	289.5	3911.5
46	O46	4815.0	1627.5	**96**	O96	454.5	3915.0
47	O47	4820.0	1752.5	**97**	MODE2	85.5	3834.0
48	O48	4817.5	1879.0	**98**	MODE1	85.5	3645.5
49	O49	4820.0	2008.0	**99**	MODE0	86.0	3522.5
50	O50	4820.0	2133.0	**100**	VBEN	83.5	2897.5

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Pad No.	Name	X	Y	Pad No.	Name	X	Y
101	CLK	87.0	3273.5	**111**	LCDV5	88.0	1974.0
102	DIN	85.5	3148.0	**112**	VBO2	88.5	1798.5
103	LD	87.0	3020.5	**113**	VBO3	87.0	1663.0
104	DOUT	88.5	2897.5	**114**	VBO4	88.5	1499.0
105	POL	88.0	2770.0	**115**	VBO5	87.0	1360.0
106	LCDV0	86.0	2622.0	**116**	CP1	90.0	1193.5
107	LCDV1	88.5	2490.5	**117**	CP2	89.5	1057.5
108	LCDV2	88.0	2361.5	**118**	GND	86.0	889.5
109	LCDV3	88.5	2330.0	**119**	VDD	88.5	717.5
110	LCDV4	88.0	2103.5				

Absolute Maximum Ratings

Supply Voltage for Logic Circuit……...+2.4V to + 5.0V
Supply Voltage for LCD Circuit
..…..….12V to +25V (V0-VBO5)
Operating temperature....….....……-10°C to 60°C
Storage Temperature.....….…..……-50°C to 125°C

Comments*

Never allow a stress to exceed the values listed under "Absolute Maximum Ratings", otherwise the device would suffer from a permanent damage. Nor is a stress at the listed value be allowed to persist over a period, since an extended exposure to the absolute maximum rating condition may also affect the reliability of the device, if not causing a damage thereof.

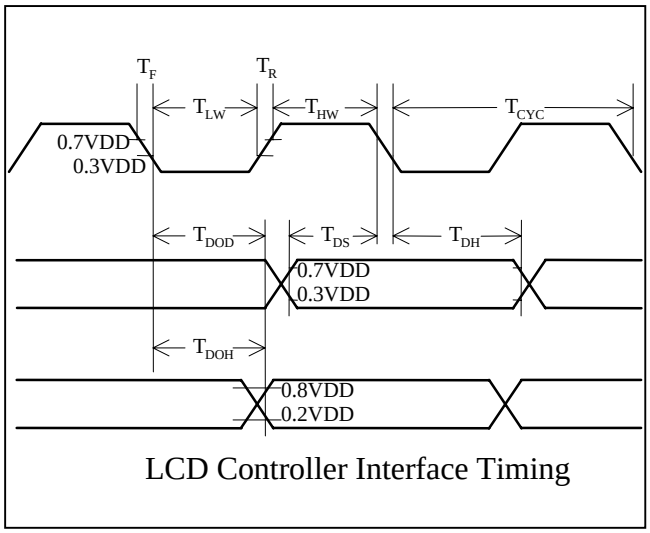
DC Electrical Characteristics

Parameters	Test Condition	Symbol	Min.	Typ.	Max.	Unit
DC Supply Voltage [1]	System Operating Voltage	VDD	2.4	3.0	5.0	V
DC supply Voltage [2]	LCD Bias Voltage (V0-V5)	V0~V5	-	15	28	V
Booster Output	VDD=3V	VBO#	3	-	12	V
DC Supply Current With voltage booster No voltage booster	VDD = 3V (No Load)	I_{CC}	-	 190 70	-	µA
Stop Current	VDD = 3V	I_{STP}	-	1	-	µA
Output Low Voltage	VDD=5.5V, I_{OL}=5.0mA	V_{OL}	-	-	0.4	V
Output High Voltage	VDD=2.4V, I_{OH}=-2.0mA	V_{OH}	2.4	-	-	V

AC Electrical Characteristics

(VDD=3.0V, GND=0V and T_A=25°C)

Parameters	Symbol	Min.	Max.	Unit
Clock Cycle Time	T_{CYC}	1	-	µS
Clock High-Level Width	T_{HW}	50	-	nS
Clock Low-Level Width	T_{LW}	100	-	nS
Clock Rise Time	T_R	-	30	nS
Clock Fall Time	T_F	-	30	nS
Data Setup Time	T_{DS}	100	$(T_{HW})/2$ - 100	nS
Data Hold Time	T_{DH}	100	-	nS
Data Output Delay Time	T_{DOD}	-	300	nS
Data Output Hold Time	T_{DOH}	100	-	nS



LCD Controller Interface Timing

Pad Description

Pad Name	Description
CLK	System serial clock
DIN	Serial data input
DOUT	Serial data output
LD	Latch data into buffer
POL	LCD display phase control (frame waveform polarity)
MODE[2, 1, 0]	Driver operation mode: MODE[2, 1, 0] = [0, 0, 0]: 96-SEG; MODE[2, 1, 0] = [0, 1, 1]: 96-COM; MODE[2, 1, 0] = [1, 1, 1]: 64-COM × 32-SEG; MODE[2, 1, 0] = [1, 1, 0]: 48-COM × 48-SEG; MODE[2, 1, 0] = [1, 0, 1]: 32-COM × 64-SEG; MODE[2, 1, 0] = [1, 0, 0]: 16-COM × 80-SEG;
VBEN	Chip enable input: VBEN=0: disabled VBEN=1: enabled All VBENs must be connected while using multiple chips.
V0 - V5	LCD Bias Voltage
O1~O96	LCD output signals These signals can be programmed as segments, commons, or both. (Depending on MODE[2, 1, 0] settings.)
VBO2~VBO5	Voltage booster output
CAP1 – CAP2	External capacitor for voltage booster function
VDD	System power
VSS	System ground

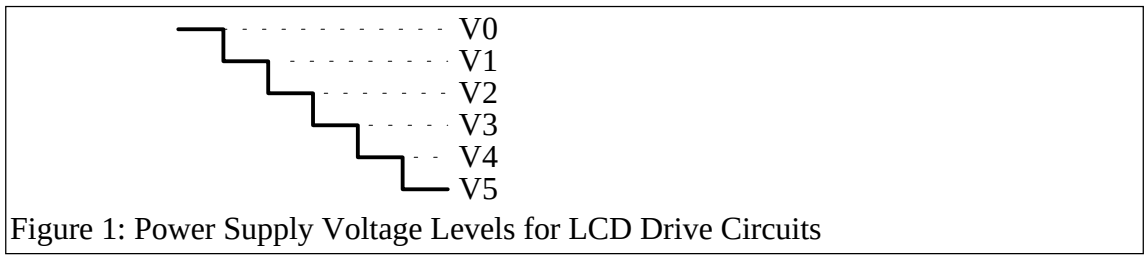


Figure 1: Power Supply Voltage Levels for LCD Drive Circuits

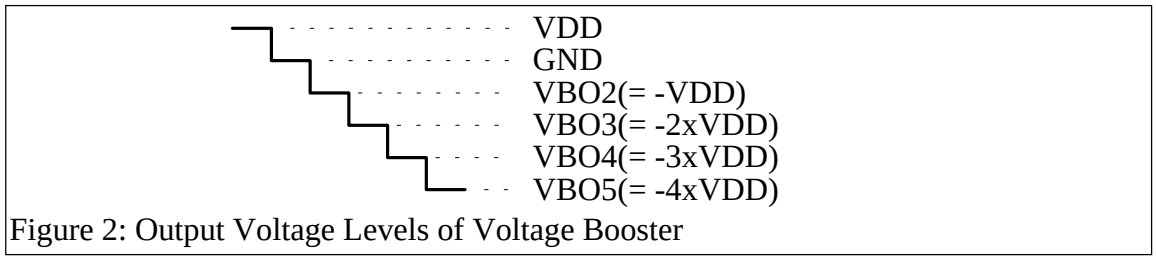


Figure 2: Output Voltage Levels of Voltage Booster

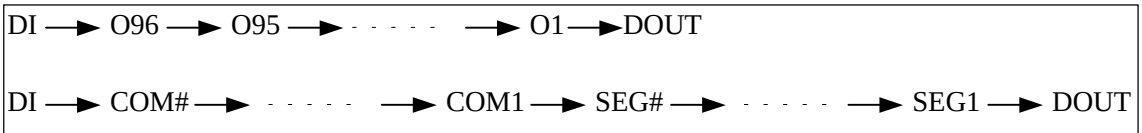
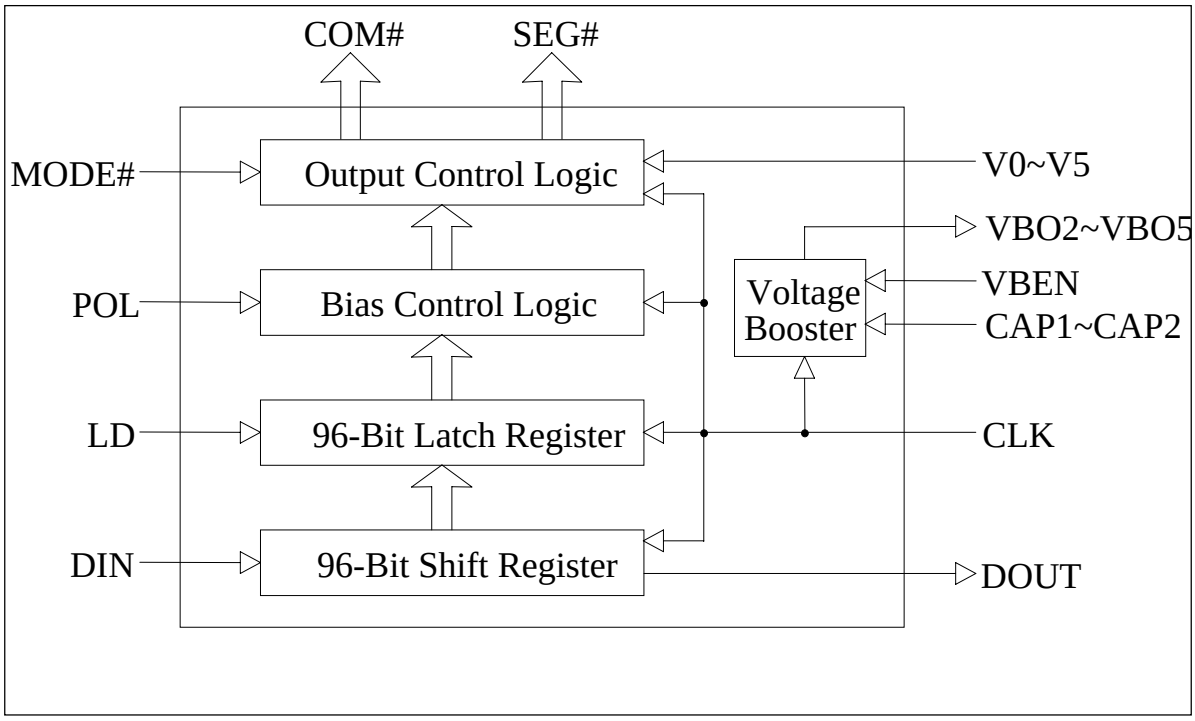


Figure 3: Display Data Shift Direction

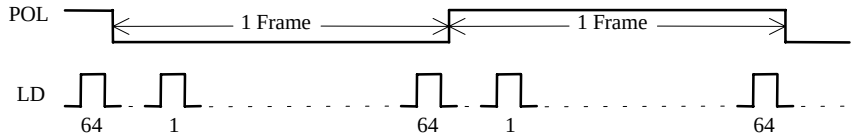
Block Diagram



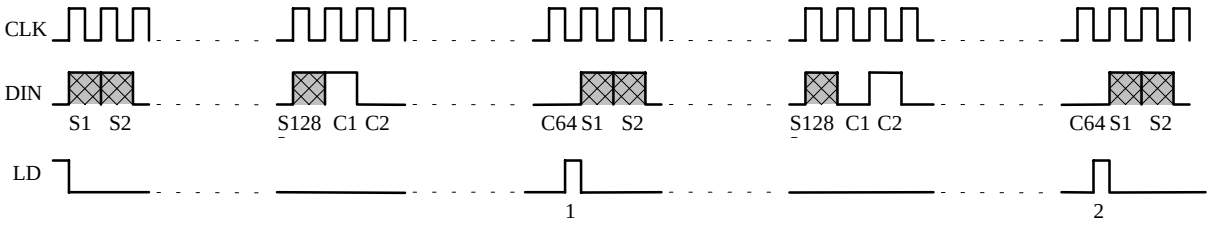
Operation Timing

Figure 4: shows the operation timing for the application example (64x128)

a. POL and LD signal



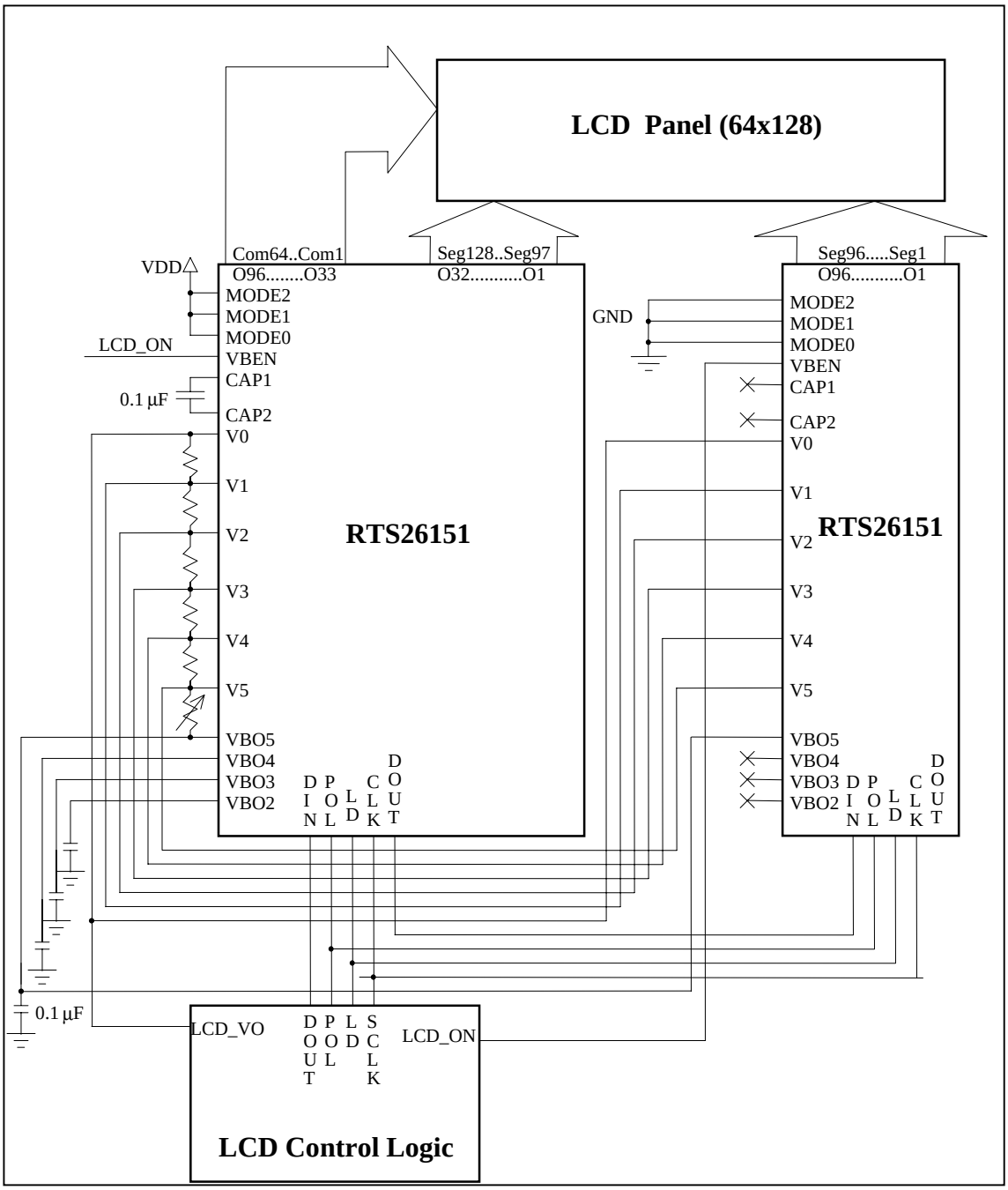
b. DIN and LD signal



*S denotes segment; C denotes common

Data Type	POL	DIN Data	Output Voltage Level
Output as Segment	0	0	V2
		1	V0
	1	0	V3
		1	V5
Output as Common	0	0	V1
		1	V5
	1	0	V4
		1	V0

Application Example (64 COM × 128 SEG)



REVISION HISTORY

Revision #	Description	Page #	Date
V1.2	Revise power consumption (DC Electrical Characteristics).	5	May 12, 1999
V1.21	Revise LOGO	1~10	May 14, 2002