WM2633

Byte-wide Parallel Input, 12-bit Voltage Output DAC with Internal Reference

Production Data, July 1999, Rev 1.0

FEATURES

- **12-bit voltage output DAC**
- **Dual supply 2.7V to 5.5V operation**
- **DNL ±0.3 LSBs, INL ±1.2 LSBs**
- **Internal programmable voltage reference**
- **Programmable settling time**
- **8-bit micro controller compatible interface**
- **Power down mode (10nA)**

APPLICATIONS

- **Battery powered test instruments**
- **Digital offset and gain adjustment**
- **Battery operated/remote industrial controls**
- **Machine and motion control devices**
- **Wireless telephone and communication systems**
- **Speech synthesis**
- **Arbitrary waveform generation**

DESCRIPTION

The WM2633 is a 12-bit voltage output, resistor string, digital-to-analogue converter. A hardware controlled power down mode is provided that reduces current consumption to 10nA. The WM2633 features an internal programmable voltage reference simplifying overall system design. A reference voltage may also be supplied externally.

The device has an 8-bit microcontroller compatible parallel interface. The eight data LSBs, the four data MSBs, and the five control bits are written using three different addresses.

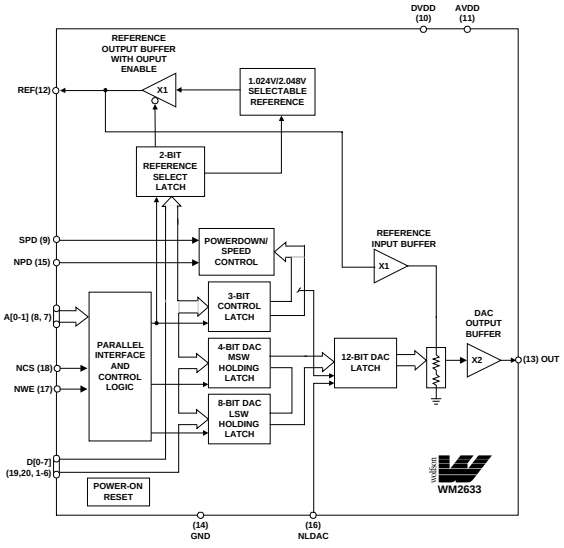
Excellent performance is delivered with a typical DNL of 0.3 LSBs and a typical INL of 1.2 LSBs. The output stage is buffered by a x2 gain near rail-to-rail amplifier, which features a Class A output stage (slow mode, Class AB). The settling time of the DAC is software or pin programmable to allow the designer to optimise speed versus power dissipation.

The device is available in a 20-pin TSSOP package. Commercial temperature (0° to 70°C) and Industrial temperature (-40° to 85°C) variants are supported.

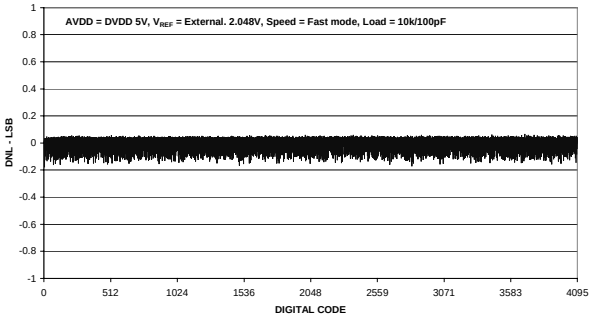
ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2633CDT	0° to 70°C	20-pin TSSOP
WM2633IDT	-40° to 85°C	20-pin TSSOP

BLOCK DIAGRAM



TYPICAL PERFORMANCE



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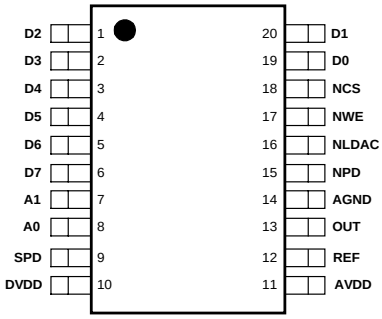
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	D2	Digital input	Data input.
2	D3	Digital input	Data input.
3	D4	Digital input	Data input.
4	D5	Digital input	Data input.
5	D6	Digital input	Data input.
6	D7	Digital input	Data input.
7	A1	Digital input	Address input.
8	A0	Digital input	Address input.
9	SPD	Digital input	Speed select. Digital input.
10	DVDD	Supply	Digital positive power supply.
11	AVDD	Supply	Analogue positive power supply.
12	REF	Analogue I/O	Analogue reference voltage input/output.
13	OUT	Analogue output	DAC analogue voltage output.
14	GND	Supply	Ground.
15	NPD	Digital input	Power down. Active low digital input which powers down all analogue circuits.
16	NLDAC	Digital input	Load DAC. Digital input active low. NLDAC must be taken low to update the DAC latch from the holding latches.
17	NWE	Digital input	Write enable. Digital input active low.
18	NCS	Digital input	Chip select. Digital input active low.
19	D0	Digital input	Data input.
20	D1	Digital input	Data input.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION		MIN	MAX
Digital supply voltages, AVDD or DVDD to GND			7V
Supply voltage differences, AVDD to DVDD		-2.8V	2.8V
Reference input voltage		-0.3V	AVDD + 0.3V
Digital input voltage range to GND		-0.3V	DVDD + 0.3V
Operating temperature range, T_A	WM2633CDT WM2633IDT	0°C -40°C	70°C 85°C
Storage temperature		-65°C	150°C
Lead temperature 1.6mm (1/16 inch) soldering for 10 seconds			260°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	AVDD, DVDD		2.7		5.5	V
High-level digital input voltage	V_{IH}	See Note 1	2			V
Low-level digital input voltage	V_{IL}	See Note 1			0.8	V
Reference voltage to REF	V_{REF}	See Note 1			AVDD - 1.5	V
Load resistance	R_L		2			kΩ
Load capacitance	C_L				100	pF
Operating free-air temperature	T_A	WM2633CDT	0		70	°C
		WM2633IDT	-40		85	°C

Note: Reference input voltages greater than AVDD/2 will cause saturation for large DAC codes.

ELECTRICAL CHARACTERISTICS

Test Characteristics:
R_L = 10kΩ, C_L = 100pF AVDD = DVDD = 5V ± 10%, V_{REF} = 2.048V and AVDD = DVDD = 3V ± 10%, V_{REF} = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static DAC Specifications						
Resolution			12			bits
Integral non-linearity	INL	See Note 1		±1.2	±3	LSB
Differential non-linearity	DNL	See Note 2		±0.3	±0.5	LSB
Zero code error	ZCE	See Note 3			12	mV
Gain error	GE	See Note 4			±0.3	% FSR
D.c power supply rejection ratio	d.c. PSRR	See Note 5		0.5		mV/V
Zero code error temperature coefficient		See Note 6		20		ppm/°C
Gain error temperature coefficient		See Note 6		20		ppm/°C
DAC Output Specifications						
Output voltage range			0		AVDD-0.4	V
Output load regulation		2kΩ to 10kΩ load See Note 7		0.1	0.3	%
Power Supplies						
Active supply current	IDD	No load, V_{IH}=DVDD, V_{IL}=0V AVDD = DVDD = 5V, V_{REF} = 2.048V, Internal				
		Slow		1.3	1.6	mA
		Fast		2.3	2.8	mA
		AVDD = DVDD = 5V V_{REF} = 2.048V, External				
		Slow		0.9	1.2	mA
		Fast		1.9	2.4	mA
		AVDD = DVDD = 3V, V_{REF} = 1.024V, Internal				
		Slow		1.2	1.5	mA
		Fast		2.1	2.6	mA
		AVDD = DVDD = 3V, V_{REF} = 1.024V, External				
		Slow		0.9	1.1	mA
		Fast		1.8	2.3	mA
		See Note 8				
Power down supply current		No load, all inputs 0V or DVDD See Note 9		0.01	1	µA
Dynamic DAC Specifications						
Slew rate		DAC code 32-4095, 10%-90%				
		Slow	1.2	1.7		V/µs
		Fast	6	10		V/µs
		See Note 10				
Settling time		DAC code 32-4095				
		Slow		3.5		µs
		Fast		1		µs
		See Note 11				

Test Characteristics:
R_L = 10kΩ, C_L = 100pF AVDD = DVDD = 5V ± 10%, V_{REF} = 2.048V and AVDD = DVDD = 3V ± 10%, V_{REF} = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Glitch energy		Code 2047 to code 2048		5		nV-s
Signal to noise ratio	SNR	f_S = 480ksps, f_{OUT} = 1kHz BW = 20kHz, TA=25°C See Note 12	73	78		dB
Signal to noise and distortion ratio	SNRD	f_S = 480ksps, f_{OUT} = 1kHz BW = 20kHz, TA=25°C See Note 12	61	67		dB
Total harmonic distortion	THD	f_S = 480ksps, f_{OUT} = 1kHz BW = 20kHz, TA=25°C See Note 12		-69	-62	dB
Spurious free dynamic range	SPFDR	f_S = 480ksps, f_{OUT} = 1kHz BW = 20kHz, T_A = 25°C See Note 12	63	74		dB
Reference Configured as Input						
Reference input resistance	RREF			10		MΩ
Reference input capacitance	CREF			55		pF
Reference feedthrough		V_{REF}=1V_{PP} at 1kHz + 1.024V d.c., DAC code 0		-60		dB
Reference input bandwidth		V_{REF}= 0.2V_{PP} + 1.024V d.c. DAC code 2048 Slow Fast		 500 900		 kHz kHz
Reference Configured as Output						
Low reference voltage	$V_{REFOUTL}$		1.003	1.024	1.045	V
High reference voltage	$V_{REFOUTH}$	VDD > 4.75V	2.027	2.048	2.069	V
Output source current	I_{REFSRC}				1	mA
Output sink current	I_{REFSNK}		-1			mA
Load Capacitance					100	pF
PSRR				-48		dB
Digital Inputs						
High level input current	I_{IH}	Input voltage = DVDD			1	µA
Low level input current	I_{IL}	Input voltage = 0V			-1	µA
Input capacitance	C_I			8		pF

Notes:

1. **Integral non-linearity (INL)** is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full scale errors).
2. **Differential non-linearity (DNL)** is the difference between the measured and ideal 1LSB amplitude change of any adjacent two codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in digital input code.
3. **Zero code error** is the voltage output when the DAC input code is zero.
4. **Gain error** is the deviation from the ideal full scale output excluding the effects of zero code error.
5. **Power supply rejection ratio** is measured by varying AVDD from 4.5V to 5.5V and measuring the proportion of this signal imposed on the zero code error and the gain error.
6. **Zero code error** and **Gain error** temperature coefficients are normalised to full scale voltage.
7. **Output load regulation** is the difference between the output voltage at full scale with a 10kΩ load and 2kΩ load. It is expressed as a percentage of the full scale output voltage with a 10kΩ load.

8. I_{DD} is measured while continuously writing code 2048 to the DAC. For V_{IH} < DVDD - 0.7V and V_{IL} > 0.7V supply current will increase.
9. **Typical supply current** in powerdown mode is 10nA. Production test limits are wider for speed of test.
10. **Slew rate results** are for the lower value of the rising and falling edge slew rates.
11. **Settling time** is the time taken for the signal to settle to within 0.5LSB of the final measured value for both rising and falling edges. Limits are ensured by design and characterisation, but are not production tested.
12. **SNR, SNRD, THD** and **SPFDR** are measured on a synthesised sinewave at frequency f_{OUT} generated with a sampling frequency f_S .

PARALLEL INTERFACE

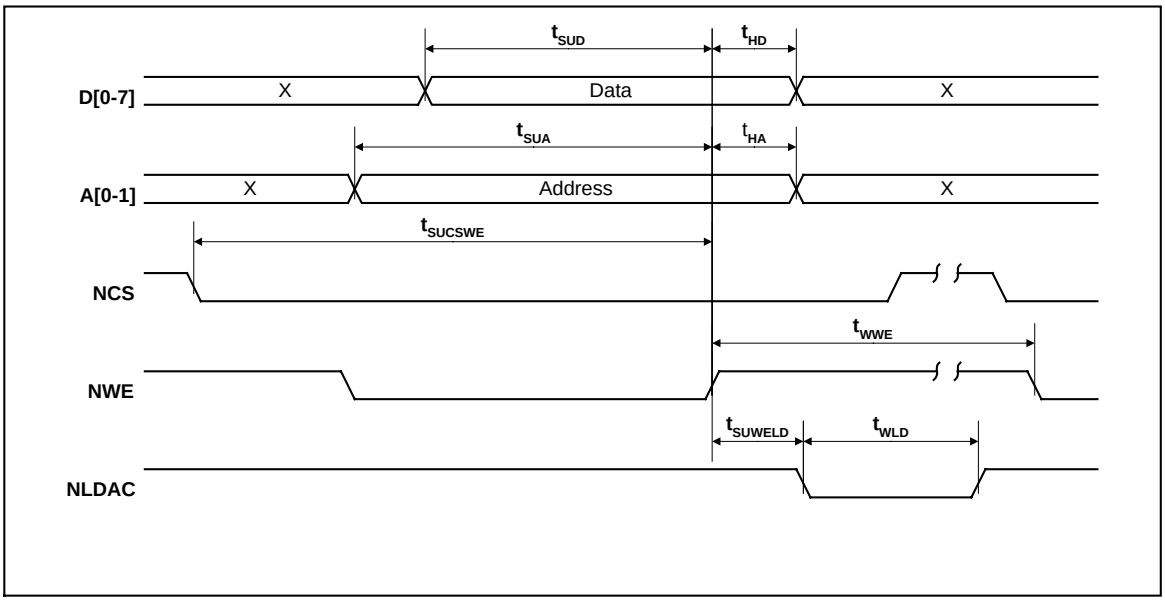


Figure 1 Timing Diagram

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SUCSWE}	Setup time NCS low before positive NWE edge	15			ns
t_{SUD}	Data ready before positive NWE edge	10			ns
t_{HD}	Data hold after positive NWE edge	5			ns
t_{SUA}	Setup time for address bits A0, A1	20			ns
t_{SUWELD}	Positive NWE edge before NLDAC low	5			ns
t_{WWE}	High pulse width of NWE	20			ns
t_{WLD}	Low pulse width of NLDAC	23			ns

TYPICAL PERFORMANCE GRAPHS

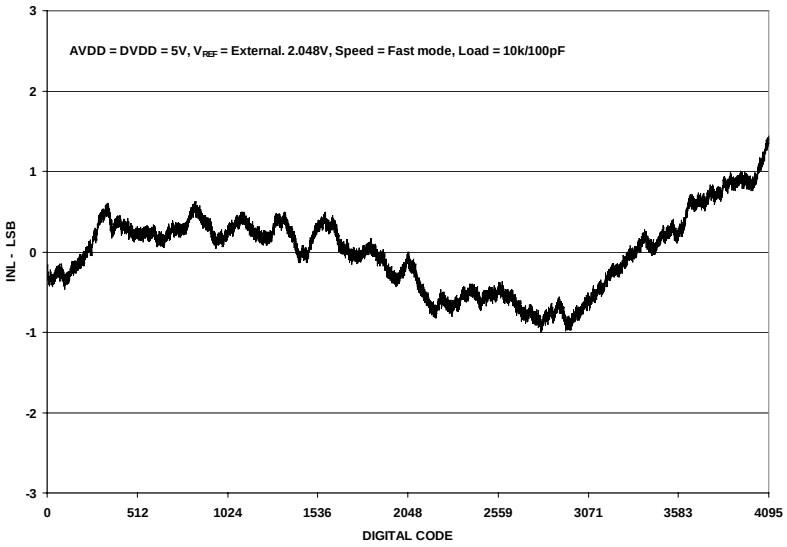


Figure 2 Integral Non-Linearity

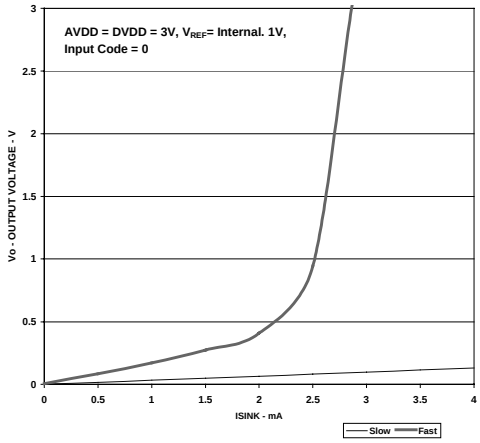


Figure 3 Sink Current AVDD = 3V

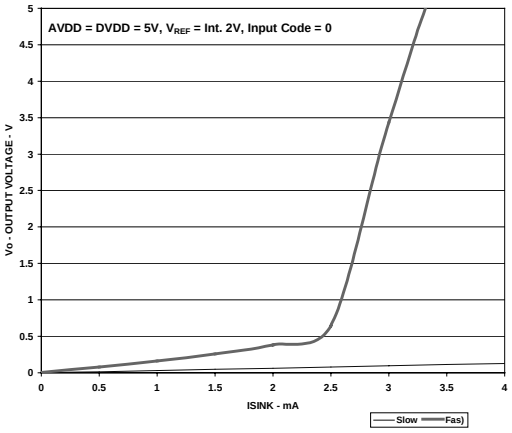


Figure 4 Sink Current AVDD = 5V

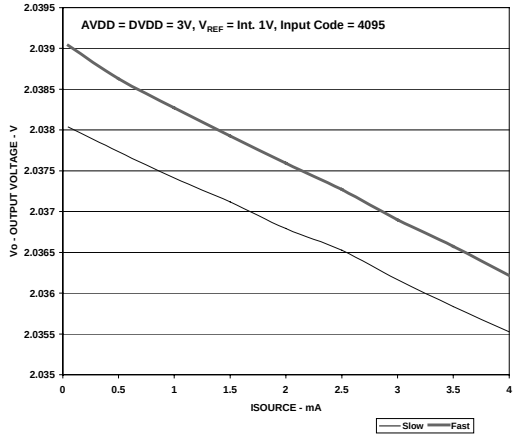


Figure 5 Source Current AVDD = 3V

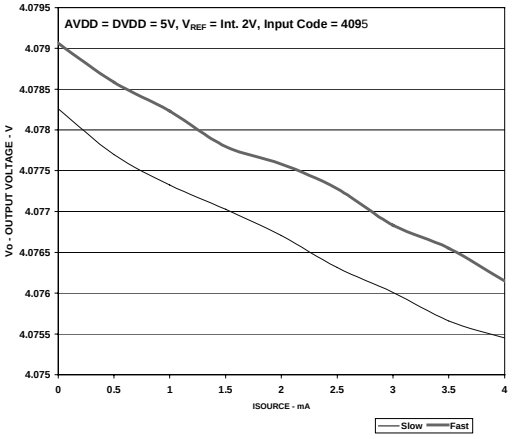


Figure 6 Source Current AVDD = 5V

DEVICE DESCRIPTION

GENERAL FUNCTION

The device uses a resistor string network buffered with an op amp to convert 12-bit digital data to analogue voltage levels (see Block Diagram). The output voltage is determined by the reference input voltage and the input code according to the following relationship:

$$\text{Output voltage} = 2\left(V_{REF}\right)\frac{\text{CODE}}{4096}$$

INPUT			OUTPUT
1111	1111	1111	$2\left(V_{REF}\right)\frac{4095}{4096}$
	:		:
1000	0000	0001	$2\left(V_{REF}\right)\frac{2049}{4096}$
1000	0000	0000	$2\left(V_{REF}\right)\frac{2048}{4096} = V_{REF}$
0111	1111	1111	$2\left(V_{REF}\right)\frac{2047}{4096}$
	:		:
0000	0000	0001	$2\left(V_{REF}\right)\frac{1}{4096}$
0000	0000	0000	0V

Table 1 Binary Code Table (0V to $2V_{REF}$ Output), Gain = 2

POWER ON RESET

An internal power-on-reset circuit resets the DAC register to all 0s on power-up.

BUFFER AMPLIFIER

The output buffer has a near rail-to-rail output with short circuit protection and can reliably drive a 2kΩ load with a 100pF load capacitance.

EXTERNAL REFERENCE

If an external reference is selected, the reference voltage input is buffered which makes the DAC input resistance independent of code. The REF pin has an input resistance of 10MΩ and an input capacitance of typically 55pF. The reference voltage determines the DAC full-scale output.

HARDWARE CONFIGURATION OPTIONS

The device has three configuration options that are controlled by device pins.

DEVICE POWER DOWN

The device can be powered-down by pulling pin NPD (pin 15) high. This powers down the DAC. This will reduce power consumption significantly. The NPD pin low overrides the software control bit PWR. When the power down function is released the device reverts to the DAC code set prior to power down.

SETTLING TIME

The settling time of the device can be controlled by pin SPD (pin 9). A ONE on pin SPD will ensure a FAST settling time; a ZERO will ensure a SLOW settling time. The SPD pin high overrides the software control bit SPD.

SIMULTANEOUS DAC UPDATE

The NLDAC pin (Pin 16) can be held high to prevent word writes from updating the DAC latch. By writing the new value to the DAC then pulling NLDAC low, the new DAC code is loaded into the DAC latch.

PARALLEL INTERFACE

The device latches data on the positive edge of NWE. It must be enabled with NCS low. Whether the data is written to one of the DAC holding latches (MSW, LSW) or the control register, depends on the address bits A1 and A0. NLDAC low updates the DAC with the value in the holding latch. NLDAC is an asynchronous input and can be held low, if a synchronous update is not necessary. Alternatively, the RLDAC bit of the control register can be used to synchonously update the DAC latch via software control.

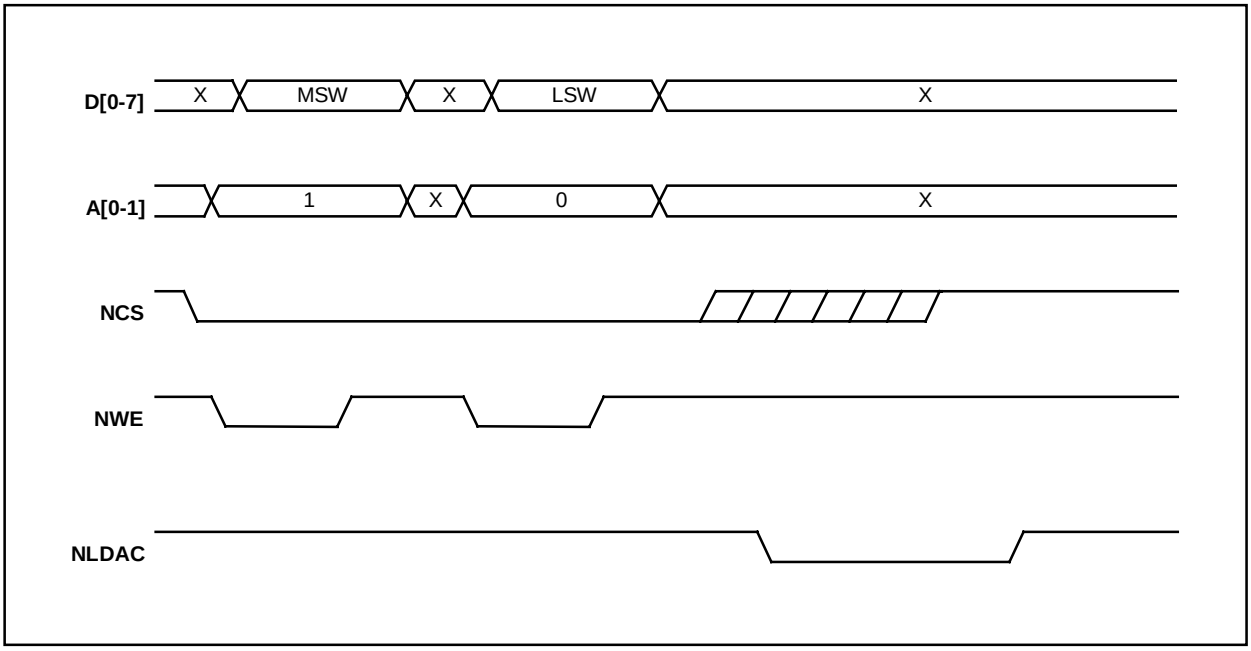


Figure 7 Example of a Complete Write Cycle Using NLDAC to Update the DAC

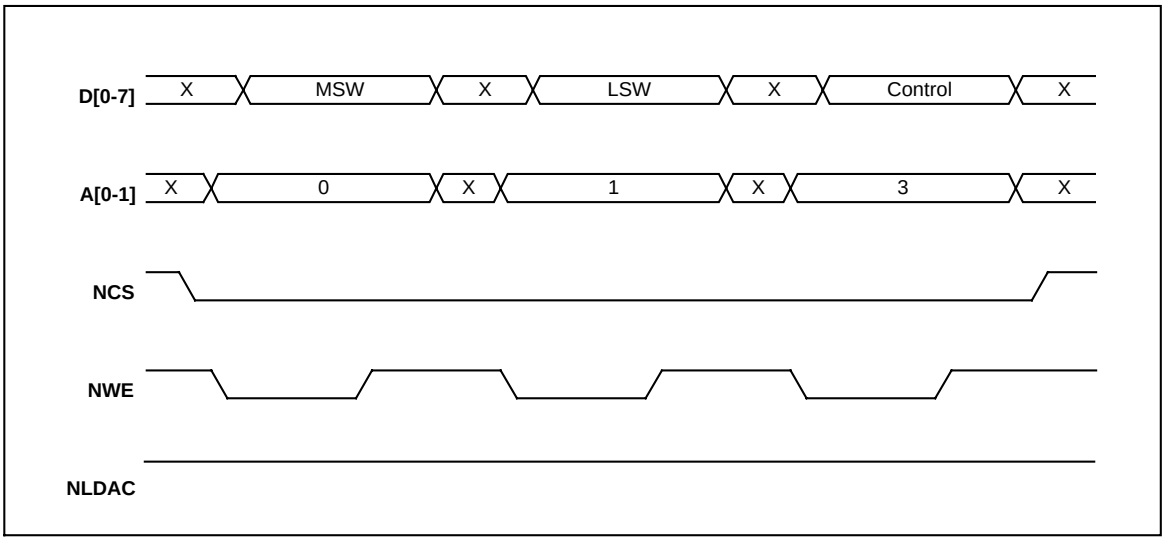


Figure 8 Example of a Complete Write Cycle Using the Control Word to Update the DAC. If NLDAC is held high as shown above, the DAC latch is normally closed, but can be made transparent by setting the RLDAC control register bit high. The procedure shown assumes that the RLDAC bit is low at the start and is written high on the final write.

SOFTWARE CONFIGURATION OPTIONS

DATA FORMAT

The WM2613 writes data either to one of the DAC holding latches or to the control register depending on the address bits A1 and A0.

A1	A0	LATCH	D7	D6	D5	D4	D3	D2	D1	D0
0	0	DAC LSW holding	DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC2	DAC 1	DAC 0
0	1	DAC MSW holding	X	X	X	X	DAC 11	DAC 10	DAC 9	DAC 8
1	0	Reserved	0	0	0	0	0	0	0	0
1	1	Control	X	X	X	REF1	REF0	RLDAC	PWR	SPD

Table 2 Register Map

PROGRAMMABLE SETTLING TIME

Settling time is a software selectable 3.5µs or 1µs, typical to within ±0.5LSB of final value. This is controlled by the value of SPD – Bit D12. A ONE defines a settling time of 1µs, a ZERO defines a settling time of 3.5µs.

PIN	BIT	MODE
SPD	SPD	
0	0	Slow
0	1	Fast
1	0	Fast
1	1	Fast

Table 3 Programmable Settling Time

PROGRAMMABLE POWER DOWN

The power down function can be controlled by PWR. A ZERO configures the device as active, or fully powered up, a ONE configures the device into power down mode. When the power down function is released the device reverts to the DAC code set prior to power down.

PIN	BIT	POWER
NPD	PWD	
0	0	Down
0	1	Down
1	0	Normal
1	1	Down

Table 4 Programmable Power Down

LOAD DAC LATCH

Bit RLDAC controls the function of the DAC latch. A ONE configures the DAC latch as transparent. A ZERO configures the DAC latch to be controlled by pin NLDAC.

PIN	BIT	LATCH
NLDAC	RLDAC	
0	0	Transparent
0	1	Transparent
1	0	Hold
1	1	Transparent

Table 5 Load DAC Latch

PROGRAMMABLE INTERNAL REFERENCE

The reference can be sourced internally or externally under software control. If an external reference voltage is applied to the REF pin, the device must be configured to accept this.

If an external reference is selected, the reference voltage input is buffered which makes the DAC input resistance independent of code. The REF pin has an input resistance of 10MΩ and an input capacitance of typically 55pF. The reference voltage determines the DAC full-scale output.

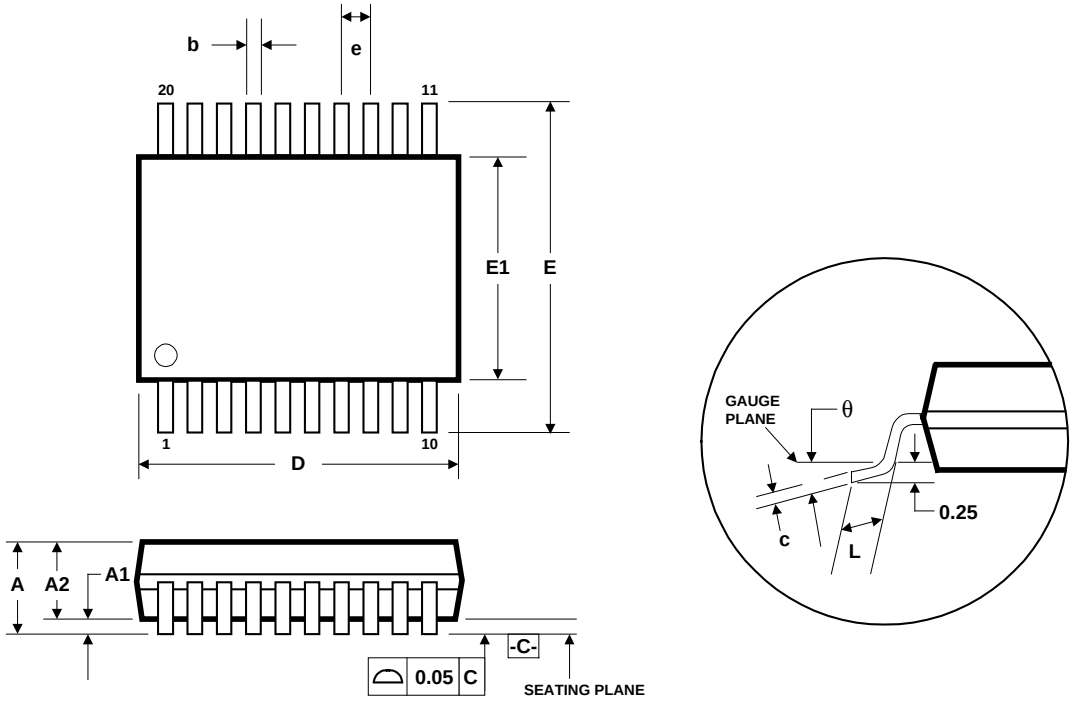
If an internal reference is selected, a voltage of 1.024V or 2.048 is available. The internal reference can source up to 1mA and can therefore be used as an external system reference.

REF1	REF0	REFERENCCE
0	0	External (default)
0	1	1.024V
1	0	2.048V
1	1	External

Table 6 Programmable Internal Reference

PACKAGE DIMENSIONS

DT: 20 PIN TSSOP (6.5 x 4.4 x 1.0 mm) **DM008.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	6.40	6.50	6.60
e	0.65 BSC		
E	6.4 BSC		
E_1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0^o	-----	8^o
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.