CMOS, 80 MHz Monolithic 256 Word Power-Down Color Palette RAM-DACs

ADV477/ADV475

ANALOG DEVICES

2

FEATURES

Personal System/2* and VGA* Compatible
80, 66, 50 and 35 MHz Pipelined Operation
ADV478/ADV471 (ADV®) Pin and Functional Compatible
Power-Down Mode
On-Board Voltage Reference
Antisparkle Circuit
Analog Output Comparators
ADV477:
- **Triple 8-Bit D/A Converters**
- **256 × 24 Color Palette RAM**
- **15 × 24 Overlay Registers**

ADV475:
- **Triple 6-Bit D/A Converters**
- **256 × 18 Color Palette RAM**
- **15 × 18 Overlay Registers**

RS-343A/RS-170 Compatible Outputs
Sync on all Three Channels
Programmable Pedestal
+5 V CMOS Monolithic Construction
44-Pin PLCC Package

APPLICATIONS

High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Laptop Computers
Desktop Publishing

AVAILABLE CLOCK RATES

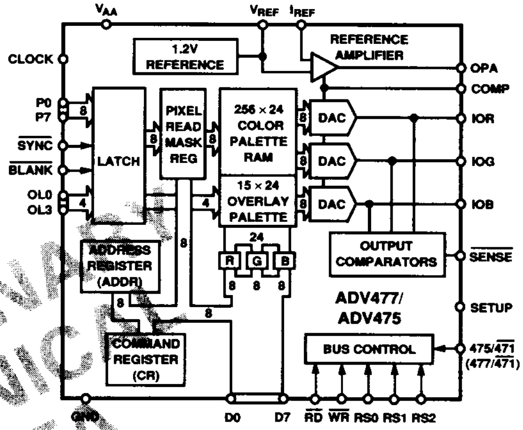
80 MHz
66 MHz
50 MHz
35 MHz

GENERAL DESCRIPTION

The ADV477 and ADV475 are pin-, functional-, and software-compatible RAM-DACs designed specifically for Personal System/2 (PS/2) compatible color graphics. They are a direct plug-in upgrade for the ADV478 and ADV471. Both support the existing 6-bit color VGA standard while also allowing for an upgrade path to 8-bit color resolution.

ADV is a trademark of Analog Devices, Inc.
*Personal System/2, PS/2, VGA and XGA are trademarks of International Business Machines Corp.

FUNCTIONAL BLOCK DIAGRAM



NOTE: PIN NAMES IN PARENTHESES DENOTE ADV477

The ADV477 has a 256 × 24 color lookup table with triple 8-bit video D/A converters. The ADV475 has a 256 × 18 color lookup table with triple 6-bit video D/A converters. New features on the ADV477/ADV475 include an on-board 1.2 V voltage reference, analog output comparators for self diagnostics and debugging as well as a power-down or sleep mode.

The power-down mode allows the ADV477/ADV475 to be put into a sleep mode with significant reduction in power consumption. This is ideal for laptop computers that may occasionally require the optional ability to drive an analog RGB monitor, but whose design is dictated by a desire to minimize power consumption.

Options on both parts include a programmable pedestal (0 or 7.5 IRE) and use of an external voltage or current reference. 15 overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc., at the hardware level. Also supported is a pixel read mask register and the ability to encode sync information on all three channels.

The ADV477/ADV475 generates RS343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADV477/ADV475—SPECIFICATIONS

(V_{AA}[1] = 5 V; SETUP = 477/$\overline{471}$ = V_{AA}; V_{REF} = 1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted.)

Parameter	ADV477	ADV475	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution (Each DAC)	8	6	Bits	
Accuracy (Each DAC)				
Integral Nonlinearity	±1	±0.25	LSB max	
Differential Nonlinearity	±1	±0.25	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	±5	% Gray Scale	
Coding			Binary	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2	2	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	7	7	pF max	f = 1 MHz, V_{IN} = 2.4 V
DIGITAL OUTPUTS				
Output High Voltage, V_{OH}	2.4	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	50	50	μA max	
Floating-State Leakage Capacitance	7	7	pF max	
ANALOG OUTPUTS				
Gray Scale Current Range	20	20	mA max	
Output Current				
White Level Relative to Black	16.74	16.74	mA min	Typically 17.62 mA
	18.50	18.50	mA max	
Black Level Relative to Blank	0.95	0.95	mA min	Typically 1.44 mA, SETUP = V_{AA}
(Pedestal = 7.5 IRE)	1.90	1.90	mA max	
Black Level Relative to Blank	0	0	μA min	Typically 5 μA, SETUP = GND
(Pedestal = 0 IRE)	50	50	μA max	
Blank Level	6.29	6.29	mA min	Typically 7.62 mA
(Sync Enabled)	8.96	8.96	mA max	
Blank Level	0	0	μA min	Typically 5 μA
(Sync Disabled)	50	50	μA max	
Sync Level	0	0	μA min	Typically 5 μA
	50	50	μA max	
LSB size	69.1	279.68	μA typ	
DAC to DAC Matching	5	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	−1	V min	
	+1.5	+1.5	V max	
Output Capacitance, C_{OUT}	30	30	pF max	f = 1 MHz, I_{OUT} = 0 mA
Output Impedance, R_{OUT}	10	10	kΩ typ	
VOLTAGE REFERENCE				
Internal Voltage Reference	1.1/1.3	1.1/1.3	V min/V max	Typically 1.235 V
External Voltage Reference Range	1.14/1.26	1.14/1.26	V min/V max	
POWER SUPPLY				
Supply Voltage, V_{AA}	4.75/5.25	4.75/5.25	V min/V max	80 MHz and 66 MHz Parts
	4.50/5.50	4.50/5.50	V min/V max	50 MHz and 35 MHz Parts
Supply Current, I_{AA}				
Normal Operation	200	200	mA max	Typically 160 mA
Power Down Mode[3]	10	10	mA max	Typically 5 mA
Power Supply Rejection Ratio	0.5	0.5	%/% max	f = 1 kHz, COMP = 0.1 μF
DYNAMIC PERFORMANCE				
Clock and Data Feedthrough[4, 5]	−30	−30	dB typ	
Glitch Impulse[4, 5]	75	75	pV secs typ	
DAC to DAC Crosstalk[6]	−23	−23	dB typ	

NOTES

[1] ±5% for 80 MHz and 66 MHz parts; ±10% for 50 MHz and 35 MHz parts.

[2] Temperature Range (T_{MIN} to T_{MAX}): 0°C to + 70°C.

[3] External Voltage/Current Reference disabled. Temperature: +25 °C to +70 °C. All digital inputs at 0.4 V.

[4] Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.

[5] TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured the 10% and 90% points. Timing reference points at 50% for inputs and outputs.

[6] DAC-to-DAC Crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = 5 V; SETUP = 477/$\overline{471}$ = V_{AA}; V_{REF} = 1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 147 Ω. All specifications T_{MIN} to T_{MAX}[3], unless otherwise noted.)

Parameter	80 MHz Version	66 MHz Version	50 MHz Version	35 MHz Version	Units	Conditions/Comments
f_{max}	80	66	50	35	MHz	Clock Rate
t_1	10	10	10	10	ns min	RS0–RS2 Setup Time
t_2	10	10	10	10	ns min	RS0–RS2 Hold Time
t_3[4]	5	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4[4]	40	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5[5]	20	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6[5]	5	5	5	5	ns min	Read Data Hold Time
t_7	10	10	10	10	ns min	Write Data Setup Time
t_8	10	10	10	10	ns min	Write Data Hold Time
t_9	50	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_{10}	$6 \times t_{13}$	$6 \times t_{13}$	$6 \times t_{13}$	$6 \times t_{13}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{11}	3	3	3	3	ns min	Pixel and Control Setup Time
t_{12}	3	3	3	3	ns min	Pixel and Control Hold Time
t_{13}	12.5	15.15	20	28	ns min	Clock Cycle Time
t_{14}	4	5	6	7	ns min	Clock Pulse Width High Time
t_{15}	4	5	6	9	ns min	Clock Pulse Width Low Time
t_{16}	30	30	30	30	ns max	Analog Output Delay
t_{17}	3	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{18}[6]	13	13	20	28	ns max	Analog Output Settling Time
t_{19}	1	1	1	1	µs typ	$\overline{SENSE}$ Output Delay
t_{SK}	2	2	2	2	ns max	Analog Output Skew
t_{PD}	$4 \times t_{13}$	$4 \times t_{13}$	$4 \times t_{13}$	$4 \times t_{13}$	ns min	Pipeline Delay

NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figure 2a.

[2]±5% for 80 MHz and 66 MHz parts; ±10% for 50 MHz and 35 MHz parts.

[3]Temperature Range (T_{MIN} to T_{MAX}): 0°C to +70°C.

[4]t_3 and t_4 are measured with the load circuit of Figure 3 and are defined as the time required for an output to cross 0.4 V or 2.4 V.

[5]t_5 and t_6 are derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the times, t_5 and t_6, quoted in the timing characteristics are the true values for the device and as such are independent of external bus loading capacitances.

[6]Settling time does not include clock and data feedthrough.

Specifications subject to change without notice.

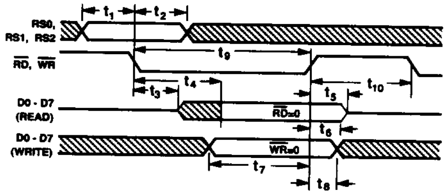


Figure 1. MPU Read/Write Timing

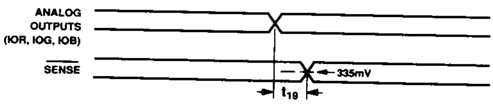
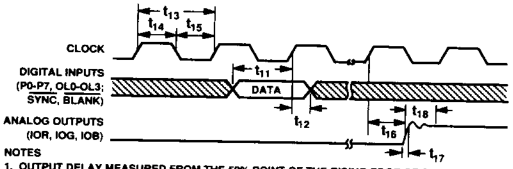


Figure 2b. Video Output vs. SENSE Timing



NOTES
1. OUTPUT DELAY MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. SETTLING TIME MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1 LSB (ADV477) AN ±0.25 LSBs (ADV475).
3. OUTPUT RISE/FALL TIME MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION

Figure 2a. Video Input/Output Timing

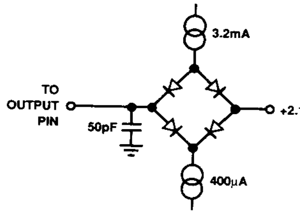


Figure 3. Load Circuit for Bus Access and Relinquish Time

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}				
80 MHz, 66 MHz Parts		4.75	5.00	5.25	Volts
50 MHz, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Current Reference Configuration					
I_{REF} Current	I_{REF}				
Standard RS-343A		−3	−8.39	−10	mA
PS/2 Compatible		−3	−8.88	−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . 7 V
Voltage on any Digital Pin . . . GND − 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . 220°C
IOR, IOG, IOB to GND[1] . . . . 0 V to V_{AA}

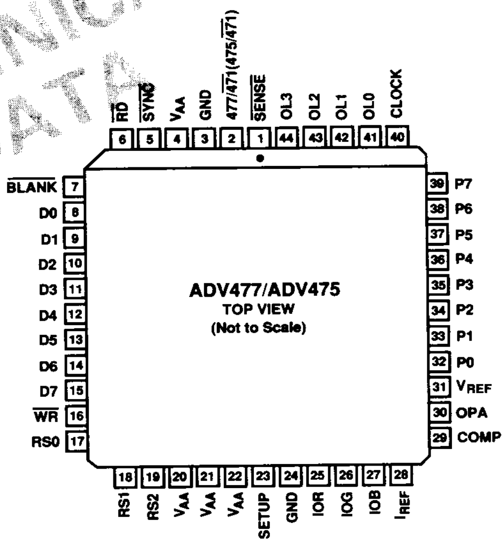
NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

PIN CONFIGURATION

PLCC



ORDERING GUIDE

Model	Speed	DAC Resolution	Palette Size	Temperature Range	Package Option*
ADV477KP80	80 MHz	8-Bit	256 × 24	0°C to +70°C	P-44A
ADV477KP66	66 MHz	8-Bit	256 × 24	0°C to +70°C	P-44A
ADV477KP50	50 MHz	8-Bit	256 × 24	0°C to +70°C	P-44A
ADV477KP35	35 MHz	8-Bit	256 × 24	0°C to +70°C	P-44A
ADV475KP80	80 MHz	6-Bit	256 × 18	0°C to +70°C	P-44A
ADV475KP66	66 MHz	6-Bit	256 × 18	0°C to +70°C	P-44A
ADV475KP50	50 MHz	6-Bit	256 × 18	0°C to +70°C	P-44A
ADV475KP35	35 MHz	6-Bit	256 × 18	0°C to +70°C	P-44A

*P = Plastic Leaded (J-Lead) Chip Carrier (PLCC). For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{BLANK}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level. It is latched on the rising edge of CLOCK. When $\overline{BLANK}$ is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.
$\overline{SYNC}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs. $\overline{SYNC}$ does not override any other control or data input; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC, and $\overline{BLANK}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable.
I_{REF}	Full-scale adjust control. Note that the IRE relationships are maintained, regardless of the full-scale output current.

When using an external voltage reference, a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is:

$$R_{SET}(\Omega) = K \times 1{,}000 \times V_{REF}(v) / I_{OUT}(mA)$$

K is defined in the table below. It is recommended that a 147 Ω value of R_{SET} resistor be used for doubly terminated 75 Ω loads (RS-343A applications). For PS/2 applications, where 0.7 V is driven into 50 Ω and which doesn't have $\overline{SYNC}$ encoded, a 182 Ω resistor is recommended.

When using an external current reference, the relationship between I_{REF} and the full-scale output current on each output is:

$$I_{REF}(mA) = I_{OUT}(mA) / K$$

Part	Color Resolution	Pedestal	K ($\overline{SYNC}$ Enabled)	K ($\overline{SYNC}$ Disabled)
ADV477	6-Bit	7.5 IRE	3.170	2.26
	8-Bit	7.5 IRE	3.195	2.28
	6-Bit	0 IRE	3.000	2.10
	8-Bit	0 IRE	3.025	2.12
ADV475	6-Bit	7.5 IRE	3.170	2.26
	8-Bit	0 IRE	3.000	2.10

Pin Mnemonic	Function
COMP	Compensation pin. If an external voltage reference is used, this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1 µF ceramic capacitor must always be used to bypass this pin to V_{AA}.
V_{REF}	Voltage reference input. If an external voltage reference is used, it must supply this input with a 1.2v (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must always be used to decouple this input to V_{AA}. When using the internal reference circuitry, this pin should only be connected to the bypass capacitor.
OPA	Reference amplifier output. If an external voltage reference is used, this pin must be connected to COMP. When using an external current reference, this pin should be left floating.

PIN FUNCTION DESCRIPTION (continued)

Pin Mnemonic	Function
V_{AA}	Analog power. All V_{AA} pins must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{WR}$	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{WR}$, and RS0–RS2 are latched on the falling edge of $\overline{WR}$ during MPU write operations.
$\overline{RD}$	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0–RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.
475/$\overline{471}$ (477/$\overline{471}$)	ADV475 (ADV477) or ADV471 select input (TTL compatible). When this input is floating or a logical zero, the ADV477/ADV475 behaves exactly as an ADV471 with antisparkle capabilities. When this input is at a logical one, the extra capabilities of the ADV477/ADV475 are available. The Command Register (CR) becomes active.
$\overline{SENSE}$	Sense Output (TTL compatible). $\overline{SENSE}$ is a logical zero if one or more of the IOR, IOG and IOB outputs have exceeded the internal voltage reference level (335 mV).

TERMINOLOGY

BLANKING LEVEL
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

COLOR VIDEO (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

COMPOSITE SYNC SIGNAL (SYNC)
The position of the composite video signal which synchronizes the scanning process.

COMPOSITE VIDEO SIGNAL
The video signal with or without setup, plus the composite SYNC signal.

GRAY SCALE
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

RASTER SCAN
The most basic method of sweeping a CRT one line at a time to generate and display images.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

SETUP
The difference between the Reference Black level and the blanking level.

SYNC LEVEL
The peak level of the composite SYNC signal.

VIDEO SIGNAL
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION

MPU Interface
The ADV477 and ADV475 support a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

Three address decode lines, RS0–RS2, specify whether the MPU is accessing the address register, the color palette RAM, the overlay registers, or read mask register. These controls also determine whether this access is a read or write function. Table I illustrates this decoding. The 8-bit address register is used to address the contents of the color palette RAM and overlay registers.

Table I. Control Input Truth Table

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Registers
1	1	0	Command Register*

*Available only when the 475/471 (477/471) pin is a logic "1."

Color Palette Writes
The MPU writes to the address register (selecting RAM write mode, RS2 = 0, RS1 = 0 and RS0 = 0) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM (RS2 = 0, RS1 = 0, RS0 = 1). After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word or an 18-bit word and are written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A complete set of colors can be loaded into the palette by initially writing the start address and then performing a sequence of red, green and blue writes. The address automatically increments to the next highest location after a blue write.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Color Palette Reads

The MPU writes to the address register (selecting RAM read mode, RS2 = 0, RS1 = 1 and RS0 = 1) with the address of the color palette RAM location to be read back. The contents of the palette RAM are copied to the red, green and blue registers and the address register increments to point to the next palette RAM location. The MPU then perform three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM (RS2 = 0, RS1 = 0, RS0 = 1). After the blue read cycle, the 24/18 bit contents of the palette RAM at the location specified by the address register is loaded into the red, green and blue registers. The address register then increments to the next location which the MPU can read back by simply reading another sequence of red, green, and blue data. A complete set of colors can be read back from the palette by initially writing the start address and then performing a sequence of red, green and blue reads. The address automatically increments to the next highest location after a blue read.

Overlay Color Writes

The MPU writes to the address register (selecting OVERLAY REGISTER write mode, RS2 = 1, RS1 = 0 and RS0 = 0) with the address of the overlay register to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers (RS2 = 1, RS1 = 0, RS0 = 1). After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word or an 18-bit word and written to the overlay register specified by the address register. The address register then increments to the next overlay register which the MPU may modify by simply writing another sequence of red, green, and blue data. A complete set of colors can be loaded into the overlay registers by initially writing the start address and then performing a sequence of red, green and blue writes. The address automatically increments to the next highest location after a blue write.

Overlay Color Reads

The MPU writes to the address register (selecting OVERLAY REGISTER read mode, RS2 = 1, RS1 = 1 and RS0 = 1) with the address of the overlay register to be read back. The contents of the overlay register are copied to the red, green and blue registers and the address register increments to point to the next highest overlay register. The MPU then perform three successive read cycles (8 or 6 bits each of red, green, and blue), using RS0–RS2 to select the Overlay Registers (RS2 = 1, RS1 = 0, RS0 = 1). After the blue read cycle, the 24/18 bit contents of the overlay register at the specified address register location is loaded into the red, green and blue registers. The address register then increments to the next overlay register which the MPU can read back by simply reading another sequence of red, green, and blue data. A complete set of colors can be read back from the overlay registers by initially writing the start address and then performing a sequence of red, green and blue reads. The address automatically increments to the next highest location after a blue read.

Internal Address Register (ADDR)

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits (since there are only 15 overlay registers) of the address register (ADDR4–7) are ignored.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Note: The pixel clock must be active for MPU accesses to the color palette.

Synchronization

The MPU interface operates asynchronously to the pixel port. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B as shown in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Internal circuitry has been included to reduce noticeable sparkling on some CRT systems which can occur during MPU accesses to the color palette RAM.

Table II. Address Register (ADDR) Operation

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (Counts Modulo 3)	00				Red Value
	01				Green Value
	10				Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	0	1	Color Palette RAM
	xxxx 0000	1	0	1	Reserved
	xxxx 0001	1	0	1	Overlay Color 1
	xxxx 0010	1	0	1	Overlay Color 2
	.	.	.	.	.
	.	.	.	.	.
	xxxx 1111	1	0	1	Overlay Color 15

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADV471 Compatibility

The ADV477/ADV475 can be made to operate as an ADV471 by setting the 477/471 input of the ADV477 and 475/471 input of the 475/471 to a logic "0". The internal Command Register (CR) is disabled and 6-bit color resolution is automatically selected. Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical "0." It should be noted that when the ADV477 is in 6-bit mode, full-scale output current will be reduced by approximately 1.5% relative to the 8-bit mode. This is the case since the 2 LSBs of each of the three DACs are always set to zero in 6-bit mode.

ADV477/ADV475 Enhancements

The enhanced modes of operation provided by the ADV477/ADV475 can be implemented when the 477/471 and 475/471 pins on the ADV477 and ADV475, respectively, are at a logic "1." The internal Command Register (CR) now becomes active, thereby allowing for full programmability of these enhanced modes. Command bit CR1 sets the ADV477 to operate in 6-bit or 8-bit color resolution.

Command Register (CR)

The ADV477/ADV475 has an internal command register which becomes active when the 475/$\overline{471}$ (477/$\overline{471}$) pin is a logic "1." This register is 8 bits wide, CR0–CR7 and is directly mapped to the MPU data bus on the part, D0–D7. The command register can be written to or read from. It is not initialized, therefore it must be set if the 477/471 (475/471) pin is high. Figure 4 shows what each bit of the CR register controls and shows the values it must be programmed to for various modes of operation.

Power-Down Mode

The ADV477/ADV475 can be placed into a power-down or sleep mode. This is especially useful in power sensitive systems such as portable or lap-top computers. This power-down mode is controlled by the Power-Down bit (CR0) of the command register. When CR0 is "0", the device goes into power-down mode. When CR0 is "1", the part operates normally.

The power to three DACs and the RAM is turned off while CR0 is low. The contents of the palette RAM, however, remain valid in the power-down state and normal read/write operations can be made to the part over the MPU port. During the actual read/write operations (when CR0 = 0) the RAM will be temporarily powered up, and on completion of MPU accesses the RAM returns to its shut-down state.

The three DACs in the ADV477/ADV475 will be shut off in the power-down mode only when the part is operated in the voltage reference configuration (internal or external reference). A further decrease in power consumption can be achieved by turning off the external voltage reference.

If operating in the current reference configuration, the I_{REF} current needs to be reduced to 0 mA when in the power-down mode, in order to minimize the total power consumption.

On-Board Comparators and $\overline{\text{SENSE}}$ Control

The three on-board comparators can be used in conjunction with the $\overline{\text{SENSE}}$ output control to determine whether or not a CRT is connected to the RGB analog outputs.

$\overline{\text{SENSE}}$ will be a logic "0" if the voltage on one or more of the IOR, IOG and IOB outputs is greater than the internal voltage reference level of 335 mV. A loaded ($\overline{\text{SENSE}}$ = "1") and unloaded ($\overline{\text{SENSE}}$ = "0") RGB line is now discernible.

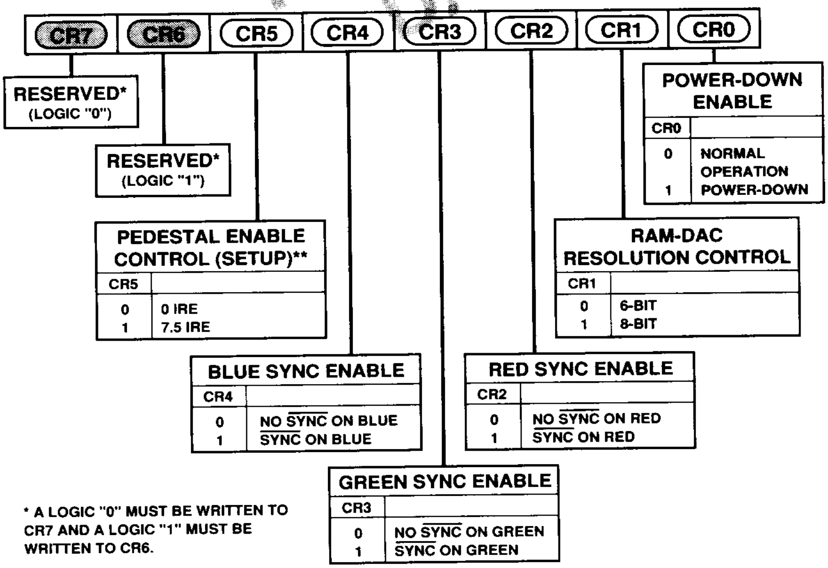


Figure 4. Command Register (CR)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

This internal voltage reference level has a ±5% tolerance when using an external voltage reference. A tolerance of ±10% is achievable with the ADV477/ADV475's internal voltage reference.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs, which are latched in on the rising edge of CLOCK, are used to address the color palette RAM and overlay registers, as shown in Table III. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides an RGB word (24 bits for the ADV477 and 18 bits for the ADV475) of color information for the three RGB D/A converters.

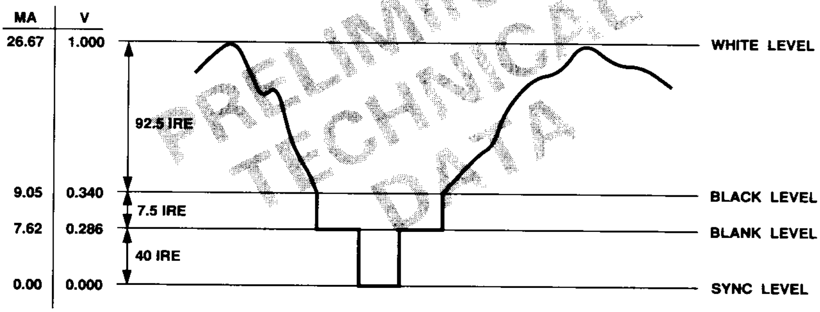
The SYNC and BLANK inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 5 and 6. Tables IV and V detail how the SYNC and BLANK inputs modify the output levels.

Table III. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = FFH)

OL0–OL3	P0–P7	Addressed by Frame Buffer
0H	00H	Color Palette RAM Location 00H
0H	01H	Color Palette RAM Location 01H
.	.	.
.	.	.
0H	FFH	Color Palette RAM Location FFH
1H	xxH	Overlay Color 1
2H	xxH	Overlay Color 2
.	.	.
.	.	.
FH	xxH	Overlay Color 15

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.

The analog outputs of the ADV477 and ADV475 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = V_{AA}.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67 mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

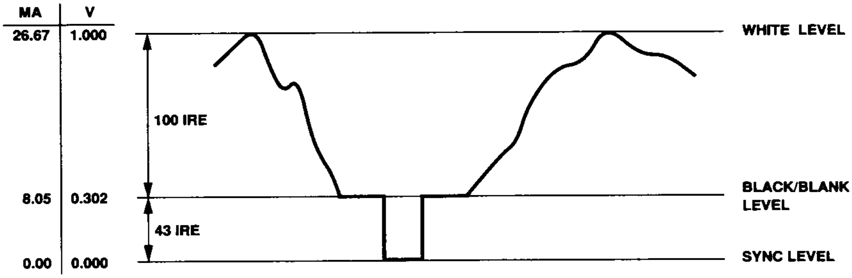
Figure 5. Composite Video Output Waveform (SETUP = V_{AA})

Table IV. Video Output Truth Table (SETUP = V_{AA})

Description	I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	data + 9.05	1	1	data
DATA-SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK	7.62	1	0	xxH
SYNC	0	0	0	xxH

NOTES
1. Typical with full scale 10G = 26.67 mA, SETUP = V_{AA}.
2. External voltage or current reference adjusted for 26.67 mA full-scale output.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = GND.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 6. Composite Video Output Waveform (SETUP = GND)

Table V. Video Output Truth Table (SETUP = GND)

Description	I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	FFH
DATA	data + 8.05	1	1	data
DATA-SYNC	data	0	1	data
BLACK	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK	8.05	1	0	xxH
SYNC	0	0	0	xxH

NOTES
1. Typical with full scale IOG = 26.67 mA, SETUP = V_{AA}.
2. External voltage or current reference adjusted for 26.67 mA full-scale output.

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the ADV477/ADV475 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV477/ADV475 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the ADV477/ADV475, the analog output traces, and all the digital signal traces leading up to the ADV477/ADV475.

Power Planes

The ADV477/ADV475 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 7, 8 and 9. This bead should be located within three inches of the ADV477/ADV475.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV477/ADV475 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV475 and ADV477 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV477/ADV475 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Due to the high clock rates involved, long clock lines to the ADV477/ADV475 should be avoided to reduce noise pickup.

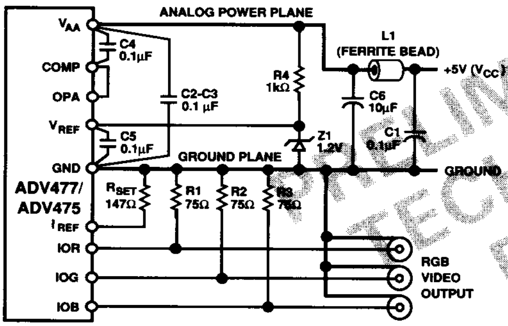
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV477/ADV475 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

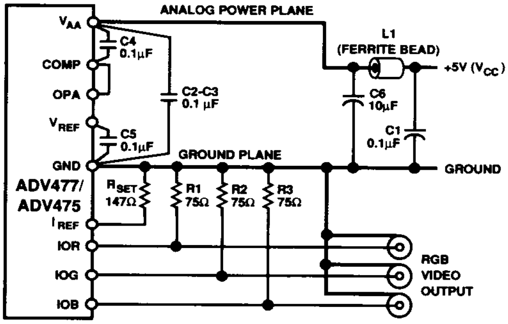
The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV477/ADV475 to minimize reflections.



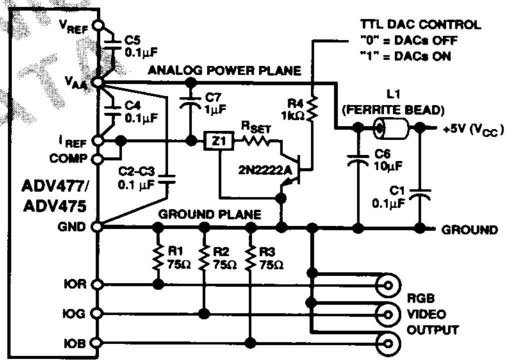
COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
R4	1kΩ 5% RESISTOR	
R_{SET}	1% METAL FILM RESISTOR	
Z1	1.23V VOLTAGE REFERENCE	AD589JN

Figure 7. Typical Connection Diagram (External Voltage Reference)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
R_{SET}	1% METAL FILM RESISTOR	

Figure 8. Typical Connection Diagram (Internal Voltage Reference)



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
C7	1µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF
Z1	ADJUSTABLE REGULATOR	LM317LZ
R_{SET}	1% METAL FILM RESISTOR	

Figure 9. Typical Connection Diagram (External Current Reference)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.