Winbond Electronics Corp.

8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The W78E516 is an 8-bit microcontroller which has an in-system programmable MTP-ROM for on-chip firmware updating. The instruction set of the W78E516 is fully compatible with the standard 8052. The W78E516 contains a 64K bytes of main MTP-ROM and a 4K bytes of auxiliary MTP-ROM which allows the contents of the 64KB main MTP-ROM to be updated by the loader program located in the 4KB MTP-ROM; a 512 bytes of RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; a serial port. These peripherals are supported by a six sources two-level interrupt capability. To facilitate programming and verification, the MTP-ROM inside the W78E516 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E516 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

FEATURES

- Fully static design 8-bit CMOS microcontroller up to 40MHz.
- 64K bytes of in-system programmable MTP-ROM for Application Program (APROM).
- 4K bytes of auxiliary MTP-ROM for Loader Program (LDROM).
- 512 bytes of on-chip RAM. (including 256 bytes of AUX-RAM, software selectable)
- 64K bytes program memory address space and 64K bytes data memory address space.
- Four 8-bit bi-directional ports.
- One 4-bit general purpose I/O port.
- Three 16-bit timer/counters
- One full duplex serial port
- Six-sources, two-level interrupt capability
- Built-in power management
- Code protection
- PACKAGE

-DIP 40 :W78E516-24/40
-PLCC 44 :W78E516P-24/40
-PQFP 44: W78E516F-24/40
-TQFP 44: W78E516M-24/40

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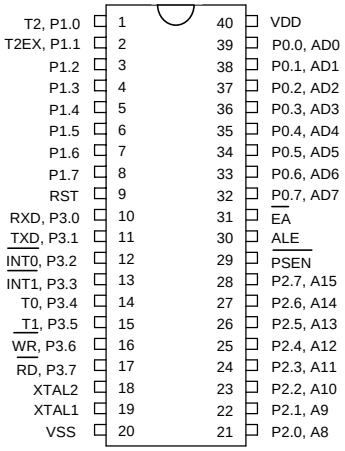
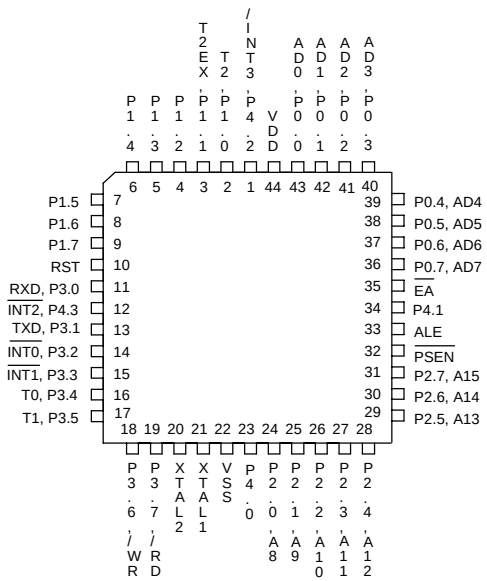
PIN CONFIGURATIONS :

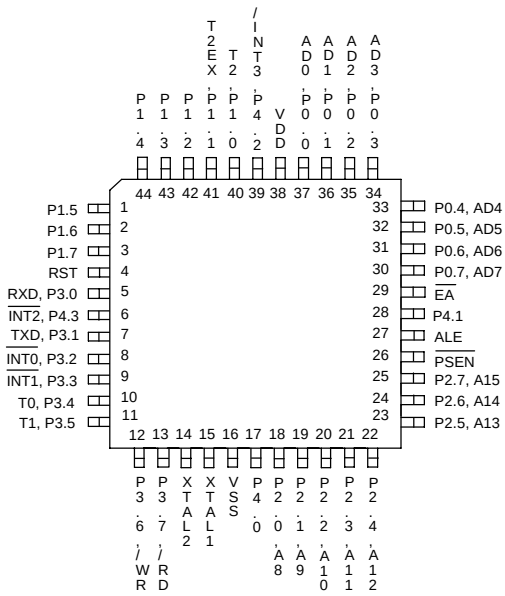
40-Pin DIP (W78E516)



44-Pin PLCC (W78E516P)



44-Pin QFP/TQFP (W78E516F/W78E516M)



PIN DESCRIPTION

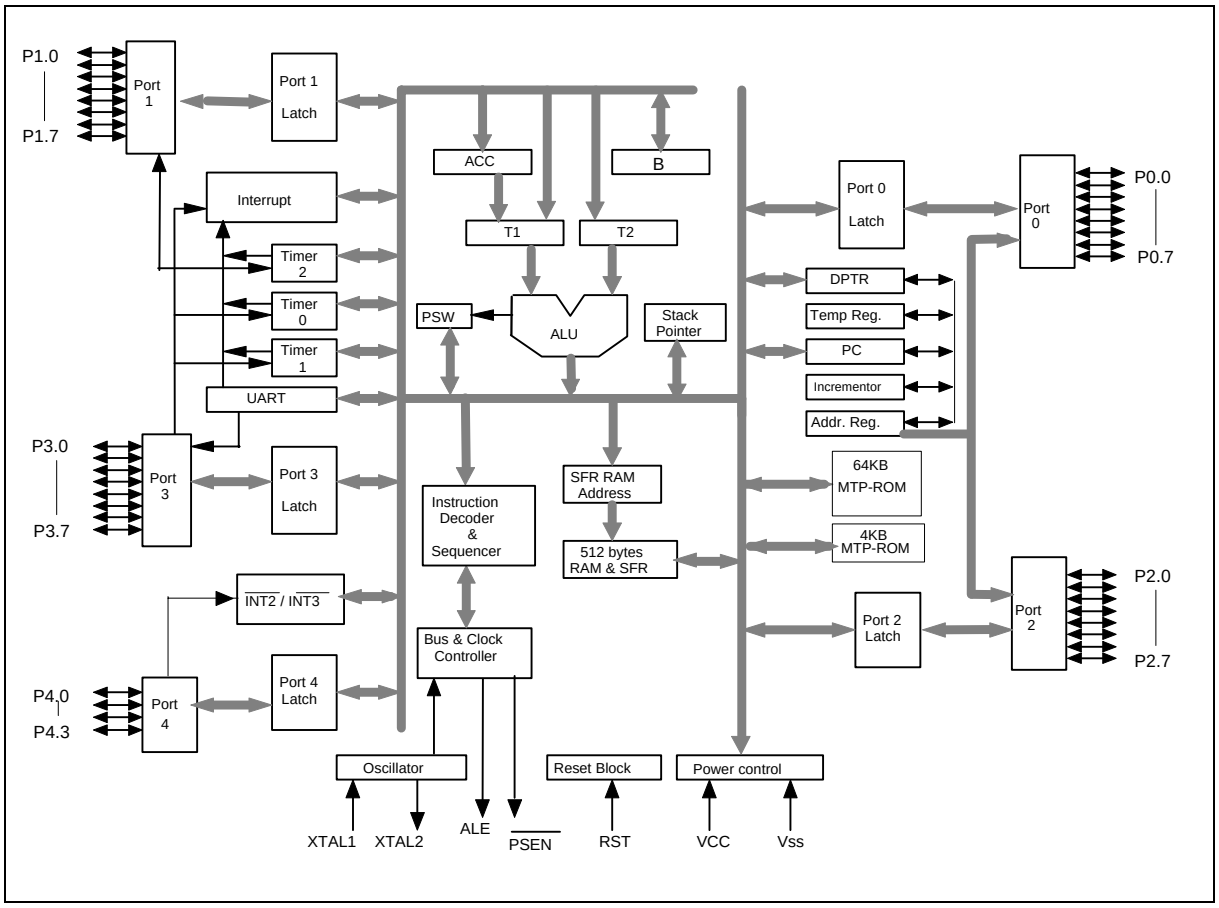
SYMBOL	TYPE	DESCRIPTIONS
EA	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be present on the bus if the $\overline{EA}$ pin is high and the program counter is within the 48 KB area. Otherwise they will be present on the bus.
PSEN	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0–P0.7	I/O D	PORT 0: Function is the same as that of the standard 8052.
P1.0–P1.7	I/O H	PORT 1: Function is the same as that of the standard 8052.
P2.0–P2.7	I/O H	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups.
P3.0–P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0–P4.3	I/O H	PORT 4: A bi-directional I/O port with alternate function. See details below.

* Note : **TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

Port 4

Port 4, SFR P4 at address D8H, P4.0~P4.3 is a bi-directional I/O port which is same as port 1. P4.2 and P4.3 also serve as external interrupt INT3 and INT2 if enabled.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The W78E516 architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 512 bytes of RAM, three timer/counters, a serial port ,and an internal 74373 latch and 74244 buffer which can be switched to port2. The processor supports 111 different opcodes and references both a 64K program address space and a 64 K data storage space.

RAM

The internal data RAM in W78E516 is 512x 8 bytes. It is divided into two banks: 256 bytes of RAM and 256 bytes of AUX-RAM . These RAMs are addressed by different ways.

- RAM 0H ~127H can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.
- RAM 128H~255H can only be addressed indirectly as the same as in 8051. Address pointers are R0,R1 of the selected registers bank.

- AUX-RAM 0H~255H is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. An access to external data memory locations higher than 255 will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is disable after power-on reset. Setting the bit 4 in CHPCON register will enable the access to AUX-RAM. When AUX-RAM is enabled the instructions of "MOVX @Ri" will always access to the on-chip AUX-RAM.

On-Chip MTP-ROM

The W78E516 includes one 64K bytes of main MTP-ROM for application program (APROM) and one 4K bytes of MTP-ROM for loader program (LDROM) when operating the in-system programming feature. In normal operation, the microcontroller will excute the code from the 64K bytes of main MTP-ROM. By setting program registers, user can force microcontroller to switch to the the programming mode which microcontroller will excute the code (loader program) from the 4K bytes of auxiliary MTP-ROM, and this loader program is going to update the contents of the 64K bytes of main MTP-ROM. After reset, the microcontroller executes the new application program in the main MTP-ROM. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programmimg feature make it possible that the end-user is able to easily update the system firmware by themselve without opening the chassis.

Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

$\overline{\text{INT2}}$ / $\overline{\text{INT3}}$

Two additional external interrupts, $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

*****XICON - external interrupt control (C0H)**

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Eight-source interrupt informations:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

Clock

The W78E516 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E516 relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78E516 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks, including the oscillator are stopped. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to

deglitch the reset line when the W78E516 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

W78E516 Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B 00000000						**CHPENR 00000000**		F7
E8									EF
E0	+ACC 00000000								E7
D8	**+P4 xxxx1111**								DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000		RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XCION 00000000								C7
B8	+IP 00000000								BF
B0	+P3 00000000								B7
A8	+IE 00000000								AF
A0	+P2 11111111								A7
98	+SCON 00000000	SBUF xxxxxxxx							9F
90	+P1 11111111								97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00110000	87

Note: 1.The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

In-System Programming Mode Enable Register (CHPENR) (F6H)

The CHPCON is read only by default .You must write #87, #59H sequentially to this special register CHPENR to enable the CHPCON write attribute, and write other value to disable CHPCON write attribute. This register protects from writing to the CHPCON register carelessly.

SFRAH,SFRAL: The objective address of on-chip MTP-ROM in programming mode. SFRFAH contains the high-order byte of address, SFRFAL contains the low-order byte of address.

SFRFD : The programming data for on-chip flash memory in programming mode.

SFRCN : The control byte of on-chip flash memory programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip MTP-ROM bank select for in-system programming. =0 : 64K bytes MTP-ROM bank is selected as destination for re-programming. =1 : 4K bytes MTP-ROM bank is selected as destination for re-programming.
5	OEN	MTP-ROM output enable.
4	CEN	MTP-ROM chip enable.
3,2,1,0	CTRL[3:0]	The flash control signals

Mode	CTRL<3:0>	WFWIN	OEN	CEN	SFRAH,SFRAL	SFRFD
Erase 64KB APROM	0010	0	1	0	X	X
Program 64KB APROM	0001	0	1	0	Address in	Data in
Read 64KB APROM	0000	0	0	0	Address in	Data out

In-System Programming Control Register (CHPCON)

CHPCON (BFH)

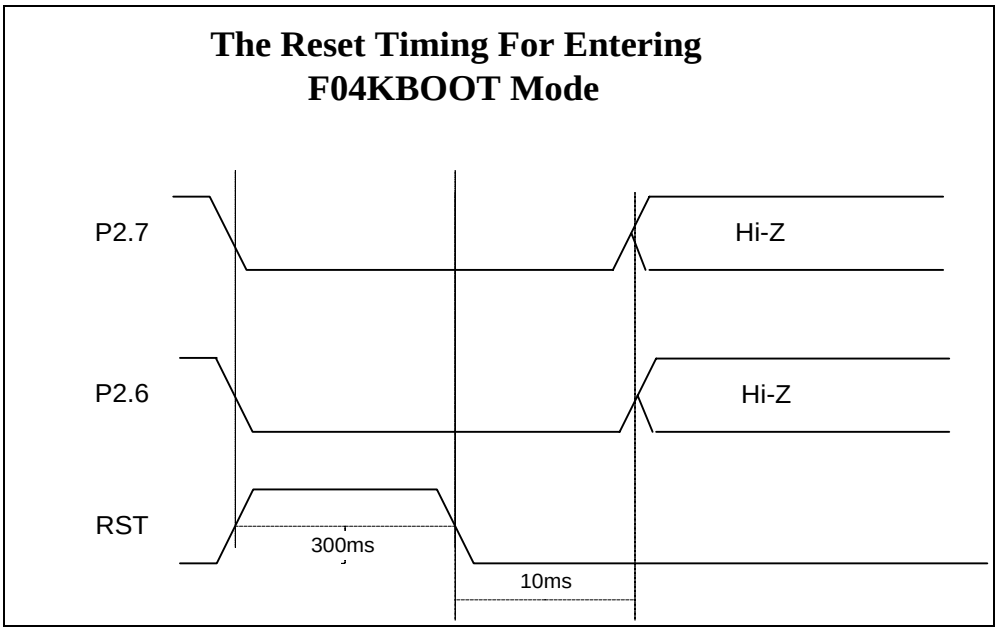
BIT	NAME	FUNCTION
7	SWRESET (F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit can determine that the F04KBOOT mode is running.
6	-	Reserve.
5	-	Reserve.
4	ENAUXRAM	=1: Enable on-chip AUX-RAM. =0: Disable the on-chip AUX-RAM
3	0	must set to 0.
2	0	must set to 0.
1	FBOOTSL	The Loader Program Location Select. 0: The Loader Program locates at the 64KB flash memory bank. 1: The Loader Program locates at the 4KB flash memory bank.
0	FPROGEN	MTP-ROM Programming Enable 1:enable. The microcontroller switches to the programming flash mode after entering the idle mode and waken up from interrupt. The microcontroller will execute the loader program while in on-chip programming mode. 0:disable. The on-chip flash memory is read-only. In-system programmability is disabled.

F04KBOOT Mode (Boot From 4K bytes of LDROM)

The W78E516 boots from APROM program (64K bytes) by default at power on reset. On some occasions, user can force the W78E516 to boot from the LDROM program (4K bytes) at a power on reset via following settings.

F04KBOOT MODE

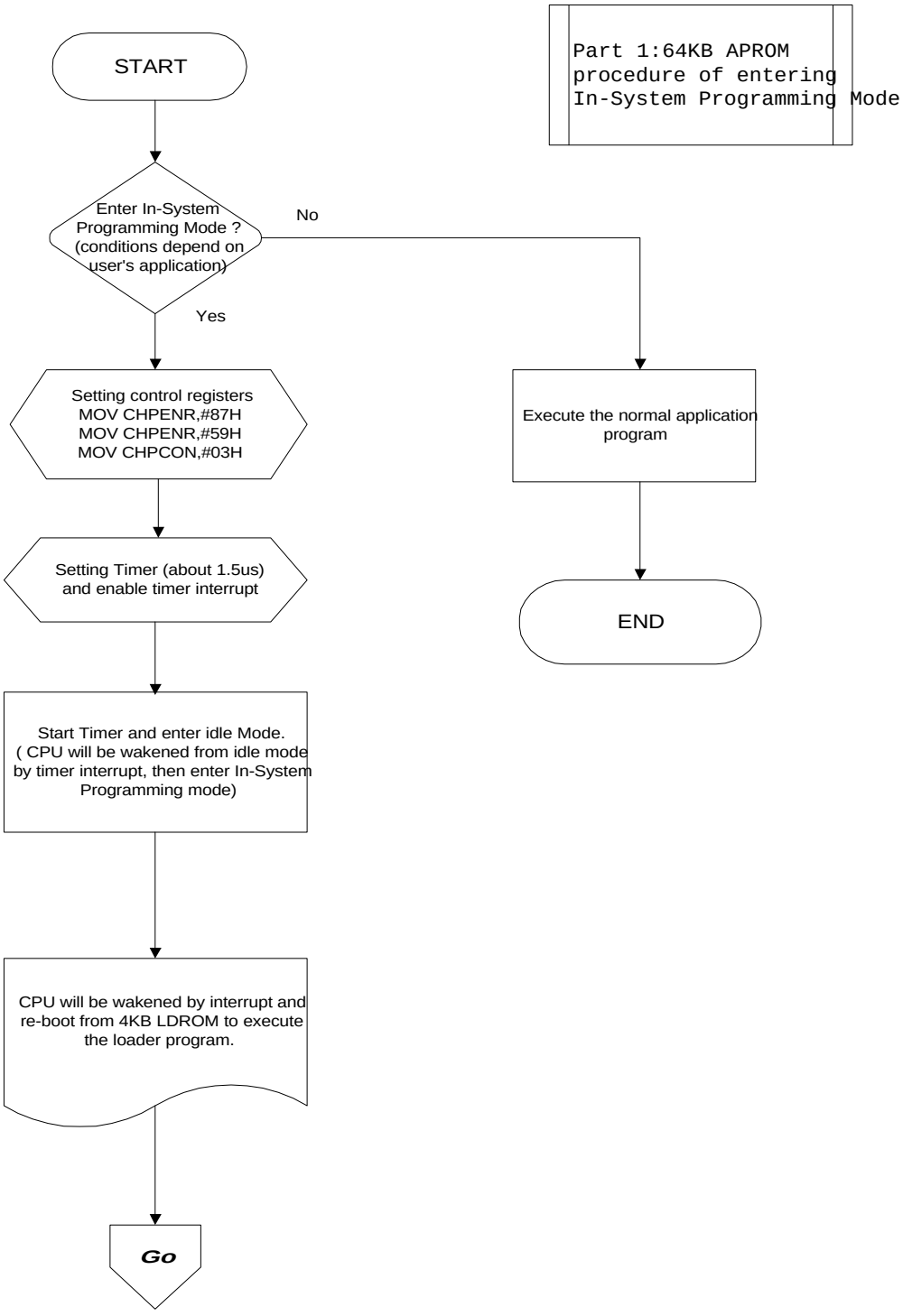
P4.3	P2.7	P2.6	Mode
X	L	L	FO4KBOOT
L	X	X	FO4KBOOT

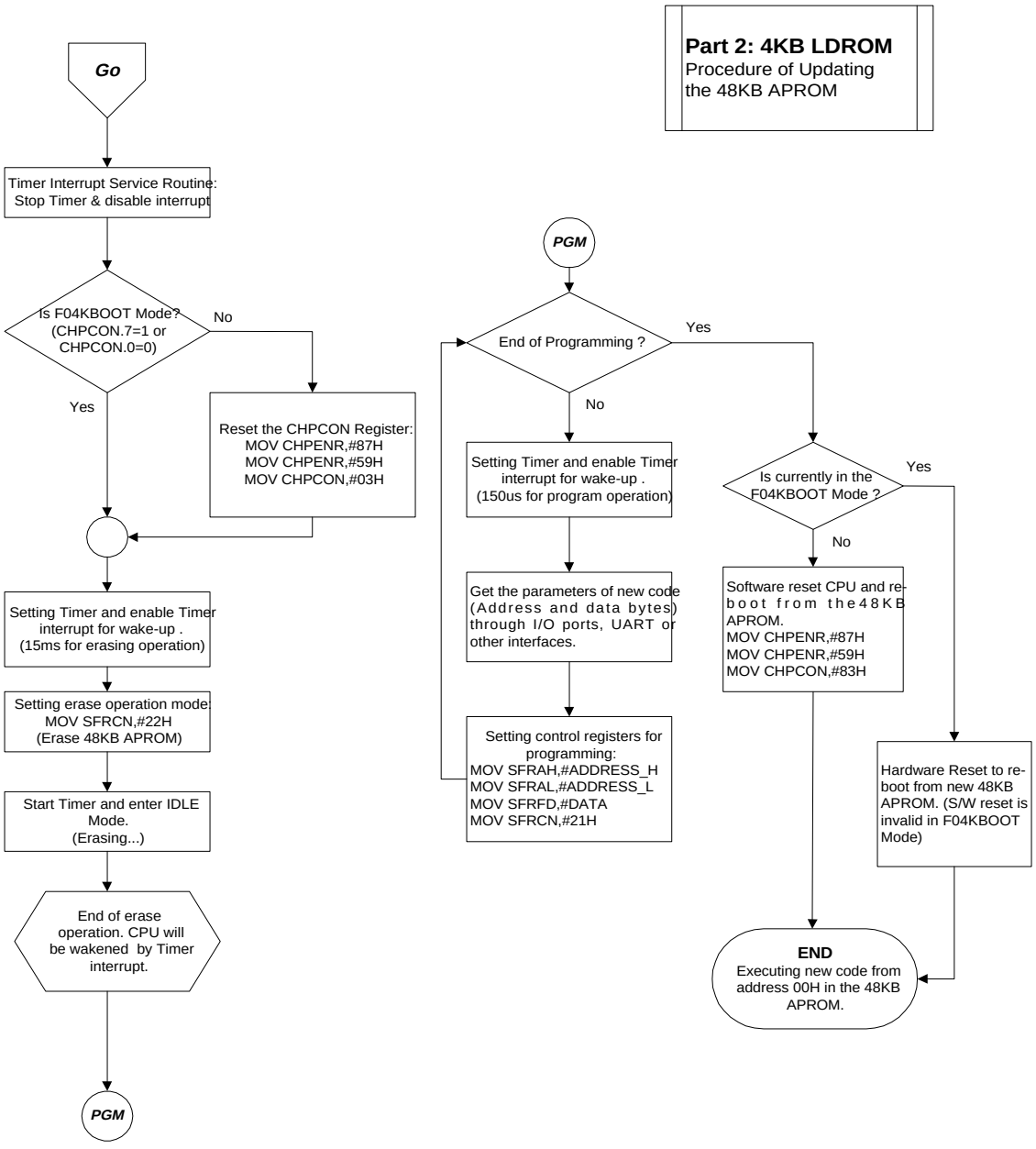


NOTE1: The possible situation that you need to enter F04KBOOT mode is when the APROM program can not run normally and W78E516 can not jump to LDROM to execute on chip programming function. Then you can use this F04KBOOT mode to force the W78E516 jump to LDROM and run the in-system programming procedure. When you design your system, you can connect the pins P2.6,P2.7 to switches or jumpers. When the APROM program is fail to execute the normal application program user can force the W78E516 to enter the F04KBOOT mode and resume the in-system programming procedure for recovering the APROM code.

NOTE2: In application system design, user must take care the P2, P3, ALE, /EA and /PSEN pin value at reset to avoid W78E516 entering the programming mode or F04KBOOT mode in normal operation.

The Algorithm of In-System Programming





Note: Setting the CHPCON from 00H to 03H will clear the program counter (PC).

SECURITY

During the on-chip MTP-ROM programming mode, the MTP-ROM can be programmed and verified repeatedly. Until the code inside the MTP-ROM is confirmed OK, the code can be protected. The protection of MTP-ROM and those operations on it are described below.

The W78E516 has several Special Setting Registers, including the Security Register and Company/Device ID Registers, which can not be accessed in programming mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The contents of the Company ID and Device ID registers have been set in factory. **The Security Register is located at the 0FFFH on the 4KB LDROM.**

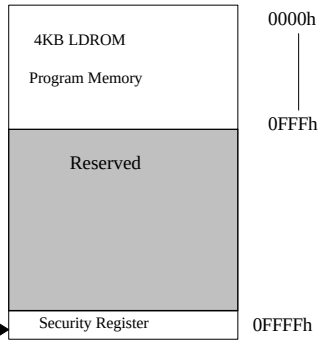
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0	1	1	0	1	0	**Company ID (#DAH)**
1	1	1	0	0	0	0	0	**Device ID (#62H)**
Reserved					B2	B1	B0	**Security Bits**

B0 : Lock bit, logic 0 : active

B1 : MOVC inhibit,
logic 0 : the MOVC instruction in external memory cannot access the code in internal memory.
logic 1 : no restriction.

B1 : Encryption
logic 0 : the encryption logic enable
logic 1 : the encryption logic disable

Default 1 for each bit.



Special Setting Registers

Lock bits

These bits are used to protect the customer's program code in the W78E516. It may be set after the programmer finishes the programming and verifies sequence. Once these bits are set to logic 0, both the MTP-ROM data and Special Setting Registers can not be accessed again.

MOVC Inhibit

These bits are used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When these bits are set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If these bits are logic 1, there are no restrictions on the MOVC instruction.

Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	PARAMETER	MIN.	MAX.	UNIT
1	VDD–VSS	DC Power Supply	-0.3	+6.0	V
2	VIN	Input Voltage	VSS -0.3	VDD +0.3	V
3	TA	Operating Temperature	0	70	°C
4	TST	Storage Temperature	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

D.C. ELECTRICAL CHARACTERISTICS

(V_{DD}-V_{SS}= 5V±10%, T_A= 25°C, Fosc = 20MHz, unless otherwise specified.)

Symbol	Parameter	Specification			Test Conditions
		Min	Max	Unit	
V_{DD}	Operating Voltage	4.5	5.5	V	RST=1, P0 = V_{DD}
I_{DD}	Operating Current	-	20	mA	No load V_{DD}=5.5V
I_{IDLE}	Idle Current	-	6	mA	Idle mode V_{DD}=5.5V
I_{PWDN}	Power Down Current	-	50	µA	Power-down mode V_{DD}=5.5V
I_{IN1}	Input Current P1, P2, P3, P4	-50	+10	µA	V_{DD}=5.5V V_{IN}=0V or V_{DD}
I_{IN2}	Input Current RST	-10	+300	µA	V_{DD}=5.5V 0<V_{IN}<V_{DD}
I_{LK}	Input Leakage Current P0, /EA	-10	+10	µA	V_{DD}=5.5V 0V<V_{IN}<V_{DD}
I_{TL}[*4]	Logic 1 to 0 Transition Current P1, P2, P3, P4	-500	-	µA	V_{DD}=5.5V V_{IN}=2.0V
V_{IL1}	Input Low Voltage P0, P1, P2, P3, P4, /EA	0	0.8	V	V_{DD}=4.5V
V_{IL2}	Input Low Voltage RST	0	0.8	V	V_{DD}=4.5V
V_{IL3}	Input Low Voltage XTAL1[*4]	0	0.8	V	V_{DD}=4.5V
V_{IH1}	Input High Voltage P0, P1, P2, P3, P4, /EA	2.4	V_{DD}+0.2	V	V_{DD}=5.5V
V_{IH2}	Input High Voltage RST	3.5	V_{DD}+0.2	V	V_{DD}=5.5V
V_{IH3}	Input High Voltage XTAL1[*4]	3.5	V_{DD}+0.2	V	V_{DD}=5.5V
V_{OL1}	Output Low Voltage P1, P2, P3, P4	-	0.45	V	V_{DD}=4.5V I_{OL}= +2mA

V_{OL2}	Output Low Voltage P0, ALE, /PSEN[*3]	-	0.45	V	V_{DD}=4.5V I_{OL}= +4mA
Isk1	Sink current P1, P3, P4	4	12	mA	V_{DD}=4.5V Vin = 0.45V
Isk2	Sink current P0, P2, ALE, /PSEN	10	20	mA	V_{DD}=4.5V Vin = 0.45V
V_{OH1}	Output High Voltage P1, P2, P3, P4	2.4	-	V	V_{DD}=4.5V I_{OH}= -100µA
V_{OH2}	Output High Voltage P0, ALE, /PSEN[*3]	2.4	-	V	V_{DD}=4.5V I_{OH}= -400µA
Isr1	Source current P1, P2, P3, P4	-120	-250	uA	V_{DD}=4.5V Vin = 2.4V (latch)
Isr2	Source current P0, P2, ALE, /PSEN	-8	-20	mA	V_{DD}=4.5V Vin = 2.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*3. P0, ALE and /PSEN are tested in the external access mode.

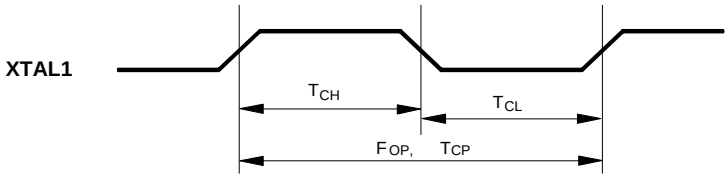
*4. XTAL1 is a CMOS input.

*5. Pins of P1, P2, P3 , P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} approximates to 2V.

AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ¡ 20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	TCH	10	-	-	nS	3
Clock Low	TCL	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

Notes:
1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{\text{RD}}$ Low	TDAR	3 TCP-Δ	-	3 TCP+Δ	nS	1, 2
$\overline{\text{RD}}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{\text{RD}}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{\text{RD}}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{\text{RD}}$ Pulse Width	TDRD	6 TCP-Δ	6 TCP	-	nS	2

Notes:
1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{\text{WR}}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{\text{WR}}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{\text{WR}}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{\text{WR}}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

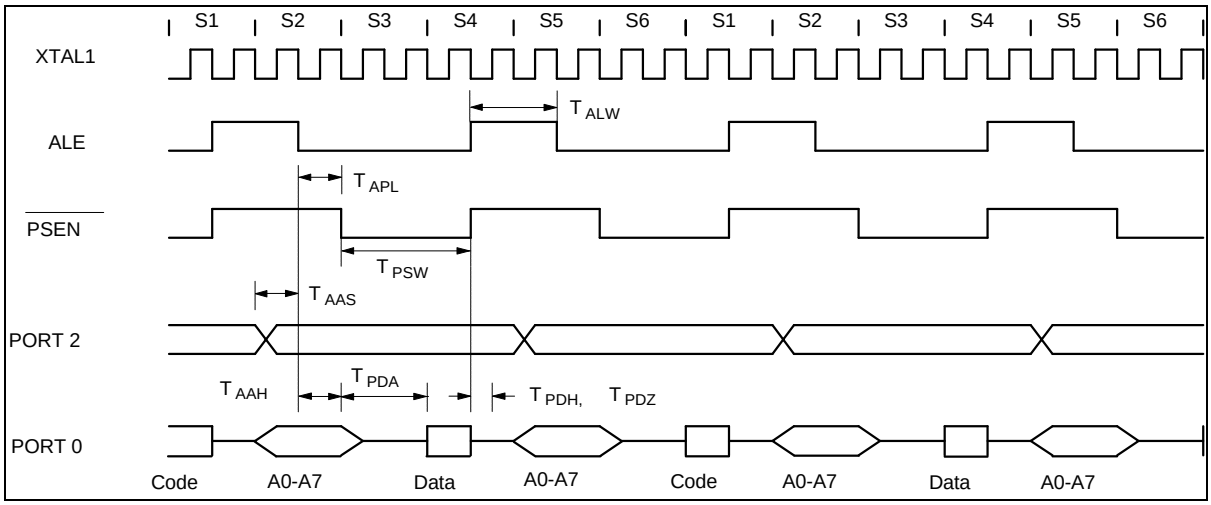
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

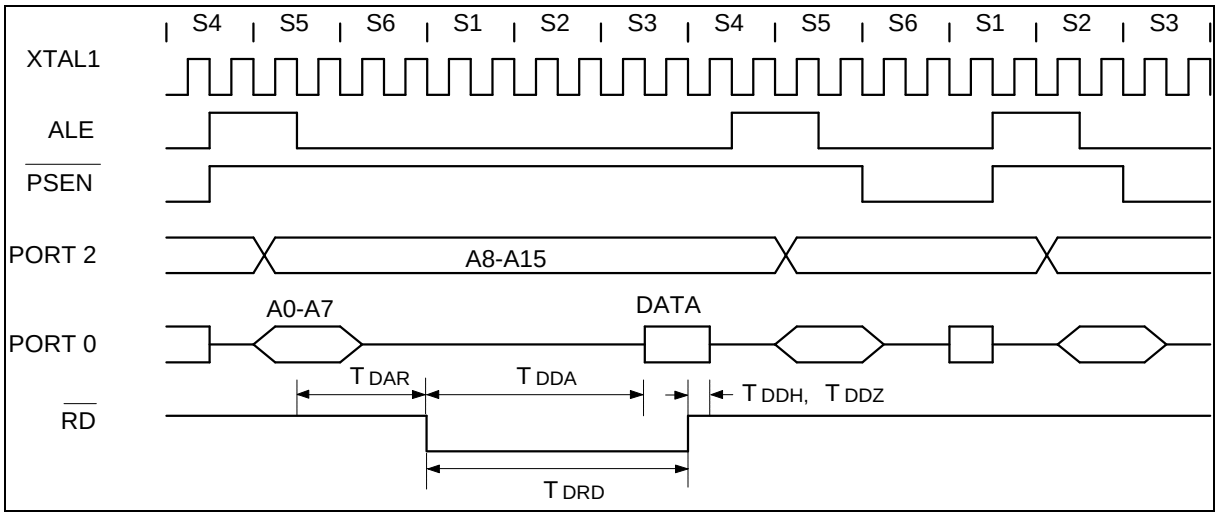
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

TIMING WAVEFORMS

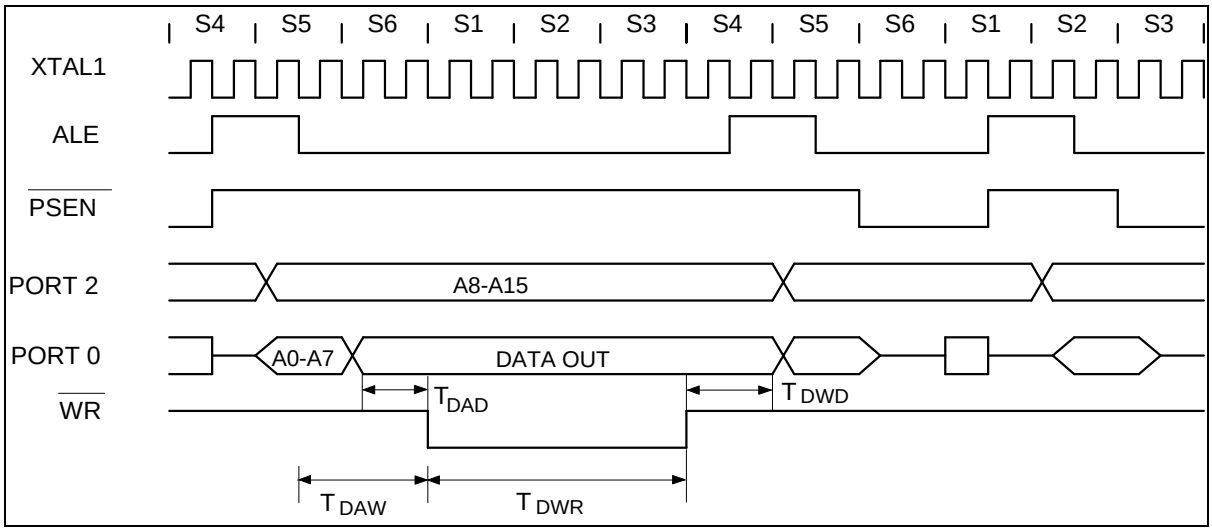
Program Fetch Cycle



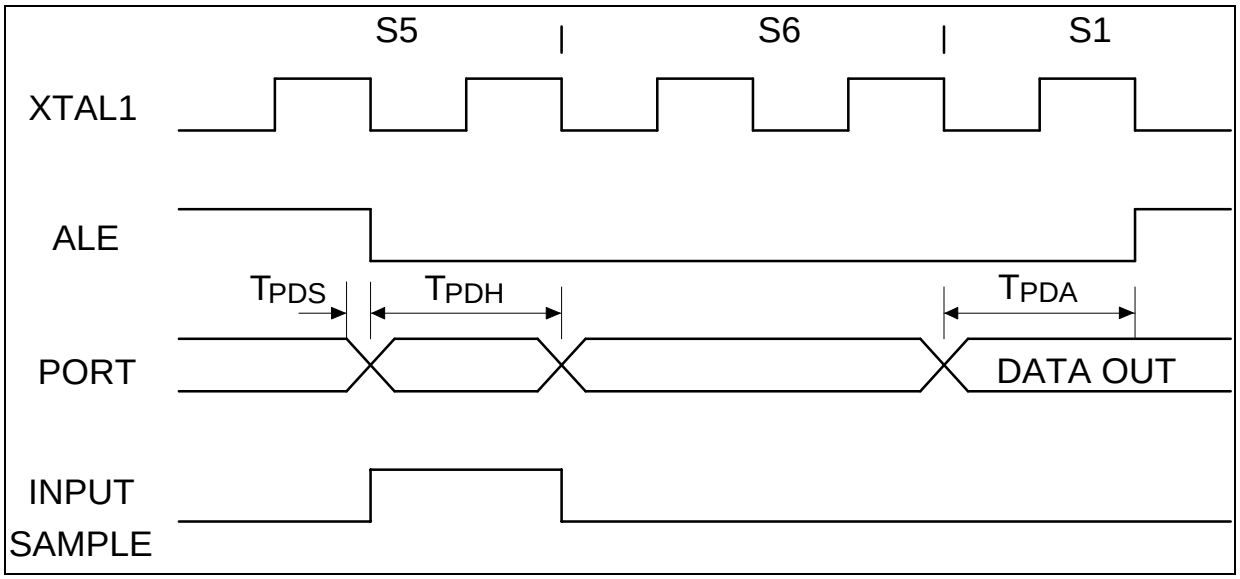
Data Read Cycle



Data Write Cycle



Port Access Cycle



TYPICAL APPLICATION CIRCUIT

Expanded External Program Memory and Crystal

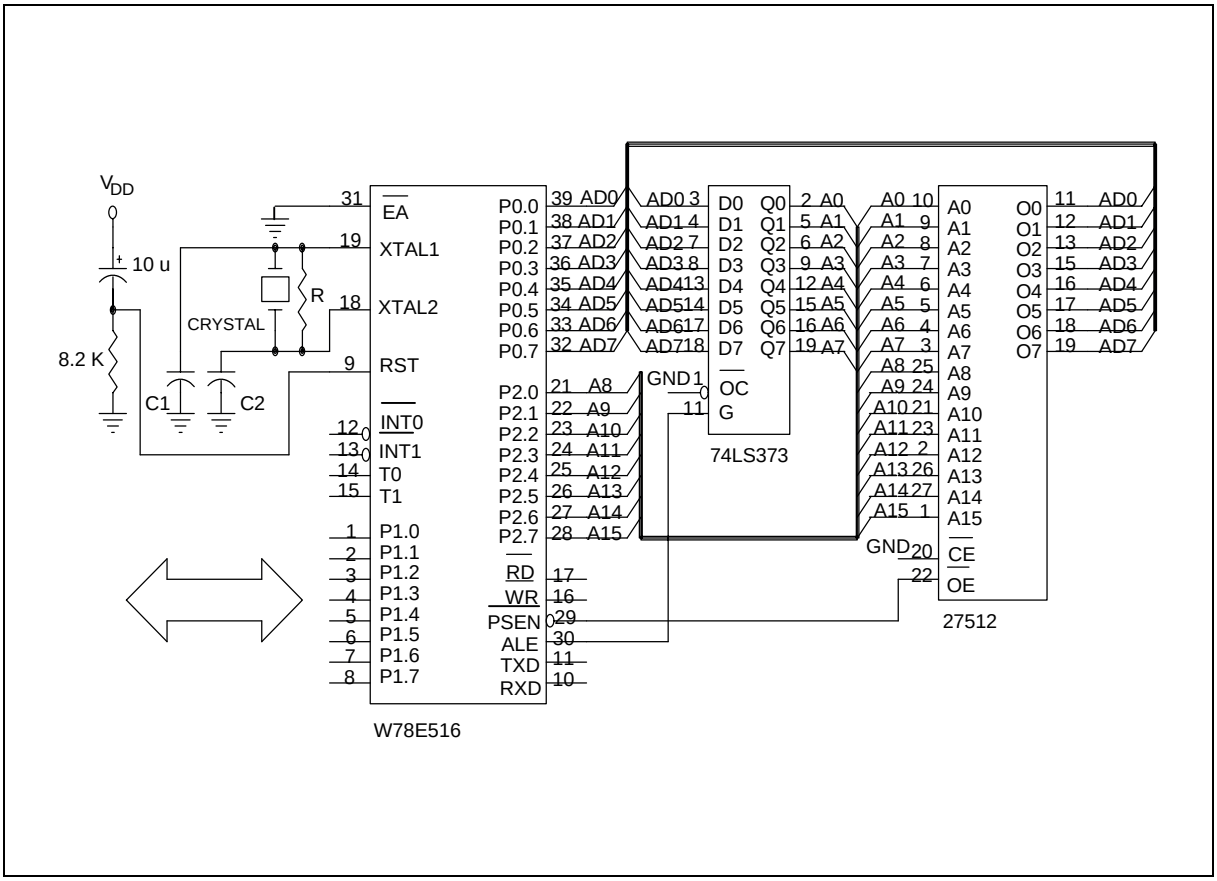


Figure A

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
24 MHz	15P	10P	-
32 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications.

Note1: C1, C2, R components refer to Figure A

Note2: Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

Expanded External Data Memory and Oscillator

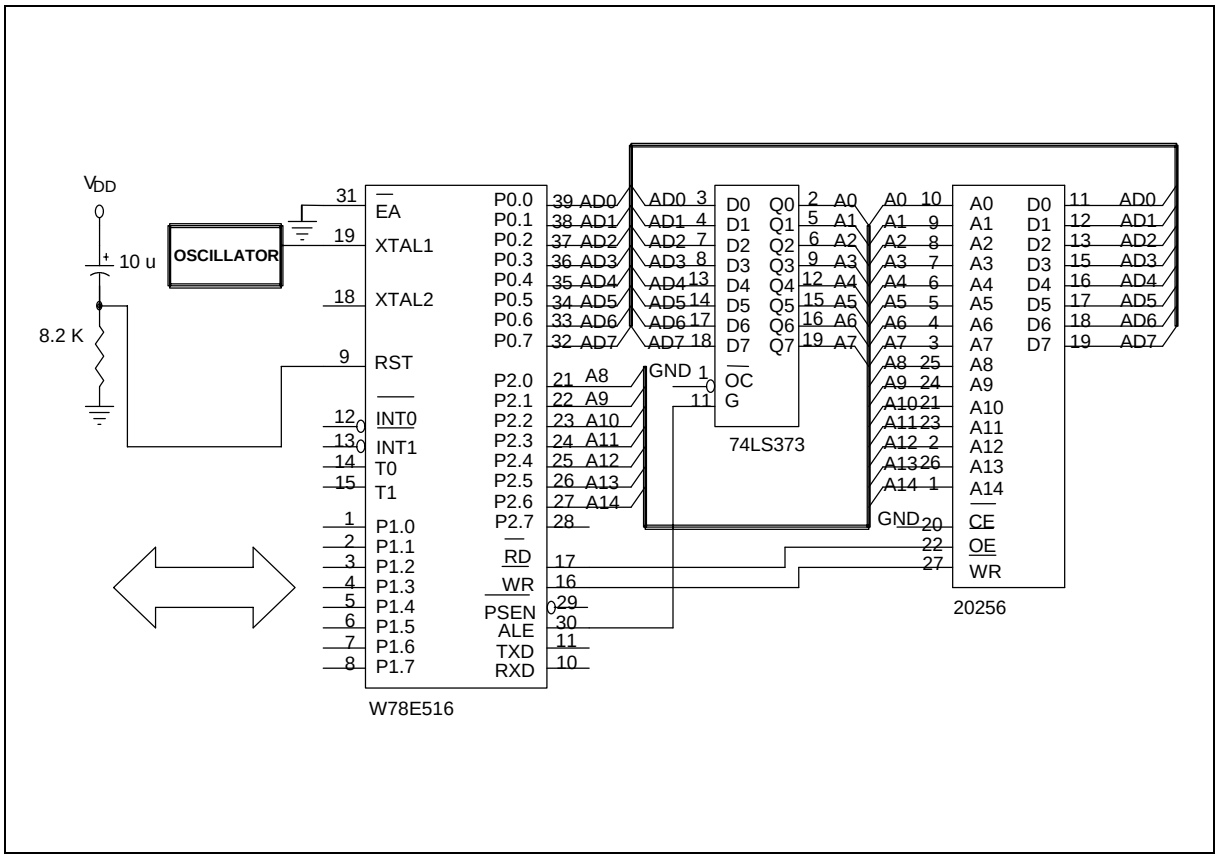
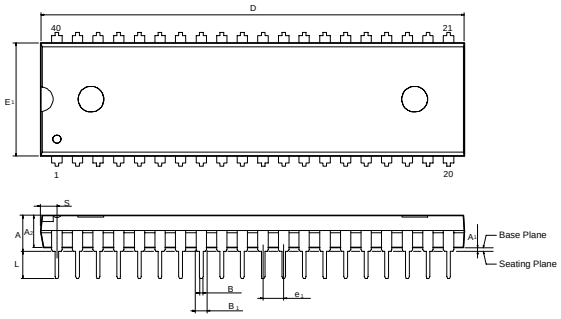

VDD
10 u
OSCILLATOR
8.2 K
EA
XTAL1
XTAL2
RST
INT0
INT1
T0
T1
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
P2.0
P2.1
P2.2
P2.3
P2.4
P2.5
P2.6
P2.7
RD
WR
PSEN
ALE
TXD
RXD
W78E516
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
A8
A9
A10
A11
A12
A13
A14
GND
OC
G
74LS373
A0
A1
A2
A3
A4
A5
A6
A7
D0
D1
D2
D3
D4
D5
D6
D7
CE
OE
WR
20256

Figure B

PACKAGE DIMENSIONS

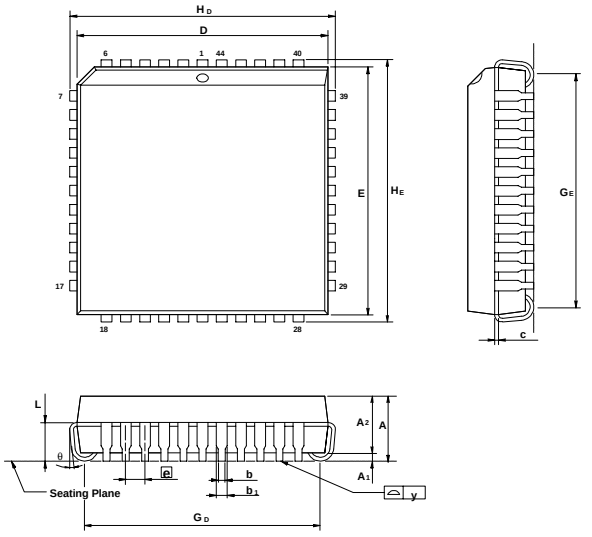
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

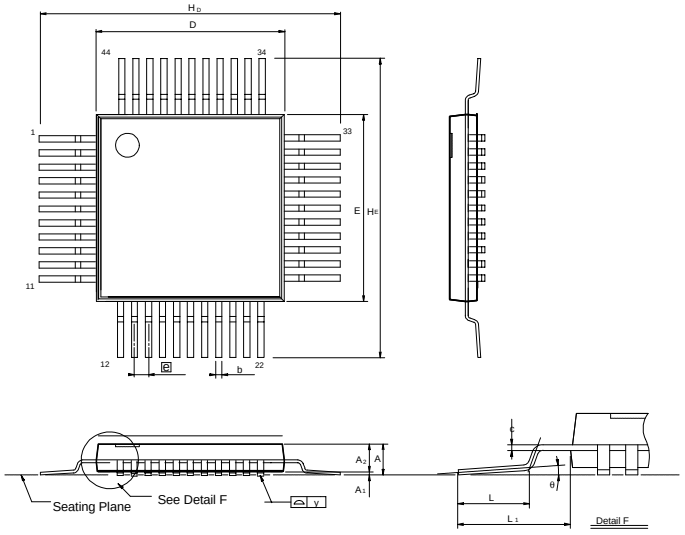
44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. **Dimension D & E do not include interlead flash.**
2. **Dimension b1 does not include dambar protrusion/intrusion.**
3. **Controlling dimension: Inches**
4. **General appearance spec. should be based on final visual inspection spec.**

44-pin PQFP

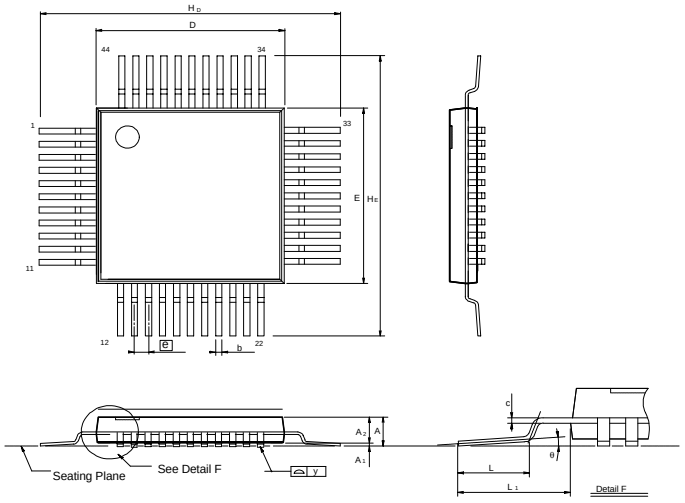


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

44-pin TQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	0.047	---	---	1.20
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.0039	0.013	0.015	0.22	0.32	0.38
c	0.004	---	0.008	0.090	---	0.200
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.468	0.472	0.476	11.90	12.00	12.10
H_E	0.468	0.472	0.476	11.90	12.00	12.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	---	0.039	---	---	1.00	---
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

Application Note: In-system Programming Software Examples

This application note illustrates the in-system programmability of the Winbond W78E516 MTP-ROM microcontroller. In this example, microcontroller will boot from 64KB APROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64KB APROM. While entering in-system programming mode, microcontroller excutes the loader program in 4KB LDROM bank. The loader program erases the 64KB APROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 64KB APROM.

EXAMPLE 1:

```
;*****************************************************************************************************************
;* Example of 64K APROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating thecontents of APROM code else excutes the current ROM code.
;* XTAL = 40 MHz
;*****************************************************************************************************************

    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON     EQU     BFH
    CHPENR     EQU     F6H
    SFRAL      EQU     C4H
    SFRAH      EQU     C5H
    SFRFD      EQU     C6H
    SFRCN      EQU     C7H

        ORG    0H
        LJMP   100H          ;JUMP TO MAIN PROGRAM
  ;*************************************************************************
  ;*  TIMER0 SERVICE VECTOR ORG=000BH
  ;*************************************************************************
        ORG    00BH
        CLR  TR0         ;TR0=0,STOP TIMER0
        MOV  TL0,R6
        MOV  TH0,R7
        RETI
  ;*************************************************************************
  ;*  64K APROM MAIN PROGRAM
  ;*************************************************************************
        ORG  100H

MAIN_64K:

       MOV A,P1                 ;SCAN P1.0
       ANL A,#01H
       CJNE A,#01H,PROGRAM_64K  ;IF P1.0=0, ENTER IN-SYSTEM PROGRAMMING MODE
       JMP NORMAL_MODE

PROGRAM_64K:
        MOV CHPENR,#87H   ;CHPENR=87H, CHPCON REGISTER WRTE ENABLE
        MOV CHPENR,#59H   ;CHPENR=59H, CHPCON REGISTER WRITE ENABLE
        MOV CHPCON,#03H     ;CHPCON=03H, ENTER IN-SYSTEM PROGRAMMING MODE
        MOV TCON,#00H       ;TR=0 TIMER0 STOP
        MOV IP,#00H         ;IP=00H
```

```
        MOV IE,#82H             ;TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV R6,#FEH             ;TL0=FEH
        MOV R7,#FFH           ;TH0=FFH
        MOV TL0,R6
        MOV TH0,R7
        MOV TMOD,#01H       ;TMOD=01H,SET TIMER0 A 16-BIT TIMER
        MOV TCON,#10H         ;TCON=10H,TR0=1,GO
        MOV PCON,#01H         ;ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                              ;PROGRAMMABILITY
;*****************************************************************************
;* Normal mode 64KB APROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
            .                           ;User's application program
            .
            .
            .
            .
```

EXAMPLE 2:

```
;*****************************************************************************************************************************************  ;*
Example of 4KB LDROM program: This lorder program will erase the 64KB APROM first, then reads the new ;*
code from external SRAM and program them into 64KB APROM bank. XTAL = 40 MHz
;*****************************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON     EQU     BFH
    CHPENR     EQU     F6H
    SFRAL      EQU     C4H
    SFRAH      EQU     C5H
    SFRFD      EQU     C6H
    SFRCN      EQU     C7H

        ORG     000H
        LJMP    100H    ;JUMP TO MAIN PROGRAM
  ;*************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG=0BH
  ;*************************************************************************
        ORG 000BH
        CLR   TR0       ;TR0=0,STOP TIMER0
        MOV TL0,R6
        MOV TH0,R7
        RETI

  ;*************************************************************************
  ;*  4KB LDROM MAIN PROGRAM
```

```
;*****************************************************************************
        ORG 100H

MAIN_4K:

        MOV CHPENR,#87H   ;CHPENR=87H, CHPCON WRITE ENABLE.
        MOV CHPENR,#59H   ;CHPENR=59H, CHPCON WRITE ENABLE.
        MOV 7FH,#01H       ;SET F04KBOOT MODE FLAG.

        MOV A,CHPCON
        ANL A,#01H
        CJNE A,#00H,UPDATE_64K    ;CHECK CHPCON BIT 0
        MOV 7FH,#00H       ; FLAG=0, NOT IN THE F04KBOOT MODE.

        MOV CHPCON,#01H   ;CHPCON=01H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR,#00H   ;DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON,#00H     ;TCON=00H ,TR=0 TIMER0 STOP
        MOV TMOD,#01H      ;TMOD=01H ,SET TIMER0 A 16BIT TIMER
        MOV IP,#00H        ;IP=00H
        MOV IE,#82H        ;IE=82H,TIMER0 INTERRUPT ENABLED
        MOV R6,#FEH
        MOV R7,#FFH
        MOV TL0,R6
        MOV TH0,R7
        MOV TCON,#10H      ;TCON=10H,TR0=1,GO
        MOV PCON,#01H      ;ENTER IDLE MODE


 UPDATE_64K:

        MOV CHPENR,#00H    ;DISABLE CHPCON WRITE-ATTRIBUTE
        MOV TCON,#00H      ;TCON=00H ,TR=0 TIM0 STOP
        MOV IP,#00H        ;IP=00H
        MOV IE,#82H        ;IE=82H,TIMER0 INTERRUPT ENABLED
        MOV TMOD,#01H      ;TMOD=01H ,MODE1
        MOV R6,#3CH          ;SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15ms.   DEPENDING
                             ;ON USER'S SYSTEM CLOCK RATE.
        MOV R7,#B0H
        MOV TL0,R6
        MOV TH0,R7

ERASE_P_4K:
        MOV SFRCN,#22H    ;SFRCN(C7H)=22H  ERASE 64K
        MOV TCON,#10H    ;TCON=10H,TR0=1,GO
        MOV PCON,#01H    ;ENTER IDLE MODE( FOR ERASE OPERATION)

;*****************************************************************************
;* BLANK CHECK
;*****************************************************************************

        MOV SFRCN,#0H      ;READ 64KB APROM MODE
        MOV SFRAH,#0H      ;START ADDRESS = 0H
        MOV SFRAL,#0H
         MOV R6,#FBH       ;SET TIMER FOR READ OPERATION, ABOUT 1.5us.
        MOV R7,#FFH
        MOV TL0,R6
```

```
        MOV TH0,R7

BLANK_CHECK_LOOP:

        SETB TR0                ;ENABLE TIMER 0
        MOV PCON,#01H           ;ENTER IDLE MODE
        MOV A,SFRFD             ;READ ONE BYTE

        CJNE A,#FFH,BLANK_CHECK_ERROR
        INC SFRAL               ;NEXT ADDRESS
        MOV A,SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A,SFRAH
        CJNE A,#0H,BLANK_CHECK_LOOP   ;END ADDRESS=FFFFH
        JMP PROGRAM_64KROM

BLANK_CHECK_ERROR:

        MOV P1,#F0H
        MOV P3,#F0H
        JMP $

;*****************************************************************************
;* RE-PROGRAMMING 64KB APROM BANK
;*****************************************************************************
PROGRAM_64KROM:

        MOV DPTR,#0H          ;THE ADDRESS OF NEW ROM CODE
        MOV R2,#00H          ;TARGET LOW BYTE ADDRESS
        MOV R1,#00H          ;TARGET HIGH BYTE ADDRESS
        MOV DPTR,#0H           ;EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH,R1      ;SFRAH, TARGET  HIGH ADDRESS
        MOV SFRCN,#21H     ;SFRCN(C7H)=21  (PROGRAM 64K)
        MOV R6,#0CH           ;SET TIMER FOR PROGRAMMING, ABOUT 150us.
        MOV R7,#FEH
        MOV TL0,R6
        MOV TH0,R7
PROG_D_64K:
        MOV SFRAL,R2          ;SFRAL(C4H)= LOW BYTE ADDRESS
        MOVX A,@DPTR          ;READ DATA FROM EXTERNAL SRAM BUFFER
        MOV SFRFD,A         ;SFRFD(C6H)=DATA IN
        MOV TCON,#10H         ;TCON=10H,TR0=1,GO
        MOV PCON,#01H         ;ENTER IDLE MODE( PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2,#0H,PROG_D_64K
        INC  R1
        MOV SFRAH,R1
        CJNE R1,#0H,PROG_D_64K
;*****************************************************************************
; * VERIFY 64KB APROM BANK
;*****************************************************************************
        MOV R4,#03H         ;ERROR COUNTER
        MOV R6,#FBH         ;SET TIMER FOR READ VERIFY, ABOUT 1.5us.
        MOV R7,#FFH
```

```
        MOV TL0,R6
        MOV TH0,R7
        MOV DPTR,#0H          ;The start address of sample code
        MOV R2,#0H            ;Target  low byte address
        MOV R1,#0H          ;Target  high byte address
        MOV SFRAH,R1          ;SFRAH, Target high address
        MOV SFRCN,#00H      ;SFRCN=00 (Read ROM CODE)
READ_VERIFY_64K:
        MOV SFRAL,R2          ;SFRAL(C4H)= LOW ADDRESS
        MOV TCON,#10H     ;TCON=10H,TR0=1,GO
        MOV PCON,#01H
        INC R2
        MOVX A,@DPTR
        INC DPTR
        CJNE A,SFRFD,ERROR_64K
        CJNE R2,#0H,READ_VERIFY_64K
        INC R1
        MOV SFRAH,R1
        CJNE R1,#0H,READ_VERIFY_64K

;*****************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*****************************************************************************
        MOV CHPENR,#87H     ;CHPENR=87H
        MOV CHPENR,#59H     ;CHPENR=59H
        MOV CHPCON,#83H     ;CHPCON=83H, SOFTWARE RESET.


ERROR_64K:
        DJNZ R4,UPDATE_64K     ;IF ERROR OCCURS, REPEAT 3 TIMES.
        .                      ;IN-SYSTEM PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
        .
        .
        .
```

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