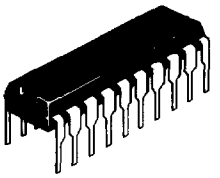
M5M21C68P-45, -55

16384-BIT (4096-WORD BY 4-BIT) CMOS STATIC RAM



DESCRIPTION

This is a family of 4096 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

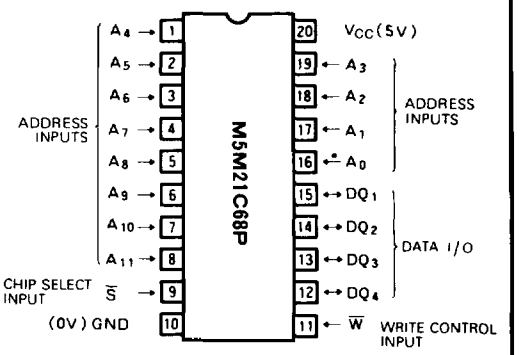
FEATURES

- Fast access time M5M21C68P-45 ..... 45 ns (max)
  M5M21C68P-55 ..... 55 ns (max)
- Low power dissipation Active .....200 mW (typ)
  Stand by .....5 μW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
  Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



Outline 20 P4

FUNCTION

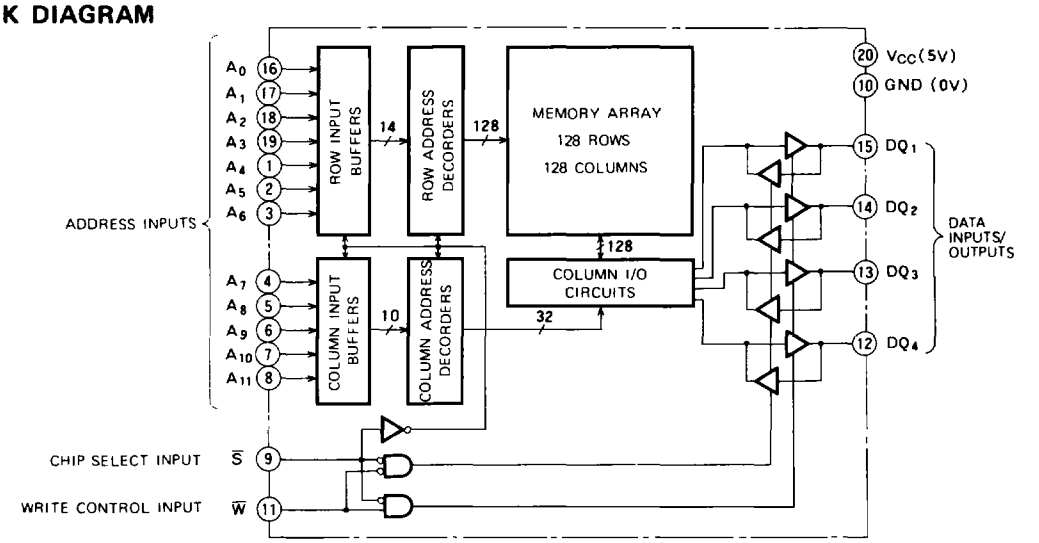
A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data ia available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
Pd	Maximum power dissipation		1	W
Topr	Operating temperature		−10~85	°C
Tstg	Storage temperature		−65~150	°C

* Pulse width = 20 ns, DC: -0.5V

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−3 *		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA				0.4	V
I_I	Input current	V_I = 0~5.5V				10	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\overline{S})}$ = 2.2V, V_O = 0~V_{CC}				50	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\overline{S})}$ = 0.8V, Output open	DC		25	50	mA
			AC			80	
I_{CC2}	Stand by current	$V_{I(\overline{S})}$ = 2.2V Other V_I ≦ 0.2V			10	20	mA
I_{CC3}	Stand by current	$V_{I(\overline{S})}$ ≧ V_{CC} − 0.2V, Other V_I ≦ 0.2V or V_I ≧ V_{CC} − 0.2V			0.001	2	mA
C_i	Input capacitance	V_I = GND, V_i = 25mVrms, f = 1MHz					pF
Co	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1MHz					pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, DC: -0.5V

SWITCHING CHARACTERISTICS (FOR READ CYCLE) (T_a = 0~70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M21C68P-45			M5M21C68P-55			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	45			55			ns
$t_{a(A)}$	Address access time			45			55	ns
$t_{a(S)}$	Chip select access time			45			55	ns
$t_{v(A)}$	Data valid time after address	5			5			ns
$t_{en(S)}$	Output enable time after chip selection	20			20			ns
$t_{dis(S)}$	Output disable time after chip deselection	0		20	0		20	ns
t_{PU}	Power-up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			45			55	ns

16384-BIT (4096-WORD BY 4-BIT) CMOS STATIC RAM

TIMING REQUIREMENTS (FOR WRITE CYCLE) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	M5M21C68P-45			M5M21C68P-55			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	45			55			ns
$t_{su(S)}$	Chip select setup time	35			40			ns
$t_{su(A)_1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0			0			ns
$t_{su(A)_2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0			0			ns
$t_{w(W)}$	Write pulse width	35			40			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{su(D)}$	Data setup time	20			20			ns
$t_{h(D)}$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0		15	0		20	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	35			40			ns

CONDITIONS

Input pulse levels . . . . . 0 to 3V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level . . . . . 0.8V ~ 2V
Output load . . . . . Fig. 1, Fig. 2

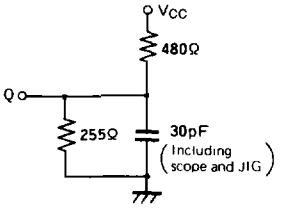


Fig. 1 Output load

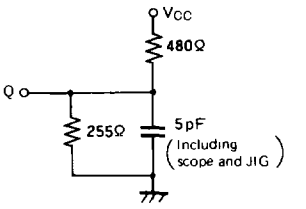
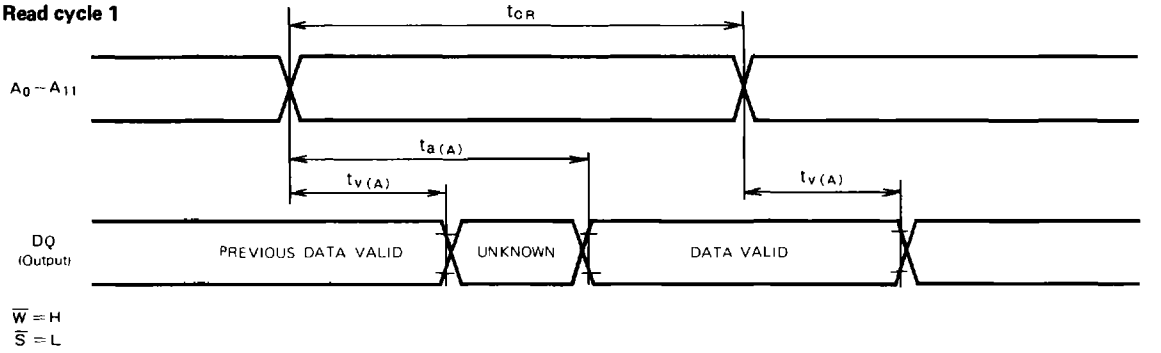


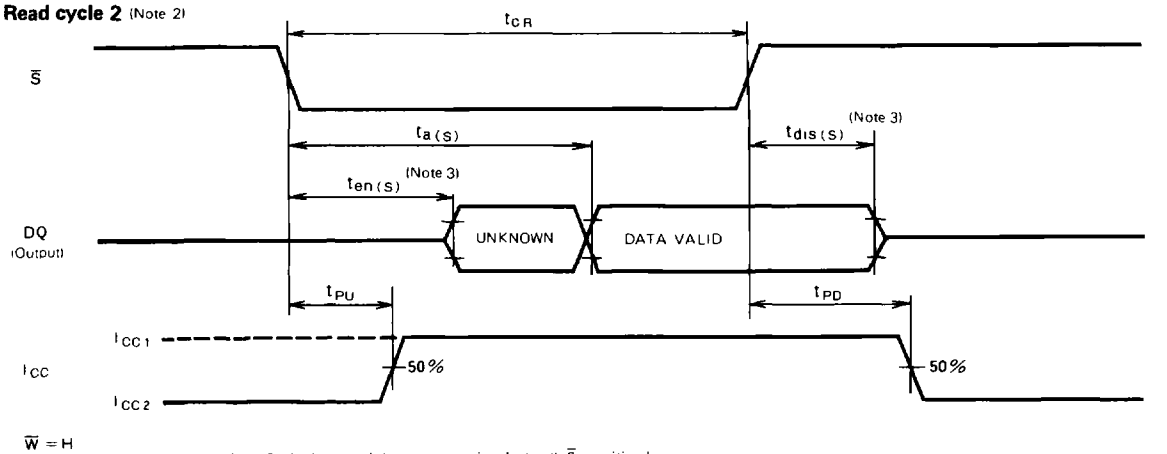
Fig. 2 Output load for t_{en}, t_{dis}

TIMING DIAGRAMS

Read cycle 1



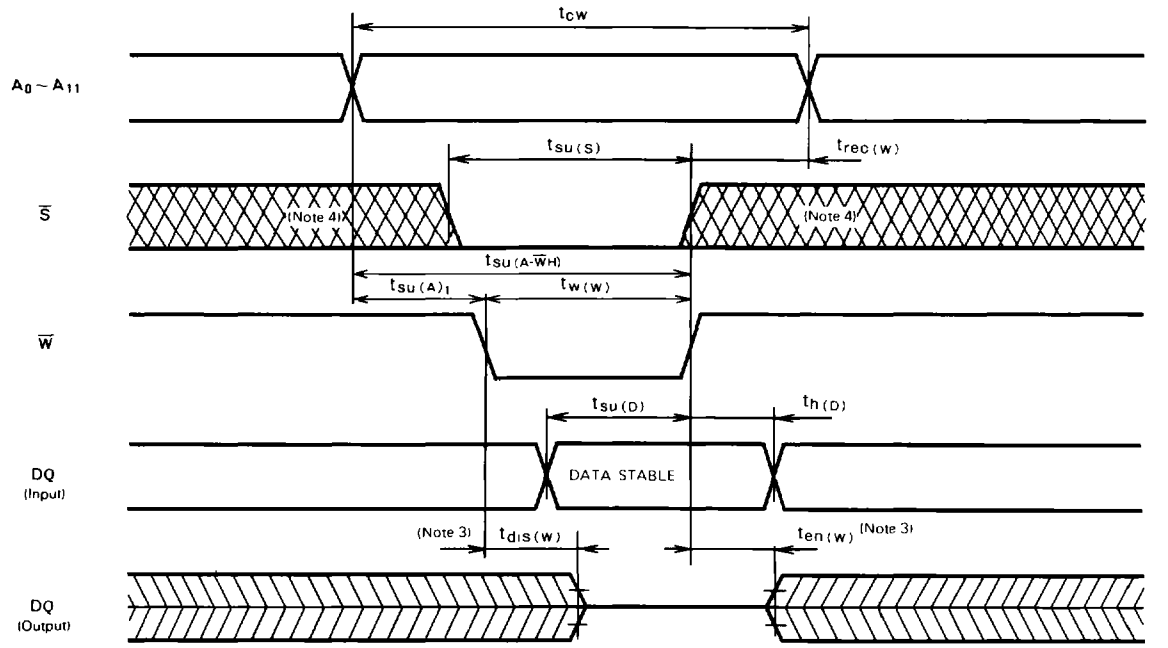
Read cycle 2 (Note 2)



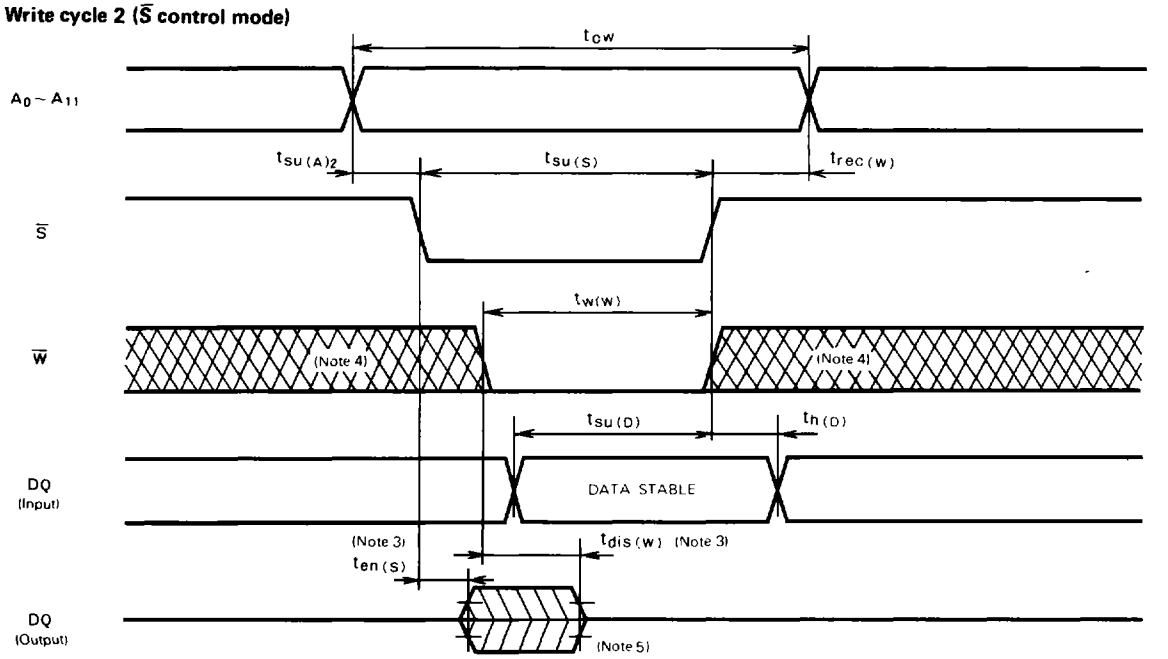
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

TIMING DIAGRAMS

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 4. Hatching indicates the state is don't care.

5 When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.