IS28LV020

262,144 x 8 CMOS FLASH MEMORY

FEATURES

- High performance
  - Power supply voltage 3V ± 10%
  - 90 ns, 120 ns maximum access time
- CMOS low power consumption
  - 30 mA maximum active current
  - 100 µA maximum standby current
- Compatible with JEDEC-standard byte-wide pinouts
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
- Program and erase voltage 12.0V ± 5%
- Maximum latch-up immunity through advanced CMOS process

- Flash electrical bulk chip-erase
  - One second typical chip-erase
- Fast-pulse programming algorithm
  - 10 µs (typical) byte-program
  - 4 second chip-program
- Command register architecture for microprocessor/microcontroller compatible write interface
- On-chip address and data latches for programming
- Advanced CMOS flash memory technology
  - Low cost single transistor memory cell
- Integrated program/erase stop timer

BLOCK DIAGRAM
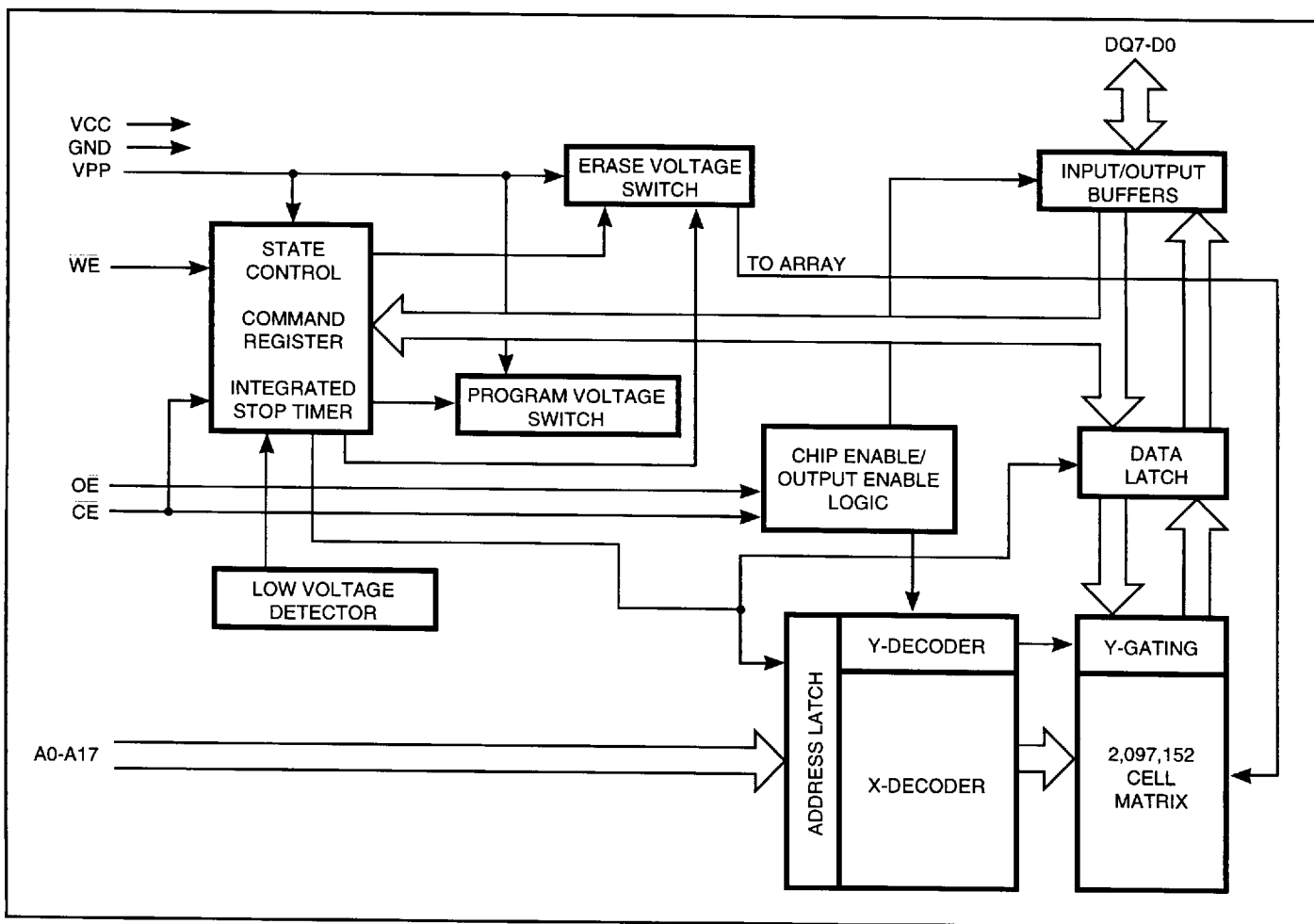
9004404 0000772 779

IS28LV020

DESCRIPTION

The *ISSI* IS28LV020 is a high-speed, low-power, 262,144 bytes of eight bits CMOS flash memory. It offers the most cost-effective and reliable alternative for read/write nonvolatile RAM.
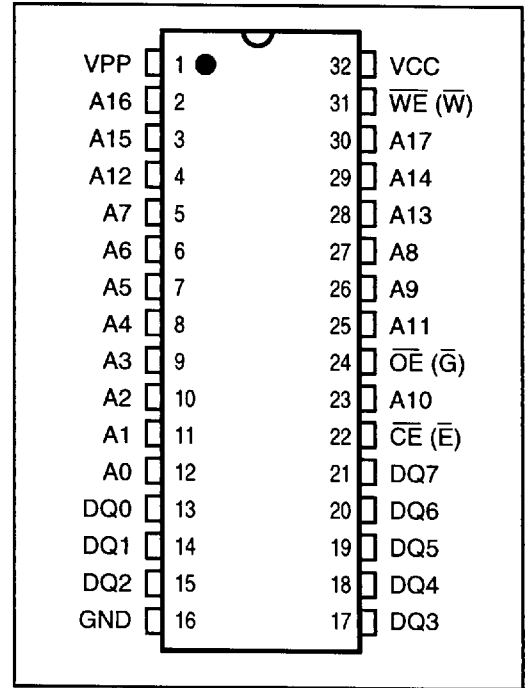
The IS28LV020 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten in a test socket; PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. Finally, the highest degree of latch-up protection is achieved with special layout. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from −1V to Vcc + 1V.

The IS28LV020 is available in 32-pin DIP, 32-lead PLCC and 32-pin TSOP packages. Pin assignments conform to JEDEC standards for byte-wide EPROMS.
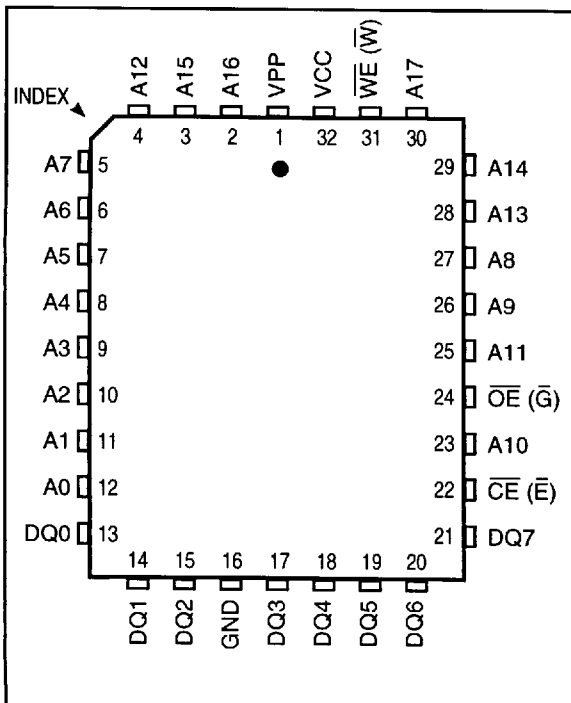
PIN DESCRIPTIONS

A0-A17	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{CE}$ ($\overline{E}$)	Chip Enable Input
$\overline{OE}$ ($\overline{G}$)	Output Enable Input
$\overline{WE}$ ($\overline{W}$)	Write Enable Input
Vcc	Power Supply Voltage
VPP	Program Supply Voltage
GND	Ground
NC	No Internal Connection

PIN CONFIGURATIONS
32-Pin DIP

VPP	1	32	VCC
A16	2	31	$\overline{WE}$ ($\overline{W}$)
A15	3	30	A17
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$ ($\overline{G}$)
A2	10	23	A10
A1	11	22	$\overline{CE}$ ($\overline{E}$)
A0	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
GND	16	17	DQ3

32-Pin PLCC

32-Pin TSOP

9004404 0000773 605

PRINCIPLES OF OPERATION

ISSI's IS28LV020 flash memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The IS28LV020 uses a command register to manage this functionality. The command register allows for 100% TTL-level control inputs and fixed power supply levels during erasure and programming, while maintaining maximum EPROM compatibility.

With the Vpp pin at a low voltage level, the IS28LV020 is a read-only memory. With the Vpp pin at a high voltage level, the same EPROM read, standby, and output disable operations are available along with enabling erasure and programming operations. All functions associated with altering memory contents—ISSI identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Command codes are written to the command register using standard microprocessor write timings. Contents of the command register serve as instruction codes input to an internal state-machine which controls the erase and programming circuitry. With the appropriate command codes written to the register, standard microprocessor read timings may output array data, access the ISSI identifier codes, or output data for erase and program verification. Table 2 defines these IS28LV020 command codes.

Integrated Stop Timer
The program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

Write Protection
The IS28LV020 uses a two-step program/erase write sequence to the command register which provides additional software write protections. The command register is active when $V_{PP} = V_{PPH}$. When $V_{PP} = V_{PPL}$, the contents of the command register default to 00H, making the IS28LV020 a read-only memory. The system designer may choose to make the Vpp power-supply switchable or to "hardwire" $V_{PP} = V_{PPH}$. The IS28LV020 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read
The IS28LV020 has $\overline{CE}$ and $\overline{OE}$ control signals. To obtain data at the output, both control signals must be brought low. Chip-Enable ($\overline{CE}$) is used for device selection. Output-Enable ($\overline{OE}$) is used to gate data from the output pins, when the device is selected by asserting $\overline{CE}$ LOW. Refer to AC read timing waveforms.

When Vpp is HIGH (VPPH), the read operation can be used to access array data, to output the ISSI identifier codes, and to access data for program/erase verification. When Vpp is LOW (VPPL), the read operation can only access the array data.

Output Disable
When $\overline{OE}$ is HIGH (VIH), device output is disabled. The output pins are placed in a high-impedance state.

Standby
When $\overline{CE}$ is HIGH, the standby operation disables most of the IS28LV020's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output Enable signal. If the IS28LV020 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

ISSI Identifier Operation
The ISSI identifier operation outputs the manufacturer code (D5H) and device code (BD). Programming equipment automatically matches the device with its proper erase and programming algorithms.

With $\overline{CE}$ and $\overline{OE}$ both LOW, raising A9 to high voltage, VID activates the ISSI identifier operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer code and device code can also be read via the command register, for example, when the IS28LV020 is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (D5H). A read from address 0001H outputs the device code (BDH).

TABLE 1. IS28F020 BUS OPERATIONS[1]

	Operation	Vpp[2]	A0	A9	Pins CE	OE	WE	DQ0-DQ7
READ-ONLY	Read	VPPL	A0	A9	L	L	H	Data Out
	Output Disable	VPPL	X	X	L	H	H	Tri-State
	Standby	VPPL	X	X	H	X	X	Tri-State
	ISSI Identifier Mfr	VPPL	L	VID[3]	L	L	H	Data = D5H
	ISSI Identifier Device	VPPL	H	VID[3]	L	L	H	Data = BDH
READ/WRITE	Read	VPPH	A0	A9	L	L	H	Data Out[4]
	Output Disable	VPPH	X	X	L	H	H	Tri-State
	Standby	VPPH	X	X	H	X	X	Tri-State
	Write	VPPH	A0	A9	L	H	L	Data In[5]

NOTES:
1. $L = V_{IL}$; $H = V_{IH}$; X = Don't Care
2. Refer to DC Characteristics.
3. V_{ID} is the ISSI identifier high voltage. Refer to DC Characteristics.
4. Read operations with $V_{PP}=V_{PPH}$ may access array data or the ISSI identifier codes.
5. Refer to Table 2 for valid Data-In during a write operation.

TABLE 2. COMMAND DEFINITIONS

Command	Bus Cycles Req'd	FirstBusCycle Operation[1]	Address[2]	Data[2]	SecondBusCycle Operation[1]	Address[2]	Data[2]
Read Memory	1	Write	X	00H			
Read ISSI Identifier Codes (Mrf/Dev)	3	Write	X	90H	Read	0000H 0001H	D5H BDH
Setup Erase/Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Setup Program/Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 1.
2. EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the program command.

Write

With the V$_{PP}$ pin at high voltage level, device erasure and programming are accomplished via the command register. The contents of the command register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing $\overline{WE}$ low (V$_{IL}$), while $\overline{CE}$ is LOW. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used. Refer to AC Write Characteristics and the Erase/ Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

With the V$_{PP}$ pin at the low voltage level, the contents of the command register default to 00H, enabling read-only operations. With the V$_{PP}$ pin at high voltage, enabling read/ write operations. Device operations are selected by writing specific command codes to the command register. Table 2 defines these IS28LV020 register commands.

Read Command (00H)

While V$_{PP}$ = V$_{PPH}$, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H to the command register. Standard microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

Upon V$_{PP}$ power-up, the default value of the command register is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V$_{PP}$ power transition. Where the V$_{PP}$ supply is hard-wired to the IS28LV020, the device powers-up and remains enabled for reads until the command-register content is changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

ISSI Identifier Command (90H)

The ISSI's IS28LV020 flash memory is intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system.

The IS28LV020 contains an ISSI identifier operation to supplement traditional PROM-programming methods. This operation is initiated by writing 90H to the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of D5H. A read cycle from address 0001H returns the device code of BDH. To terminate the operation, it is necessary to write another valid command to the register.

Setup Erase/Erase Commands (20H/20H)

Two-step sequence of setup erase operation followed by erase operation ensures that the memory content is not accidentally erased.

The setup erase operation is initiated by writing 20H to the command register. Setup erase is a command-only operation that instructs the device for electrical erasure of all bytes in the array.

The erase command (20H) must again be written to the register. The erase command erases all bytes of the array in parallel. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command). Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command (A0H)

After each erase operation, all bytes must be verified. The erase-verify operation is initiated by writing A0H into the command register prior to each byte verification to latch its address. The address for the byte to be verified must be ready as it is latched on the falling edge of the Write-Enable control signal. The IS28LV020 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased. The process continues for each byte in the array until a byte does not return data FFH, or the last address is accessed.

In the case where the data read is not FFH, user should perform another erase operation. (Refer to Setup Erase/ Erase). Then verification can resume from the address of the last verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be reprogrammed. At this point, the verify operation is terminated by writing a valid command (e.g., Program Setup) to the command register. Figure 2, the Fast-Erase algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the IS28LV020. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Setup Program/Program Commands (40H)

The setup program operation is initiated by writing 40H to the command register. It is a command-only operation that instructs the device for byte programming. Once the setup program operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The IS28LV020 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. The programming operation terminates with the next rising edge of Write-Enable that used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command (C0H)

Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H to the command register. It instructs the device for verification of the byte last programmed. The IS28LV020 applies an internally-generated margin voltage to the byte. A standard microprocessor read cycle may output the data. If a comparison between the programmed byte and the true data is successful, programming then proceeds to the next desired byte location. Figure 1, the IS28LV020 Fast-Pulse programming algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command (FFH)

A reset command is used to abort the erase- or program-command sequences safely. Following either setup erase operation or setup program operation with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

ERASE/PROGRAM CYCLING

The IS28LV020 is programmed and erased using ISSI's Fast-Pulse programming and Fast-Erase algorithms. The algorithmic approach uses a series of pulses, along with byte verification, to completely and reliably erase and program the device.

FAST-PULSE PROGRAMMING ALGORITHM

The IS28LV020 is programmed on a byte-by-byte basis using 10 µs duration programming pulse in accordance with ISSI's Fast-Pulse programming algorithm. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 1 illustrates the Fast-Pulse Programming algorithm.
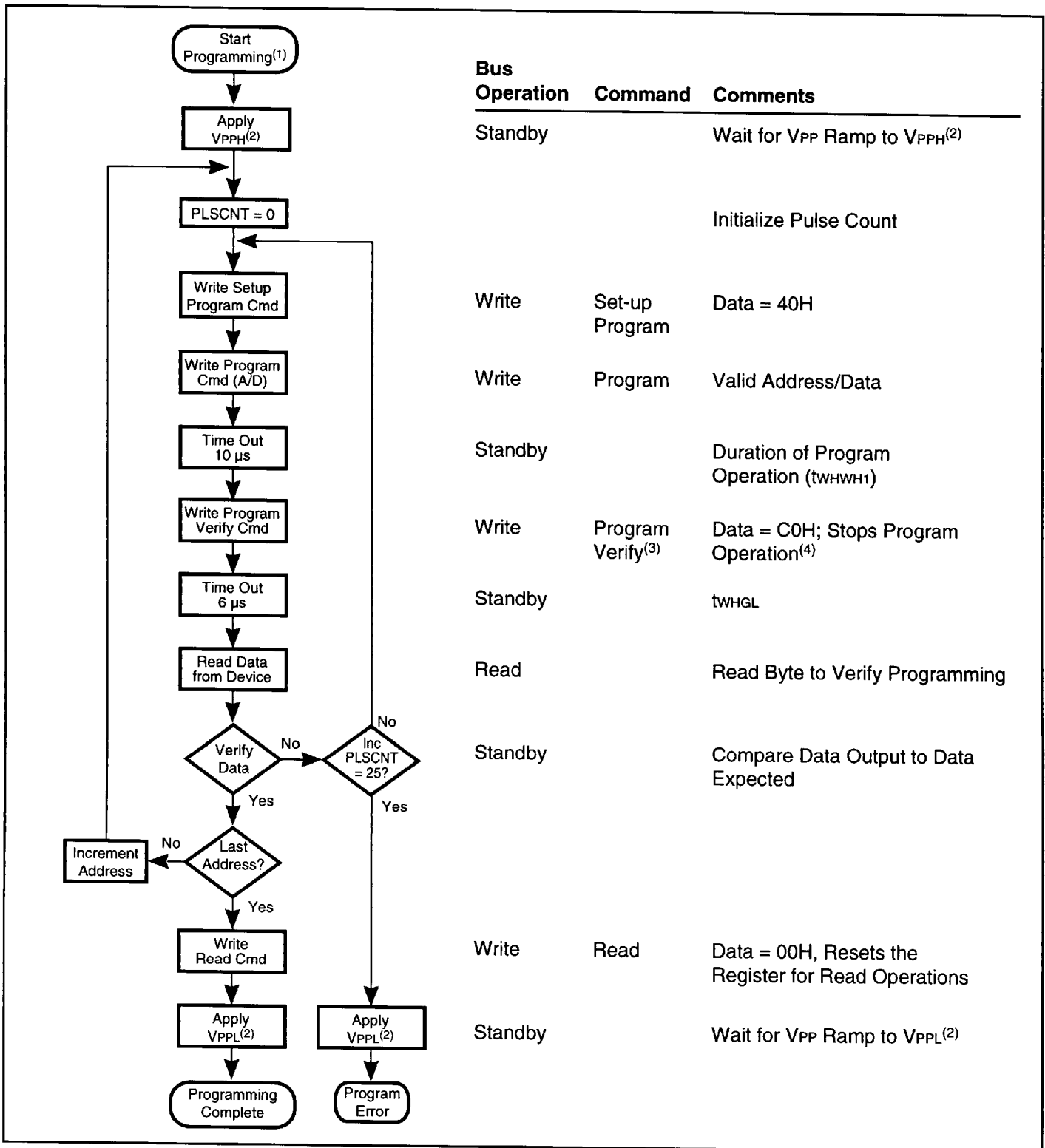
FAST-ERASE ALGORITHM

The erase operation erases all bytes of the array in parallel. The entire device is bulk erased using 10 ms duration erase pulse in accordance with ISSI's Fast-Erase algorithm. The Fast-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a Fowler-Nordheim tunneling to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The IS28F020 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data=00H). This is accomplished, using the Fast-Pulse Programming algorithm, in approximately two seconds.

Erase execution then continues with an initial erase operation. Erase verification (Data=FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 2 illustrates the Fast-Erase algorithm.
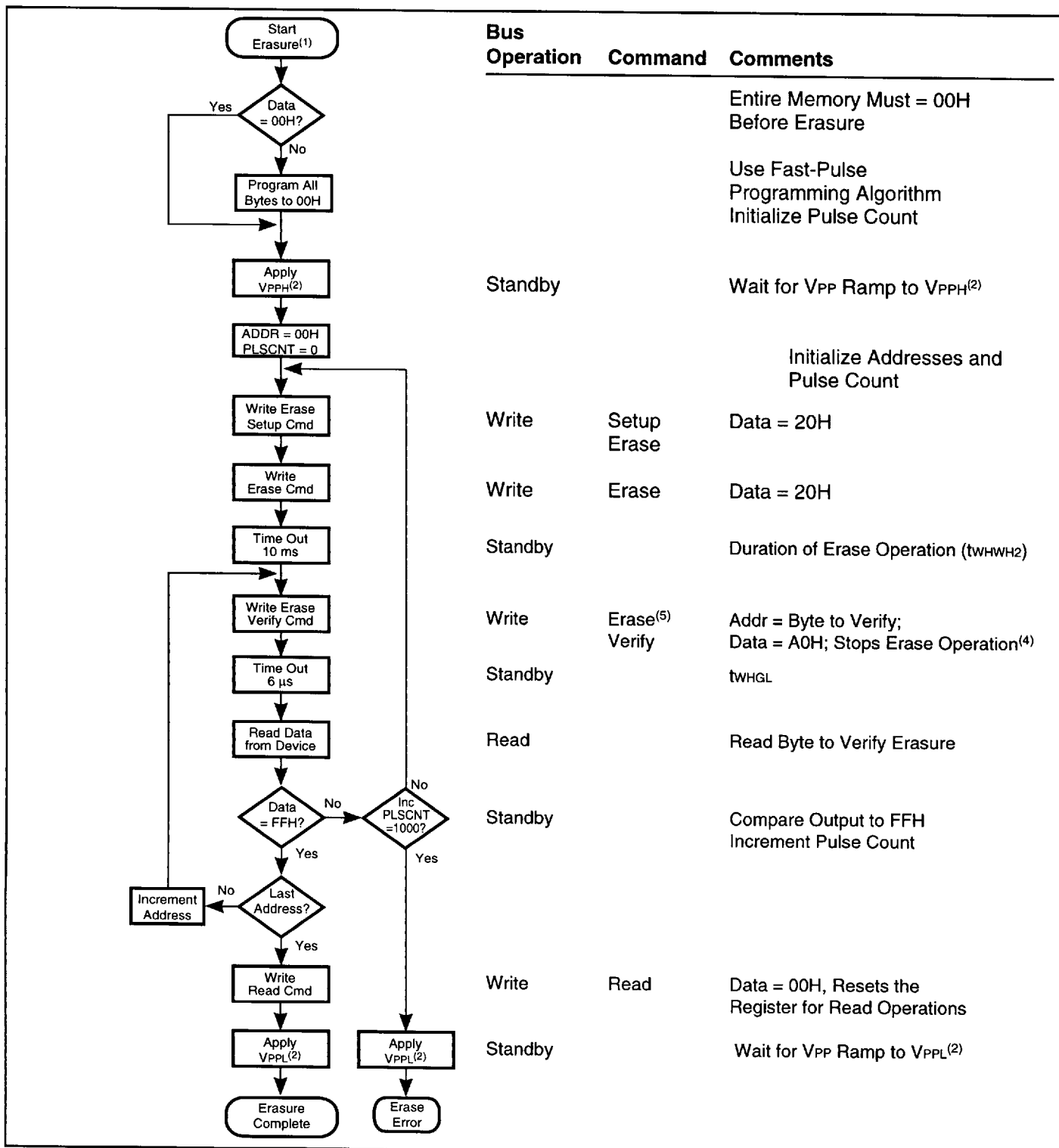
9004404 0000777 250

FIGURE 1. IS28LV020 FAST-PULSE PROGRAMMING ALGORITHM[1]

Bus Operation	Command	Comments
Standby		Wait for V$_{PP}$ Ramp to V$_{PPH}$[2]
		Initialize Pulse Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t$_{WHWH1}$)
Write	Program Verify[3]	Data = C0H; Stops Program Operation[4]
Standby		t$_{WHGL}$
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V$_{PP}$ Ramp to V$_{PPL}$[2]

NOTES:
1. The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of V$_{PPH}$ and V$_{PPL}$.
3. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

Integrated Silicon Solution, Inc.

■ 9004404 0000778 197 ■

FIGURE 2. IS28LV020 FAST-ERASE ALGORITHM[1]

Bus Operation	Command	Comments
		Entire Memory Must = 00H Before Erasure
		Use Fast-Pulse Programming Algorithm Initialize Pulse Count
Standby		Wait for V_{PP} Ramp to V_{PPH}[2]
		Initialize Addresses and Pulse Count
Write	Setup Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase[5] Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation[4]
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse Count
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}[2]

NOTES:
1. The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
3. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.
5. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the Read command.

9004404 0000779 023

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V$_{TERM}$	Terminal Voltage with Respect to GND		
	During Erase/Program	−2.0 to +14.0[2,3]	V
	Any Pin	−2.0 to +7.0[3]	V
	A9	−2.0 to +13.5[2,3]	V
	Vcc	−2.0 to +7.0[2]	V
T$_A$	Commercial Operating Temperature		
	During Read	0 to +70	°C
	During Read	0 to +70	°C
T$_{BIAS}$	Temperature Under Bias	−10 to +80	°C
T$_{STG}$	Storage Temperature	−65 to +125	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 10 ns. Maximum DC voltage on output pins is Vcc + 0.5V, which may overshoot to Vcc + 2.0V for periods less than 10 ns.
3. Maximum DC voltage on A9 or V$_{PP}$ may overshoot to +14.0V for periods less than 20 ns.
4. No more than one output shorted at one time. Duration of short shall not exceed one second.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3V ± 10%

Note:
1. Operating ranges define those limits between which the functionally of the device is guaranteed.

CAPACITANCE

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 0V	—	6	pF
C$_{OUT}$	Output Capacitance	V$_{OUT}$ = 0V	—	12	pF

DC CHARACTERISTICS: TTL/NMOS COMPATIBLE

Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I$_{LI}$	Input Leakage Current	V$_{CC}$ = V$_{CC}$ Max., V$_{IN}$ = V$_{CC}$ or GND		—	±1.0	μA
I$_{LO}$	Output Leakage Current	V$_{CC}$ = V$_{CC}$ Max., V$_{OUT}$ = V$_{CC}$ or GND		—	±10	μA
I$_{CCS}$	V$_{CC}$ Standby Current	V$_{CC}$ = V$_{CC}$ Max., $\overline{CE}$ = V$_{IH}$		—	1.0	mA
I$_{CC1}$	V$_{CC}$ Active Read Current	V$_{CC}$ = V$_{CC}$ Max., $\overline{CE}$ = V$_{IL}$, $\overline{OE}$ = V$_{IH}$ I$_{OUT}$ = 0 mA, at 6 MHz		—	30	mA
I$_{CC2}$	V$_{CC}$ Programming Current	$\overline{CE}$ = V$_{IL}$ Programming in Process	Com.	—	10	mA
I$_{CC3}$	V$_{CC}$ Erase Current	$\overline{CE}$ = V$_{IL}$ Erasure in Process	Com.	—	15	mA
I$_{CC4}$	V$_{CC}$ Program Verify Current	V$_{PP}$ = V$_{PPH}$ Program Verify in Process	Com.	—	15	mA
I$_{CC5}$	V$_{CC}$ Erase Verify Current	V$_{PP}$ = V$_{PPH}$ Erase Verify in Process	Com.	—	15	mA
I$_{PPS}$	V$_{PP}$ Leakage Current	V$_{PP}$ ≤ V$_{CC}$		—	±10	μA
I$_{PP1}$	V$_{PP}$ Read Current	V$_{PP}$ > V$_{CC}$ V$_{PP}$ ≤ V$_{CC}$		— —	200 ±10	μA
I$_{PP2}$	V$_{PP}$ Programming Current	V$_{PP}$ = V$_{PPH}$ Programming in Process		—	30	mA
I$_{PP3}$	V$_{PP}$ Erase Current	V$_{PP}$ = V$_{PPH}$ Erasure in Process		—	30	mA
I$_{PP4}$	V$_{PP}$ Program Verify Current	V$_{PP}$ = V$_{PPH}$ Program Verify in Process		—	5.0	mA
I$_{PP5}$	V$_{PP}$ Erase Verify Current	V$_{PP}$ = V$_{PPH}$ Erase Verify in Process		—	5.0	mA
V$_{IL}$	Input Low Voltage			−0.5	0.8	V
V$_{IH}$	Input High Voltage			2.0	V$_{CC}$ + 0.5	V
V$_{OL}$	Output Low Voltage	I$_{OL}$ = 5.8 mA, V$_{CC}$ = V$_{CC}$ Min.		—	0.45	V
V$_{OH1}$	Output High Voltage	I$_{OH}$ = −2.5 mA, V$_{CC}$ = V$_{CC}$ Min.		2.4	—	V
V$_{ID}$	A9 Auto Select Voltage	A9 = V$_{ID}$		11.5	13.0	V
I$_{ID}$	A9 Auto Select Current	A9 = V$_{ID}$ Max., V$_{CC}$ = V$_{CC}$ Max.		—	200	μA
V$_{PPL}$	V$_{PP}$ During Read-Only Operations	**Note:** Erase/Program are inhibited when V$_{PP}$ = V$_{PPL}$		0.0	V$_{CC}$ + 2.0	V
V$_{PPH}$	V$_{PP}$ During Read/Write Operations			11.4	12.6	V
V$_{LKO}$	V$_{CC}$ Erase/Write Lock Voltage			2.5	—	V

■ Ꝺ004404 0000781 781 ■

DC CHARACTERISTICS: CMOS COMPATIBLE

Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or GND		—	±1.0	μA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or GND		—	±10	μA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ± 0.2V		—	100	μA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		—	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Process	Com.	—	15	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Process	Com.	—	15	mA
I_{CC4}	V_{CC} Program Verify Current	V_{PP} = V_{PPH} Program Verify in Process	Com.	—	15	mA
I_{CC5}	V_{CC} Erase Verify Current	V_{PP} = V_{PPH} Erase Verify in Process	Com.	—	15	mA
I_{PPS}	V_{PP} Leakage Current	$V_{PP} \leq V_{CC}$		—	±10	μA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		—	200	μA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Process		—	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Process		—	30	mA
I_{PP4}	V_{PP} Program Verify Current	V_{PP} = V_{PPH} Program Verify in Process		—	5.0	mA
I_{PP5}	V_{PP} Erase Verify Current	V_{PP} = V_{PPH} Erase Verify in Process		—	5.0	mA
V_{IL}	Input Low Voltage			−0.5	0.8	V
V_{IH}	Input High Voltage			0.7V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, V_{CC} = V_{CC} Min.		—	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA, V_{CC} = V_{CC} Min.		0.85 x V_{CC}	—	V
V_{OH1}	Output High Voltage	I_{OH} = −100 μA, V_{CC} = V_{CC} Min.		V_{CC} − 0.4	—	V
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}		11.5	13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max., V_{CC} = V_{CC} Max.		—	200	μA
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}		0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} During Read/Write Operations			11.4	12.6	V
V_{LKO}	V_{CC} Erase/Write Lock Voltage			2.5	—	V

■ 9004404 0000782 618 ■

SWITCHING CHARACTERISTICS[1]: READ ONLY (Over Operating Range)

JEDEC Symbol	Std. Symbol	Parameter	-90 Min.	-90 Max.	-120 Min.	-120 Max	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	90	—	120	—	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	—	90	—	120	ns
t_{AVQV}	t_{ACC}	Address Access Time	—	90	—	120	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	—	35	—	50	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	0	—	0	—	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	—	45	—	50	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	0	—	0	—	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	—	30	—	30	ns
t_{AXQX}	t_{OH}	Output Hold from First of Address, $\overline{CE}$ or $\overline{OE}$ Change	0	—	0	—	ns
t_{WHGL}		Write Recovery Time before Read	6	—	6	—	µs

Notes:

1. Output load: 1 TTL Gate and C_L = 30 pF, input Rise and Fall times: ≤ 10 ns, input pulse levels: 0 to 3 V, timing measurement reference level: Inputs: 1.5V
   Outputs: 1.5V

SWITCHING WAVEFORM: READ ONLY

■ 9004404 0000783 554 ■
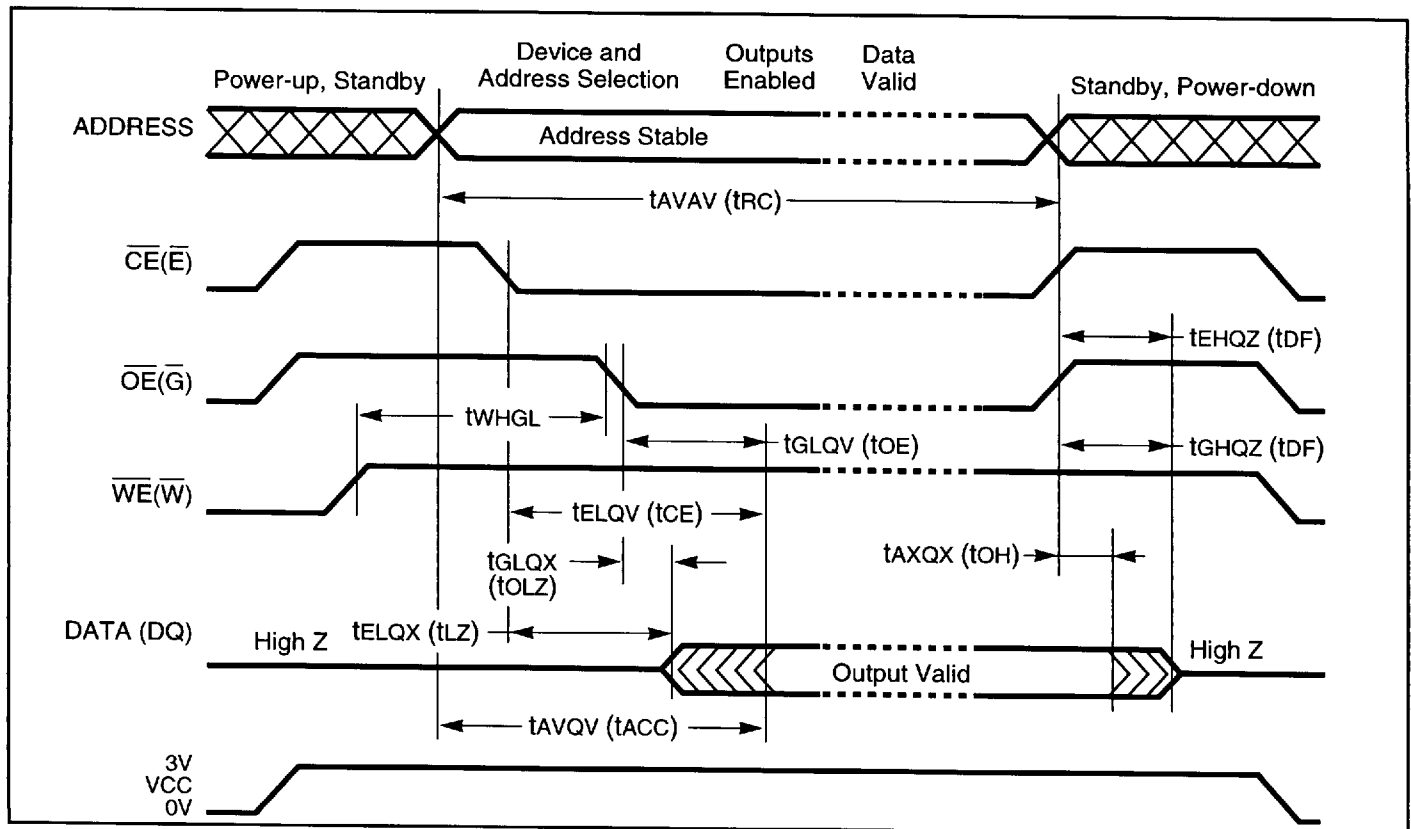
SWITCHING CHARACTERISTICS: WRITE/ERASE PROGRAM[1] (Over Operating Range)

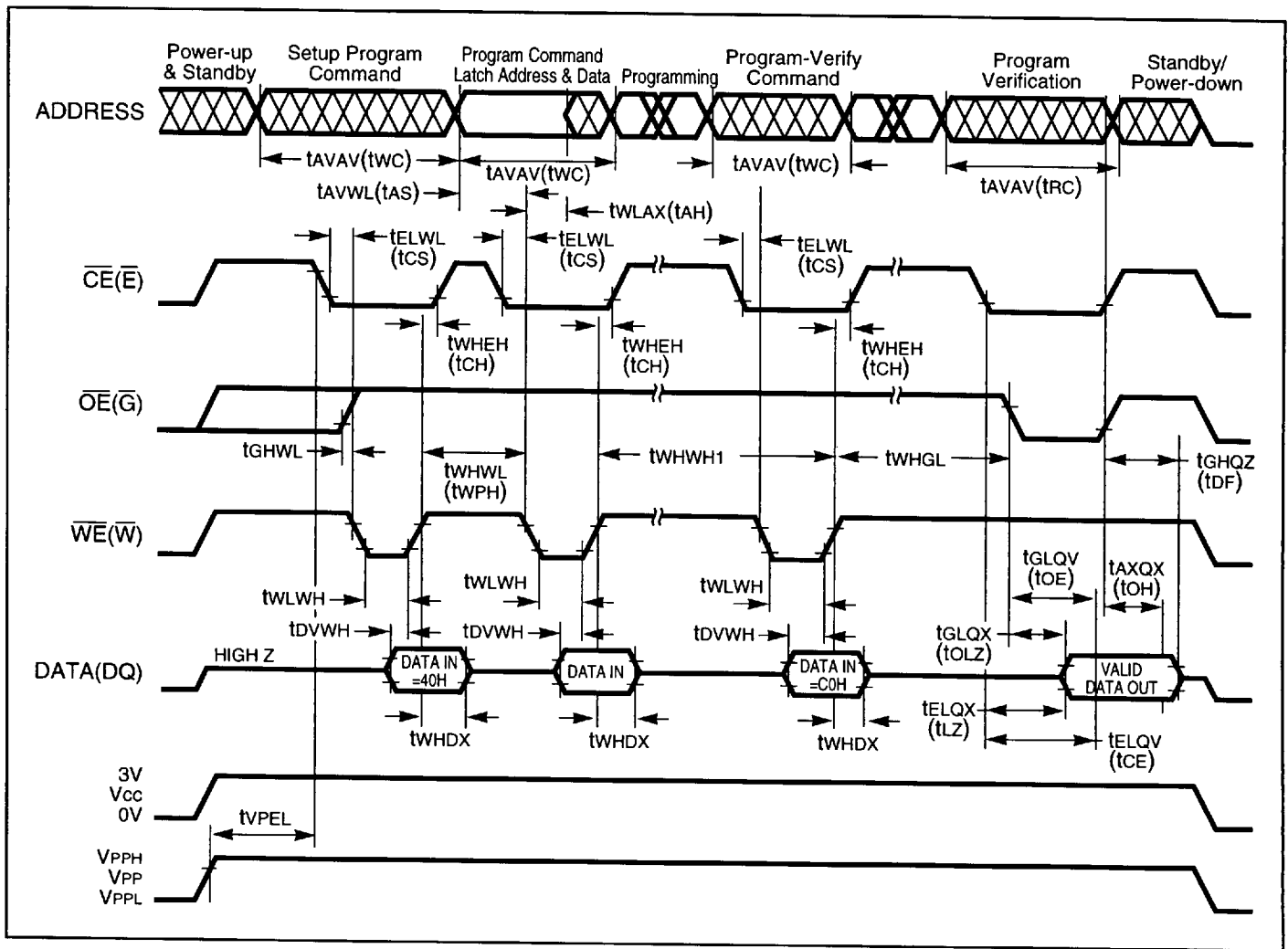| JEDEC Symbol	Std. Symbol	Parameter	-90 Min.	-90 Max.	-120 Min.	-120 Max	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	90	—	120	—	ns
t_{AVWL}	t_{AS}	Addess Setup Time	0	—	0	—	ns
t_{WLAX}	t_{AH}	Address Hold Time	40	—	40	—	ns
t_{DVWH}	t_{DS}	Data Setup Time	45	—	45	—	ns
t_{WHDX}	t_{DH}	Data Hold Time	10	—	10	—	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6	—	6	—	μs
t_{GHWL}		Read Recovery Time before Write	0	—	0	—	μs
t_{ELWL}	t_{CS}	Chip Enable Setup Time before Write	15	—	15	—	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	0	—	0	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width	40	—	60	—	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	20	—	20	—	ns
t_{WHWH1}		Duration of Programming Operation[2]	10	—	10	—	μs
t_{WHWH2}		Duration of Erase Operation[2]	9.5	—	9.5	—	ms
t_{VPEL}		V_{PP} Setup Time to Chip Enable LOW	1.0	—	1.0	—	μs

Notes:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.
2. The integrated stop timer terminates the programming/erase operations, thereby eliminating the need for a maximum specification.

SWITCHING WAVEFORM: ERASE OPERATION

■ 9004404 0000785 327 ■

SWITCHING WAVEFORM: PROGRAMMING OPERATION

9004404 0000786 263
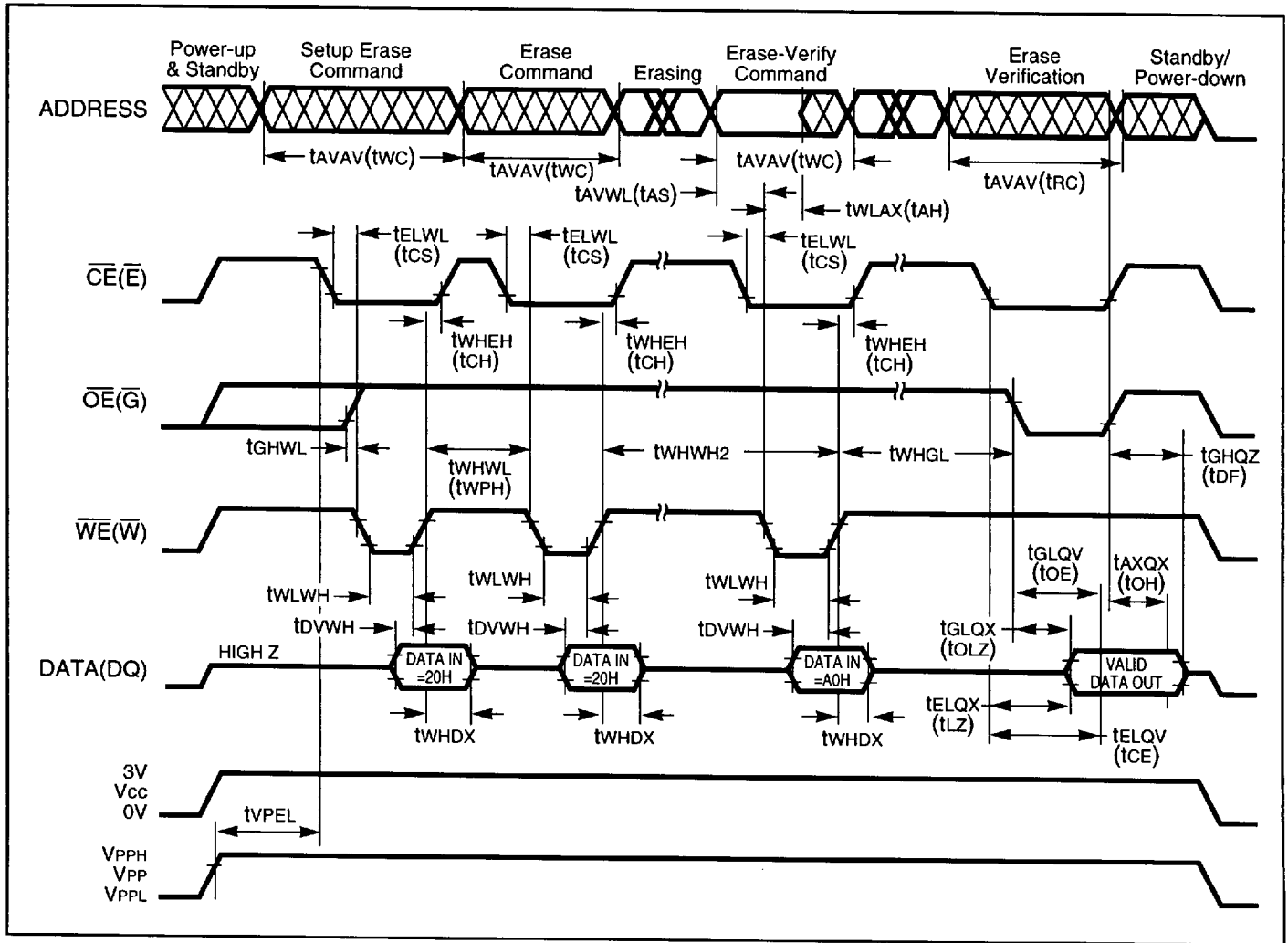
SWITCHING CHARACTERISTICS:
ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES[1] (Over Operating Range)

JEDEC Symbol	Std. Symbol	Parameter	-90 Min.	-90 Max.	-120 Min.	-120 Max	Unit
tAVAV	tWC	Write Cycle Time	90	—	120	—	ns
tAVEL	tAS	Addess Setup Time	0	—	0	—	ns
tELAX	tAH	Address Hold Time	50	—	55	—	ns
tDVEH	tDS	Data Setup Time	45	—	45	—	ns
tEHDX	tDH	Data Hold Time	10	—	10	—	ns
tEHGL	tWR	Write Recovery Time before Read	6	—	6	—	µs
tGHEL		Read Recovery Time before Write	0	—	0	—	µs
tWLEL		Write Enable Setup Time before Chip Enable	0	—	0	—	ns
tEHWH		Write Enable Hold Time	0	—	0	—	ns
tELEH	tWP	Write Pulse Width	50	—	70	—	ns
tEHEL	tWPH	Write Pulse Width HIGH	20	—	20	—	ns
tEHEH1		Duration of Programming Operation[2]	10	—	10	—	µs
tEHEH2		Duration of Erase Operation[2]	9.5	—	9.5	—	ms
tVPEL		VPP Setup Time to Chip Enable LOW	1.0	—	1.0	—	µs

Notes:

1. Chip Enable Controlled Writes: Write operations are driven by the valid combination of Chip Enable and Write Enable. In system where Chip Enable defines the write pulse width all setup, hold and inactive Write Enable times should be measured relative to the Chip Enable waveform.

2. The integrated stop timer terminates the programming/erase operations, thereby eliminating the need for a maximum specification.

■ ٩004404 0000787 1TT ■

ALTERNATIVE SWITCHING WAVEFORM: PROGRAMMING OPERATION
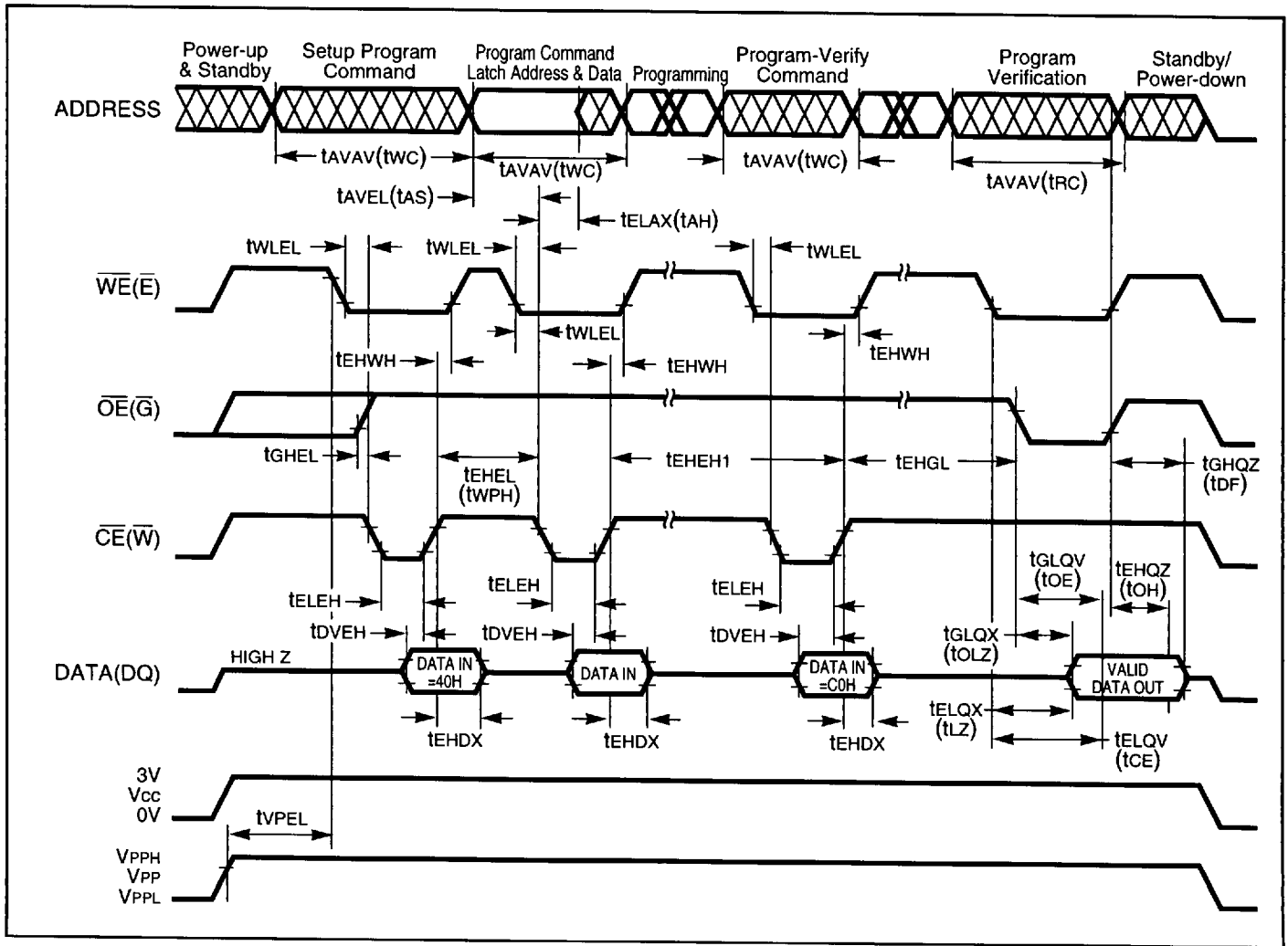
Notes:

1. Alternative $\overline{CE}$-Controlled Write Timings also apply to Erase Operations.

ORDERING INFORMATION

Commerical Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
90	IS28LV020-90W	600-mil Plastic DIP
90	IS28LV020-90PL	PLCC – Plastic Leaded Chip Carrier
90	IS28LV020-90T	TSOP
120	IS28LV020-12W	600-mil Plastic DIP
120	IS28LV020-12PL	PLCC – Plastic Leaded Chip Carrier
120	IS28LV020-12T	TSOP

█ ꟼ004404 0000789 T72 █

ISSI

400-mil Plastic DIP
Package Code: M
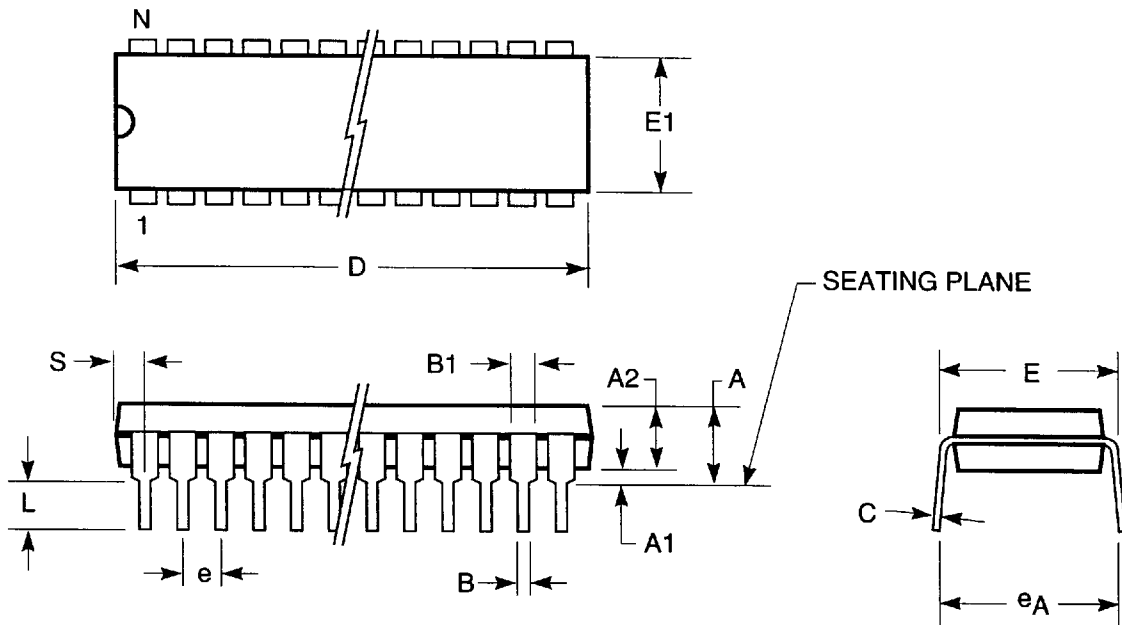
400-mil Plastic DIP (M)

Symbol	Inches Min	Max
Ref. Std.		
N	32	
A	—	0.200
A1	0.015	—
A2	0.145	0.155
B	0.016	0.022
B1	0.058	0.064
C	0.008	0.015
D	—	1.620
E	0.400	0.420
E1	0.380	0.390
e_A	0.430	0.470
e	0.100 BSC	
L	0.120	0.140
S	—	0.065

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Integrated Silicon Solution, Inc.

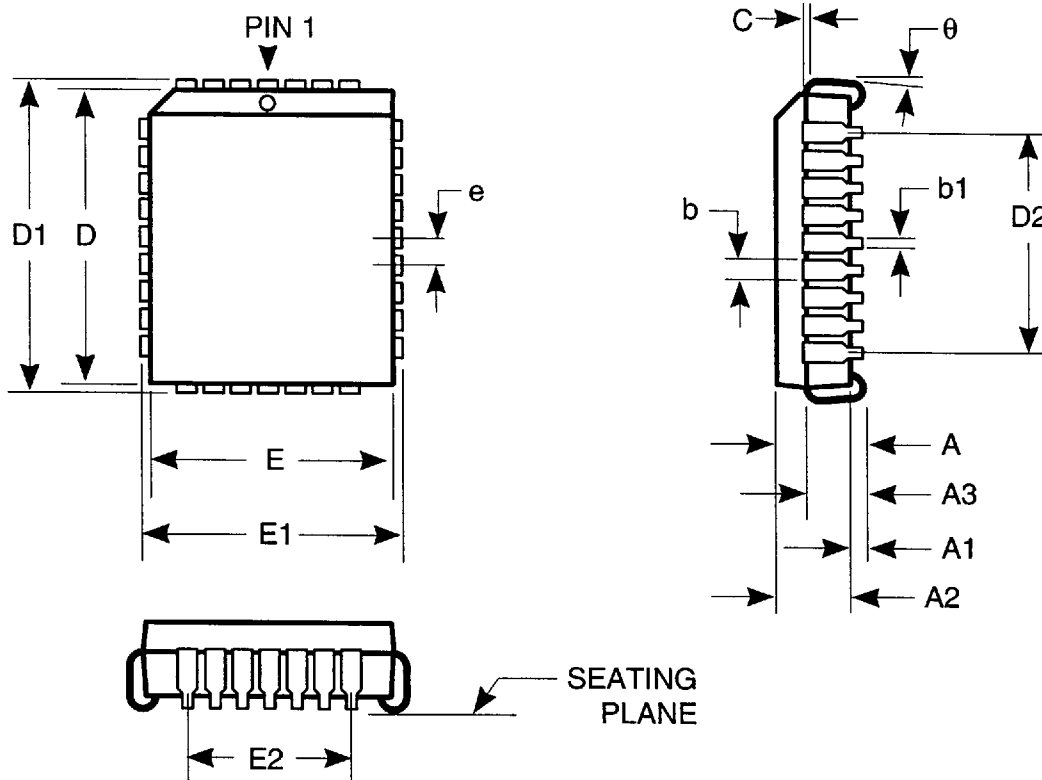PK13197M   Rev. B   01/31/97

■ 9004404 0000544 T42 ■

PLCC (Plastic Leaded Chip Carrier)
Package Code: PL

| Plasstic Leaded Chip Carrier (PL)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		32		
A	3.33	3.56	0.131	0.140
A1	0.50	—	0.020	—
A2	2.67	2.93	0.105	0.115
A3	1.91	2.41	0.075	0.095
b	0.66	0.81	0.026	0.032
b1	0.33	0.54	0.013	0.021
C	0.20	0.35	0.008	0.014
D	13.89	14.05	0.547	0.553
D1	14.86	15.10	0.585	0.595
D2	—	10.16	—	0.400
E	11.35	11.51	0.447	0.453
E1	12.32	12.57	0.485	0.495
E2	—	7.62	—	0.300
e	1.27 BSC		0.050 BSC	
θ	0°	10°	0°	10°

Notes:
1. Controlling dimension: millimeters/inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.
5. ND and NE represent the number of leads in D and E directions, respectively.
6. D1 and E1 should be measured from the bottom of the package.

9004404 0000546 815

Plastic TSOP - 32 pins
Package Code: T (Type I)
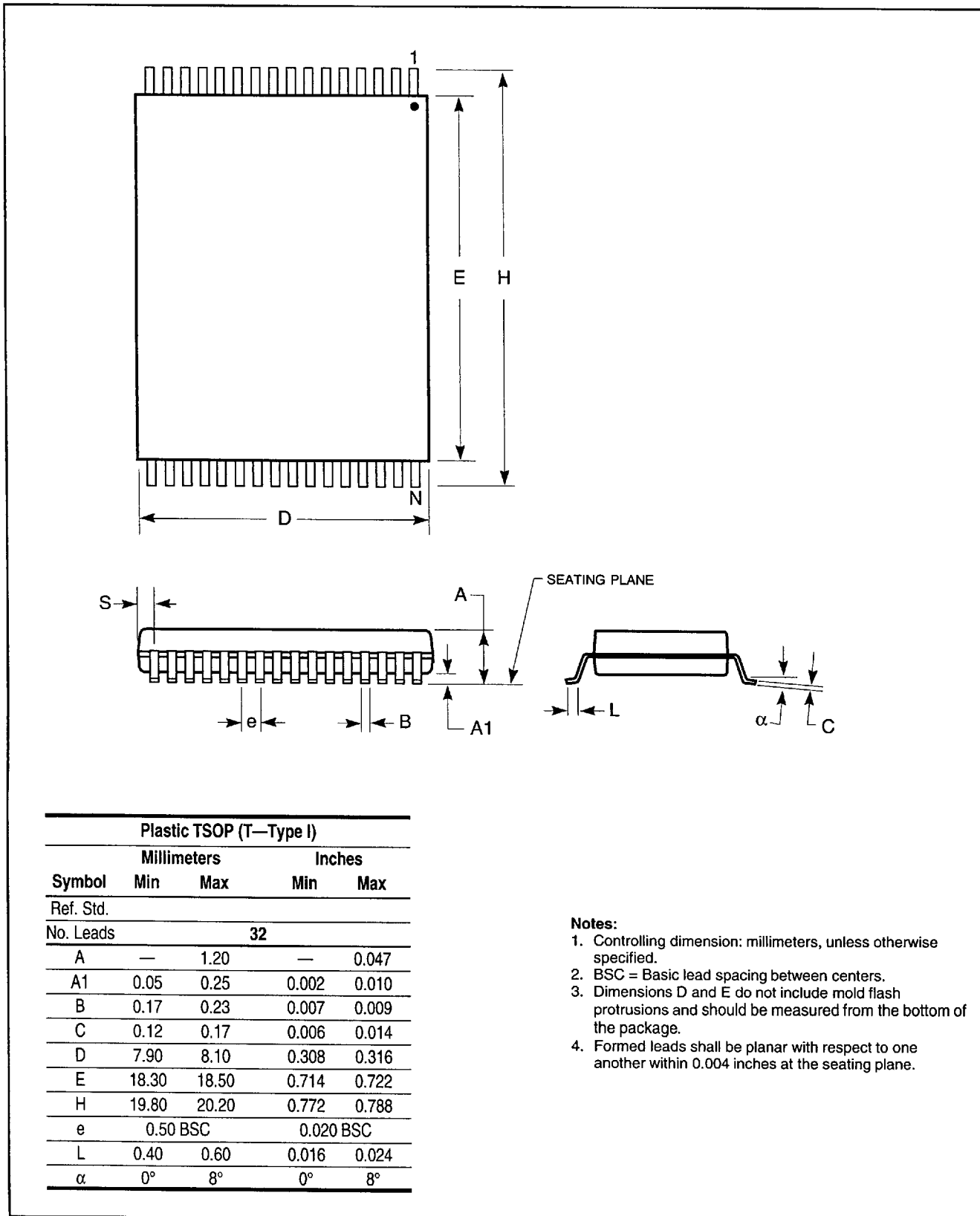
Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		32		
A	—	1.20	—	0.047
A1	0.05	0.25	0.002	0.010
B	0.17	0.23	0.007	0.009
C	0.12	0.17	0.006	0.014
D	7.90	8.10	0.308	0.316
E	18.30	18.50	0.714	0.722
H	19.80	20.20	0.772	0.788
e	0.50 BSC		0.020 BSC	
L	0.40	0.60	0.016	0.024
α	0°	8°	0°	8°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Integrated Silicon Solution, Inc.

9004404 0000564 830

22