8M x 16 SDRAM
SYNCHRONOUS DRAM MEMORY

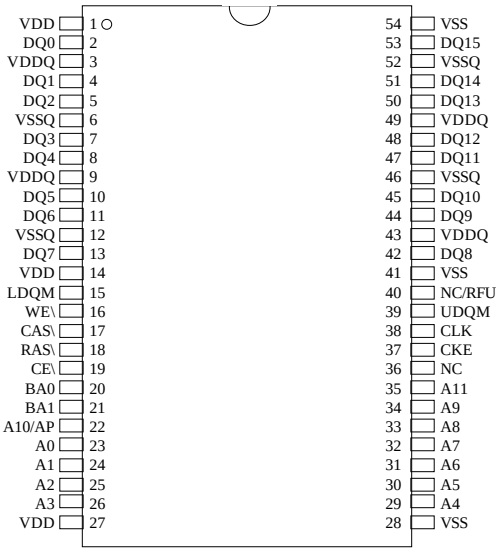
FEATURES
- Single 3.3V Power Supply
- Fully Synchronous to positive Clock Edge
- SDRAM CAS Latency = 2 (66 MHz), 3 (75 MHz or 83 MHz)
- Burst Operation
  - Sequential or Interleave
  - Burst length = programmable 1, 2, 4, 8 or full page
  - Burst Read and Write
  - Multiple Burst Read and Single Write
- DATA Mask Control per byte
- Auto Refresh (CBR) and Self Refresh
  - 4096 refresh cycles across 64ms
- Automatic and Controlled Precharge Commands
- Suspend Mode and Power Down Mode

OPTIONS — MARKING

- **Timing**
  12ns access — -12

- **Package(s)•**
  Plastic 54-pin TSOP — DG — No. 901

PIN ASSIGNMENT
(Top View)



GENERAL DESCRIPTION
The AS4SD8M16 is a synchronous, high data rate, 134,217,728 bit DRAM organized as 4 x 2,097,152 words x 16 bits. The synchronous design allows precise cycle control with the use of system clock, I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

The AS4SD8M16 comes in a 54 pin TSOP package and is tested over the industrial temp range (-40°C to +85°C) providing a solution for rugged main memory applications.

For more products and information please visit our web site at
www.austinsemiconductor.com

PIN DESCRIPTION

CLK	Clock Input
CKE	Clock Enable
RAS\	Row Address Strobe
CAS\	Column Address Strobe
WE\	Write Enable
CE\	Chip Select
A0-A11	Address Inputs
BA0, BA1	Bank Select Address
DQ0-DQ15	Data Input/Output
L(U)DQM	Data Input/Output Mask
V_{CC}	Power (3.3V)
V_{CCQ}	Data Output Power
V_{SS}	Ground
V_{SSQ}	Data Output Ground

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

SYMBOL	TYPE	SIGNAL	POLARITY	FUNCTION
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
CE	Input	Pulse	Active Low	CE disable or enable device operation by masking or enabling all inputs except CK0, CKE and DQM.
RAS, CAS, WE	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, CAS, RAS, WE define the operation to be executed by the SDRAM.
BA0,BA1	Input	Level	---	Selects which SDRAM bank is to be active.
A0-A11, A10/AP	Input	Level	---	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A7 defines the column address (CA0-CA7) when sampled at the rising edge of the clock. In additions to the row address, A10/AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycles. If A10/AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10/AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If A10/AP is high, all banks will be precharged regardless of the state of BA0, BA1. If A10/AP is low, then BA0, BA1 is used to define which bank to precharge.
DQ0-DQ15	Input Output	Level	---	Data Input/Output are multiplexed on the same pins.
L(U)DQM	Input	Pulse	Mask Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like and output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the Write operation if DQM is high.
VDD, VSS	Supply			Power and ground for the input buffers and the core logic.
VDDQ, VSSQ	Supply			Isolated power and ground for the output buffers to improve noise immunity.

ABSOLUTE MAXIMUM RATINGS *

Power Supply Voltage.....-1.0V to +4.6V
Input Voltage.....-1.0V to +4.6V
Output Voltage.....-1.0V to +4.6V
Operating Temperature.....-40°C to +85°C
Storage Temperature.....-55°C to +125°C
Short Circuit Output Current (per I/O)….....50mA
Power Dissipation .....1.0 W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CHARACTERISTICS

Voltage referenced to VSS = 0V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	RATING			UNITS	NOTES
		Min.	Typ.	Max.		
VDD	Supply Voltage	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	3.0	VDD + 0.3	V	
V_{IL}	Input Low Voltage	-0.3	---	0.8	V	
V_{OH}	Output High Voltage	2.4	---	---	V	I_{OH} = -2mA
V_{OL}	Output Low Voltage	---	---	0.4	V	I_{OL} = 2mA
I_{IL}	Input Leakage Voltage	-5	---	5	µA	
I_{OL}	Output Leakage Voltage	-5	---	5	µA	

CAPACITANCE

(T_A=25°C, f=1MHz, VDD = 3.3V to 3.6V)

SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A0-A12, BA)		4	pF	
C_{I2}	Input Capacitance (CLK, CKE, RAS, CAS, WE, CE, DQM)		4	pF	
C_{out}	Input/Output Capacitance (DQ0-DQ71)		5	pF	

OPERATING CURRENT CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	-12	UNITS	NOTES
Operating Current (One Bank Active)	I_{CC1}	Burst Length = 1 $t_{rc} \geq t_{rc}$(MIN)	125	mA	
Operating Current (Burst Mode)	I_{CC4}	Page Burst, 2 banks active t_{ccd} = 2 clocks	165	mA	
Precharge Standby Current in Power Down Mode	$I_{CC2}P$	CKE $\leq V_{IL}$(MAX), t_{CK} = 15ns	2	mA	
	$I_{CC2}PS$	CKE, CLK$\leq V_{IL}$(MAX) t_{CK} = Infinity, inputs stable	2	mA	
Precharge Standby Current in Non-Power Down Mode	$I_{CC1}N$	CKE $\leq V_{IH}$, t_{CK} = 15ns Input Chagne every 30ns	50	mA	
	$I_{CC1}NS$	CKE$\geq V_{IH}$(MIN) t_{CK} = Infinity No Input Change	35	mA	
Active Standby Current in Power Down Mode	$I_{CC3}P$	CKE$\leq V_{IL}$(MAX), t_{CK} = 15ns	12	mA	
	$I_{CC3}PS$	CKE$\leq V_{IL}$(MAX), t_{CK} = Infinity	12	mA	
Active Standby Current in Non-Power Down Mode	$I_{CC2}N$	CKE $\leq V_{IH}$, t_{CK} = 15ns Input Chagne every 30ns	30	mA	
	$I_{CC2}NS$	CKE$\geq V_{IH}$(MIN) t_{CK} = Infinity No Input Change	20	mA	
Refresh Current	I_{CC5}	$t_{rc} \geq t_{rc}$ (MIN)	210	mA	2
Self Refresh Current	I_{CC6}	CKE$\leq$0.2V	3	mA	

RECOMMENDED AC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER		-12		UNITS	NOTES
			MIN	MAX		
t_{CC}	Clock cycle time	CAS Latency = 3	12	1000	ns	1
		CAS Latency = 2	15	1000		
t_{SAC}	Clock to valid Output delay		---	8	ns	1,2
t_{OH}	Output data hold time		3	---	ns	2
t_{CH}	Clock high pulse width		4.0	---	ns	3
t_{CL}	Clock low pulse width		4.0	---	ns	3
t_{SS}	Input set-up time		3	---	ns	3
t_{SH}	Input hold time		1	---	ns	3
t_{SLZ}	CLK to output Low-Z		1	---	ns	2
t_{SHZ}	CLK to output High-Z		---	8	ns	
t_{RRD}	Row active to row active delay		24	---	ns	4
t_{RCD}	RAS\ to CAS\ delay		26	---	ns	4
t_{RP}	Row precharge time		26	---	ns	4
t_{RAS}	Row active time		60	100,000	ns	4
t_{RC}	Row cycle time (operation)		90	---	ns	4
t_{RFC}	Row cycle time (auto refresh)		90	---	ns	4,8
t_{CDL}	Last data in to new column address delay		1	---	CLK	5
t_{RDL}	Last data in to row precharge		1	---	CLK	5
t_{BDL}	Last data in to burst stop		1	---	CLK	5
t_{CCD}	Column address to column address delay		1	---	CLK	6
	Number of Valid output data	CAS Latency = 3	2	---	ea	7
		CAS Latency = 2	1	---		

NOTES:

1) Parameters depend on programmed CAS latency.

2) If clock rise item is longer then 1ns, (t_{rise}/2-0.5)ns should be added to the parameter.

3) Assumed input rise and fall time = 1ns. If t_{rise} or t_{fall} are longer than 1ns. ((t_{rise} + t_{fall})/2)-1ns should be added to the parameter.

4) The minimum number of clock cycles required is determined by dividing the minimum time required by the clock cycle time and then rounding up to the higher integer.

5) Minimum delay is required to complete write.

6) All devices allow every cycle column address changes

7) In case of row precharge interrupt, auto precharge and read burst stop.

8) A new command may be given t_{RFC} after self refresh exit.

REFRESH CYCLE PARAMETERS

SYMBOL	PARAMETER	-12		UNITS	NOTES
		MIN	MAX		
t_{REF}	Refresh Period	---	64	ms	1,2
t_{SREX}	Self Refresh Exit Time	t_{RFC}	---	ns	3

NOTES:
1) 4,096 cycles
2) Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be to "wake-up" the device.
3) The self refresh in exited by restarting the external clock and then asserting CKE high. This must be followed by NOPs for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation.

CLOCK FREQUENCY AND LATENCY PARAMETERS
(units in number of clocks)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12ns)	3	8	5	3	2	3	1	1	1
75MHz (12ns)	3	7	5	2	2	2	1	1	1
66MHz (15ns)	2	6	4	2	2	2	1	1	1

COMMAND TRUTH TABLE

FUNCTION	CKE		CE	RAS	CAS	WE	DQM	BA	A10/AP	A12, A11, A9-A0	NOTES
	PREVIOUS CYCLE	CURRENT CYCLE									
Mode Register Set	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	H	H	L	L	L	H	X	X	X	X	
Entry Self Refresh	H	L	L	L	L	H	X	X	X	X	
Single Bank Precharge	H	X	L	L	H	L	X	BA	L	X	2
Precharge all Banks	H	X	L	L	H	L	X	X	H	X	
Bank Activate	H	X	L	L	H	H	X	BA	Row Address		2
Write	H	X	L	H	L	L	X	BA	L	Column	2
Write with Auto-Precharge	H	X	L	H	L	L	X	BA	H	Column	2
Read	H	X	L	H	L	H	X	BA	L	Column	2
Read with Auto-Precharge	H	X	L	H	L	H	X	BA	H	Column	2
Burst Termination	H	X	L	H	H	L	X	X	X	X	3
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Clock Suspend/Standby Mode	L	X	X	X	X	X	X	X	X	X	4
Data Write/Output Enable	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	H	X	X	X	X	X	H	X	X	X	5
Power Down Mode Entry	X	L	H	X	X	X	X	X	X	X	6
Power Down Mode Exit	X	H	H	X	X	X	X	X	X	X	6

NOTES:
1) All of the SDRAM operations are defined by states of CE, WE, RAS, CAS, and DQM at the positive rising edge of the clock.
2) Bank Select (BA), if BA0, BA1 = 0,0 then bank A is selected; if BA0, BA1 = 1,0 then bank B is selected; if BA0, BA1 = 0,1 then bank C is selected; if BA0, BA1 = 1,1 then bank D is selected, respectively.
3) During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS latency.
4) During normal access mode, CKE is held high and CLK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5) The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6) All banks must be precharged before entering the Power Down Mode. The Power Down Mode does not preform any Refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.

CLOCK ENABLE (CKE0) TRUTH TABLE

CURRENT STATE	CKE		COMMAND						ACTION	NOTES
	PREVIOUS CYCLE	CURRENT CYCLE	CE	RAS	CAS	WE	BA	A12-A0		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
	L	H	L	X	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	CBR Refresh	
	H	H	L	L	L	L	OP Code		Mode Register Set	4
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	OP Code		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4
Any State Other Than Listed Above	H	H	X	X	X	X	X	X	Refer to operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

NOTES:

1) For the given Current State CKE must be low in the previous cycle.

2) When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CKS}) must be satisfied before any command other than Exit is issued.

3) The address inputs (A12-A0) depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.

4) The Power Down Mode, Self Refresh Mode, and the Mode Register Set can only be entered from the all banks idle state.

5) Must be a legal command as defined in the Current State Truth Table.

CURRENT STATE TRUTH TABLE

CURRENT STATE	COMMAND							ACTION	NOTES
	CE	RAS	CAS	WE	BA	A12, A11 A10/AP-A0	Description		
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	1
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	2
	L	L	H	L	X	X	Precharge	No Operation	2
	L	L	H	H	BA	Row Address	Bank Activate	Activate the specified bank and row	2
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	2
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	1
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	2
Row Active	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	2
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Precharge	3
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	3
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	3
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	
	L	H	H	L	X	X	Burst Termination	No Operation	4
	L	H	H	H	X	X	No Operation	No Operation	3
	H	X	X	X	X	X	Device Deselect	No Operation	3
Read	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	3
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	4
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	Power Down	4
	L	H	L	L	BA	Column	Write	Terminate Burst; Start the Write Cycle	
	L	H	L	H	BA	Column	Read	Terminate Burst; Start a new Read Cycle	5
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

CURRENT STATE TRUTH TABLE (Continued)

CURRENT STATE	COMMAND							ACTION	NOTES
	CE	RAS	CAS	WE	BA	A12, A11 A10/AP-A0	Description		
Write	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Terminat Burst; Start a new Write Cycle	8, 9
	L	H	L	H	BA	Column	Read	Terminate Burst; Start the Read Cycle	8, 9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

CURRENT STATE TRUTH TABLE (Continued)

CURRENT STATE	COMMAND							ACTION	NOTES
	CE	RAS	CAS	WE	BA	A12, A11 A10/AP-A0	Description		
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	No Operation; Bank(s) idle after t_{RP}	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	4
	L	H	L	H	BA	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RP}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RP}	
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4, 10
	L	H	L	L	BA	Column	Write	ILLEGAL	4
	L	H	L	H	BA	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RCD}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RCD}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RCD}	
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	9
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	9
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{DPL}	

CURRENT STATE TRUTH TABLE (Continued)

CURRENT STATE	COMMAND							ACTION	NOTES
	CE	RAS	CAS	WE	BA	A12, A11 A10/AP-A0	Description		
Write Recovering with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	4, 9
	L	H	L	H	BA	Column	Read	ILLEGAL	4, 9
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{DPL}	
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RC}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RC}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RC}	
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

NOTES ON FOLLOWING PAGE.

NOTES:

1) CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the command is being applied to.

2) All Banks must be idle otherwise it is an illegal action.

3) If CKE is active (high) the SDRAM starts the Auto (CBR) Refresh operation, if CKE is inactive (low) then the Self Refresh mode is entered.

4) The Current State refers only to one of the banks, if BA0, BA1 selects this bank then the action is illegal. If BA0, BA1 selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.

5) If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a No Operation.

6) The minimum and maximum Active time (t_{RAS}) must be satisfied.

7) The RAS to CAS Delay (t_{RCD}) must occur before the command is given.

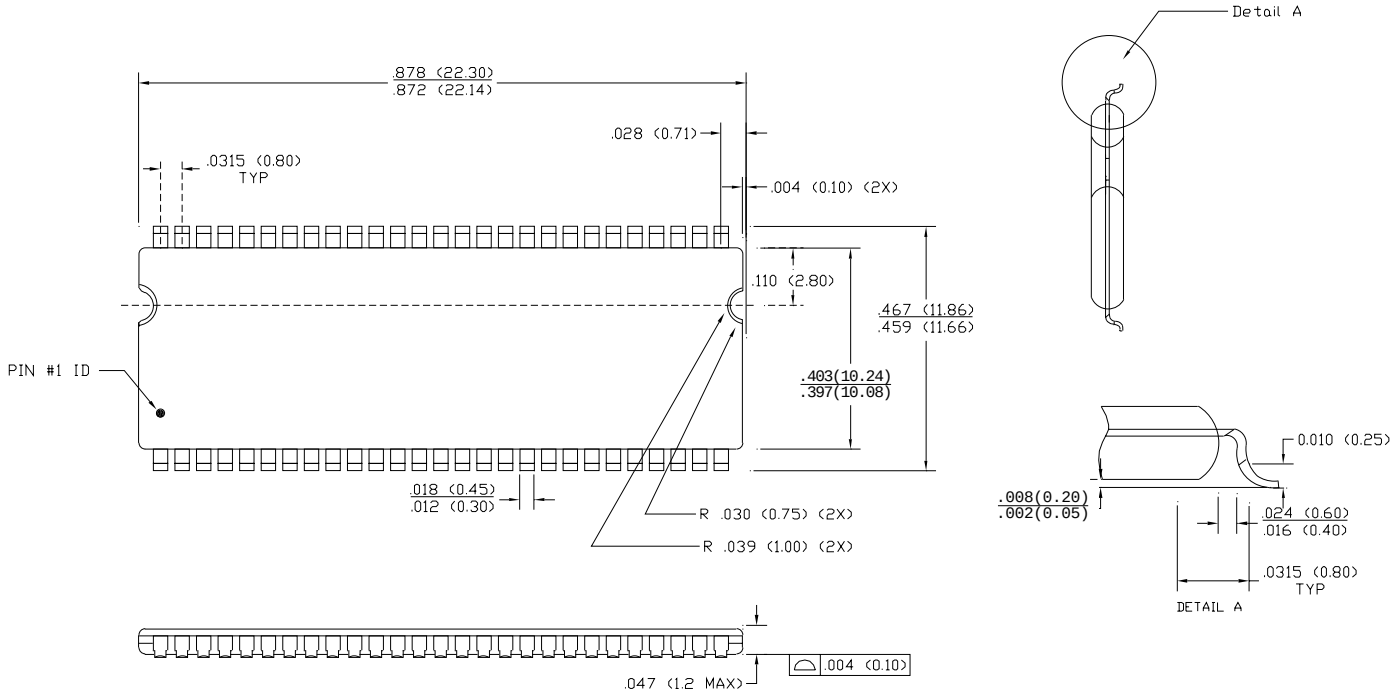
8) Address A10 is used to determine if the Auto Precharge function is activated.

9) The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.

10) The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

MECHANICAL DEFINITIONS*

ASI Case #901 (Package Designator DG)



All measurements are in inches (millimeters), MAX unless noted otherwise. Package width and length do not include mold protrusion (0.25mm allowable per side). MIN

ORDERING INFORMATION

EXAMPLE: AS4SD8M16DG-12/IT

Device Number	Package Type	Speed ns	Process
AS4SD8M16	DG	- 12	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C