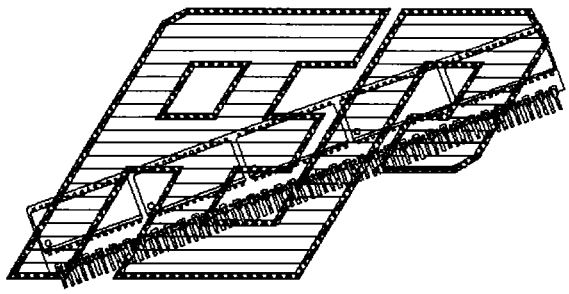
- >> ***8192 by 40 bit CREG/CRAM***
- >> ***General purpose pipeline register combined with a serial scan register and fast static RAM***
- >> ***Commonly used as a Writable Control Store***
- >> ***Word width expandable using multiple modules***
- >> ***Compact ZIP I/O lead format***
- >> ***TTL compatible I/Os***
- >> ***Uses single +5V power supply***



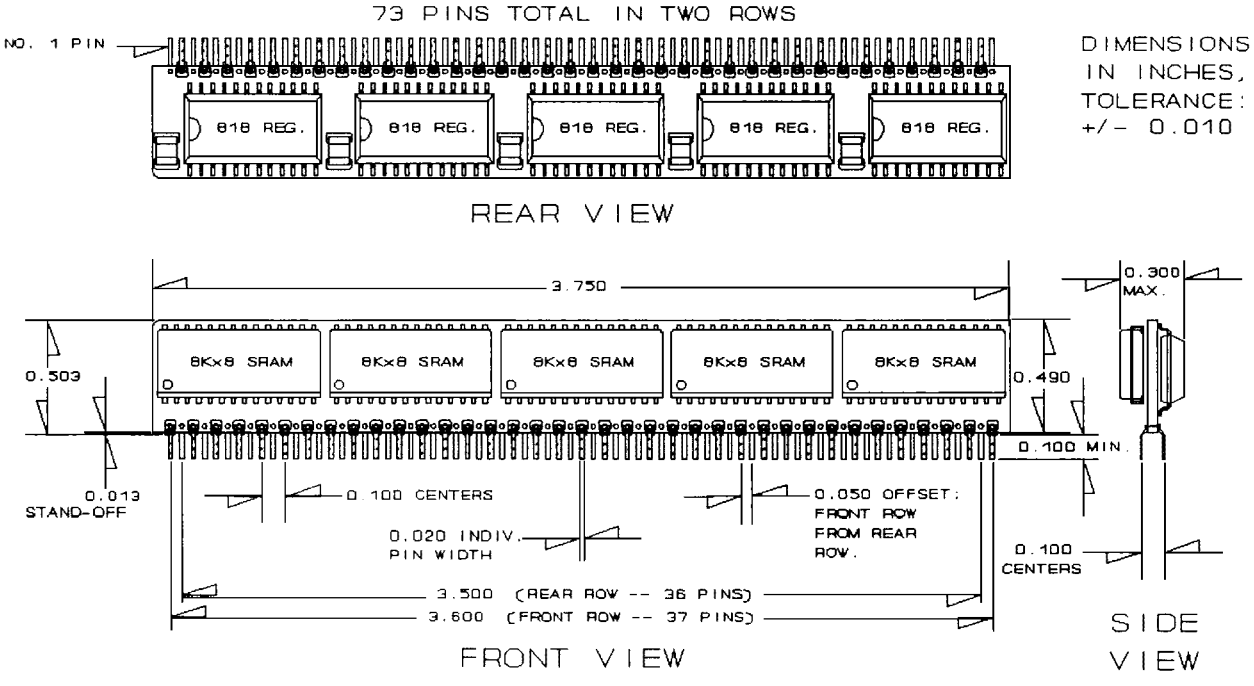
8192 BY 40 BIT HIGH SPEED CREG/CRAM MODULE

DESCRIPTION:

The AEPSZ8K40/818 is an 8 kilobytes by 40 bit wide Control Register/Control RAM (CREG/CRAM) module. It's purpose is to combine Writable Control Store (WCS) static RAM and a pipeline register in space-savings module form. Physically it consists of five high speed 8K x 8 static RAM ICs, five 818-type serial scan register ICs, and five 0.18 microfarad decoupling capacitors surface mounted on an FR4 PC material substrate. I/O is provided through 73 pins in a ZIP format.

The devices are organized with the 40 I/Os of the RAM connected to the D input/output ports of the 818s. The 40 Y output ports of the 818s are brought out individually to form the general purpose parallel pipeline register. The serial data-in and serial data-out pins of the 818s are chained to form the 40 bit serial data shadow register, creating one serial input and one serial output for the module as a whole. The register mode control input, the serial shift clock (DCLK), the parallel data clock (PCLK), and the register output enable input are connected in common to all 818 ICs. Similarly, the address lines and memory control inputs are bus organized across all memory devices on board.

SPECIFICATION DRAWING



8Kx40 LINE CREG/CRAM MODULE

PIN CONFIGURATION (TOP VIEW)

PIN #s

SDI -- 1	2 --WE_M*
OE_M* -- 3	4 -- A_0
Y_0 -- 5	6 -- Y_1
Y_2 -- 7	8 -- Y_3
Y_4 -- 9	10 -- Y_5
Y_6 -- 11	12 -- Y_7
A_1 -- 13	14 -- A_2
A_3 -- 15	16 -- A_4
A_5 -- 17	18 -- A_6
A_7 -- 19	20 -- Y_8
Y_9 -- 21	22 -- Y_{10}
Y_{11} -- 23	24 -- Y_{12}
Y_{13} -- 25	26 -- Y_{14}
Y_{15} -- 27	28 -- A_8
GND -- 29	30 -- VCC
GND -- 31	32 -- VCC
GND -- 33	34 -- A_9
Y_{16} -- 35	36 -- Y_{17}
Y_{18} -- 37	38 -- Y_{19}
Y_{20} -- 39	40 -- Y_{21}
Y_{22} -- 41	42 -- Y_{23}
A_{10} -- 43	44 -- VCC
GND -- 45	46 -- VCC
GND -- 47	48 --MODE
A_{11} -- 49	50 -- Y_{24}
Y_{25} -- 51	52 -- Y_{26}
Y_{27} -- 53	54 -- Y_{28}
Y_{29} -- 55	56 -- Y_{30}
Y_{31} -- 57	58 -- NC
PCLK -- 59	60 -- DCLK
OE_R* -- 61	62 -- CS_{2M}
CS_{1M}* -- 63	64 -- A_{12}
Y_{32} -- 65	66 -- Y_{33}
Y_{34} -- 67	68 -- Y_{35}
Y_{36} -- 69	70 -- Y_{37}
Y_{38} -- 71	72 -- Y_{39}
SDO -- 73	

*ACTIVE WHEN LOW

FUNCTIONAL DIAGRAM