# Dual Output 150/300 mA Low Dropout Regulator

## FEATURES

- 2.25 V to 5.5 V Input Voltage Range
- Two Outputs – 150 mA and 300 mA
- Low Ground Current of 48 μA
- Open Drain Driver Output Sinking 150 mA
- Low Dropout Voltage of 65 mV at 100 mA
- ERR
- Current Limit
- Thermal Shutdown
- MLP33-10 PowerPAK® Package (Fixed Output)
- MLP44-16 PowerPAK® Package (Adjustable Output)
- MIC2210 Pin-for-Pin Replacement

Pb-free

## APPLICATIONS

- Cellular Phones
- Wireless Modems
- PDAs

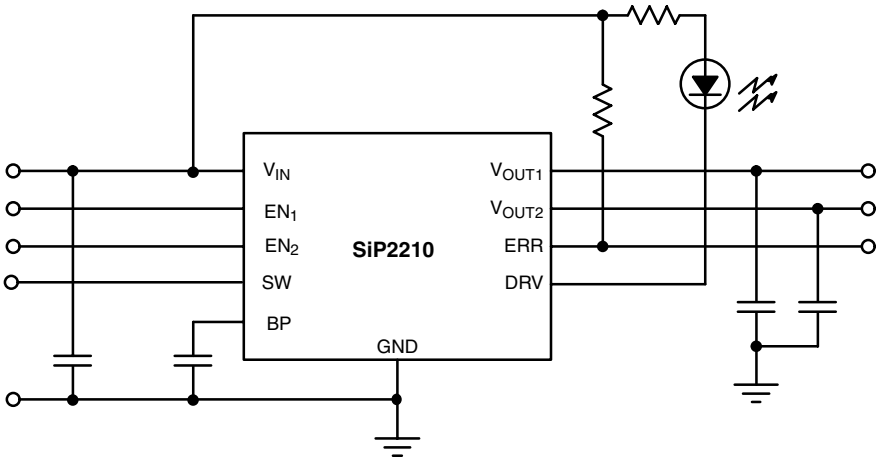
## DESCRIPTION

SiP2210 is a dual output low dropout regulator capable of supplying 150 mA from output 1 and 300 mA from output 2. The SiP2210 has the outputs independently enabled. In addition to the LDOs, an open drain output has been included, which is capable of sinking 150 mA. SiP2210 offers a low dropout, low ground current and extremely low noise with the addition of a bypass capacitor.

Protection features include ERR, undervoltage lockout, output current limit, and thermal shutdown.

The fixed output version of SiP2210 is available in a lead (Pb)-free MLP33-10 PowerPAK package and the adjustable version is available in a lead (Pb)-free MLP44-16 PowerPAK package. Both packages ares specified to operate over the range of –40 °C to 85 °C.

## TYPICAL APPLICATION CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

$V_{IN}$, $V_{EN}$, to GND . . . . . –0.3V to 7 V
Power Dissipation
MLP33-10 PowerPAK[b] . . . . . 1600 mW
MLP44-16 PowerPAK[c] . . . . . 1880 mW
Storage Temperature . . . . . –55 to 150 °C
Thermal Resistance (MLP10 PowerPAK) . . . . . 50 °C/W

Notes:
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 20 mW/°C above 70 °C.
c. Derate 23.5 mW/°C above 70 °C.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING RANGE

Input Voltage Range . . . . . 2.25 to 5.5 V
Enable Voltage Range . . . . . 0 V to 5.5 V
Operating Temperature Range $T_A$ . . . . . –40 to 85 °C
Operating Temperature Range $T_J$ . . . . . –40 to 125 °C

## SPECIFICATIONS

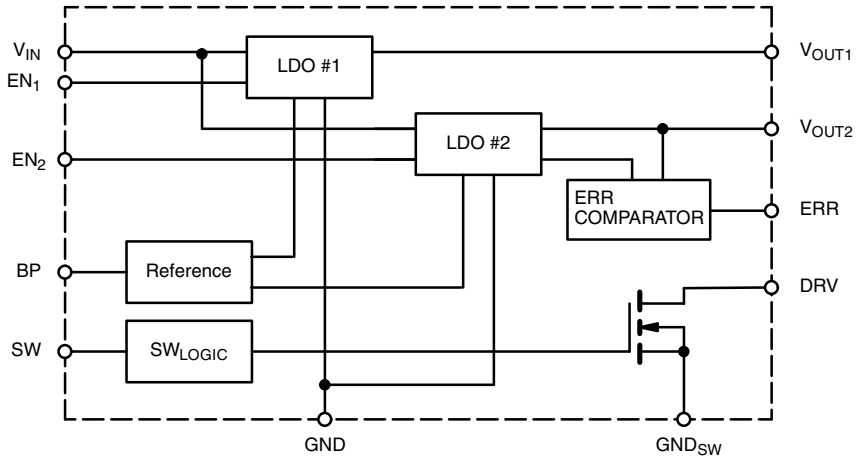
| Parameter | Symbol | Test Conditions Unless Specified<br>$V_{IN} = V_{OUT} + 1$ V[e], $C_{OUT} = 1$ µF, $I_{OUT} = 100$ µA, $T_A = 25$ °C | Temp[a] | Limits Min[b] | Limits Typ[c] | Limits Max[b] | Unit |
|---|---|---|---|---|---|---|---|
| **Regulators** | | | | | | | |
| Output Voltage Accuracy | | From Nominal $V_{OUT}$ | Room | –1 | | 1 | % |
| | | | Full | –2 | | 2 | |
| Output Voltage Temperature Coefficient | | | Room | | 40 | | ppm/°C |
| Line Regulation[e] | | $V_{IN} = V_{OUT} + 1$ V to 5.5 V | Room | –0.3 | 0.2 | 0.3 | % |
| | | | Full | –0.6 | | 0.6 | |
| Load Regulation | | $I_{OUT}$ = 100 µA to 150 mA (LDO 1 and 2) | Room | | 0.2 | 1.0 | |
| | | $I_{OUT}$ = 100 µA to 300 mA (LDO 2) | Room | | | 1.5 | |
| Dropout Voltage[f] | $V_{DROP}$ | $I_{OUT}$ = 150 mA (LDO 1 and 2) | Room | | 120 | 190 | mV |
| | | | Full | | | 250 | |
| | | $I_{OUT}$ = 300 mA (LDO 2) | Room | | 240 | 340 | |
| | | | Full | | | 420 | |
| Ground Pin Current | $I_G$ | $I_{OUT1} = I_{OUT2} = 0$ µA | Room | | 48 | 65 | µA |
| | | $I_{OUT1} = I_{OUT2} = 0$ µA | Full | | | 80 | |
| | | $I_{OUT1}$ = 150 mA, $I_{OUT2}$ = 300 mA | Room | | 60 | | |
| | | $V_{EN} < 0.4$ V | Full | | | 2.0 | |
| Sequence Time Delay[d] | $t_{SEQ}$ | | Room | | 70 | | µs |
| Output Voltage Noise | | $C_{BP}$ = 0.01 µF | | | 30 | | µVrms |
| Ripple Rejection | | f = 1 kHz, $C_{OUT} = 1$ µF, $C_{BP}$ = 10 nF | Room | | 60 | | dB |
| | | f = 20 kHz, $C_{OUT} = 1$ µF, $C_{BP}$ = 10 nF | Room | | 40 | | |
| **Inputs** | | | | | | | |
| EN, SW Input Voltage | $V_{IL}$ | Logic Low | Full | | | 0.6 | V |
| | $V_{IH}$ | Logic High | Full | 1.8 | | | |
| EN, SW Input Current | $I_{IL}$ | $V_{IL} < 0.6$ V | Room | –1 | 0.01 | 1 | µA |
| | $I_{IH}$ | $V_{IH} > 1.8$ V | Room | –1 | 0.01 | 1 | |
| SET Pin Threshold Voltage | $V_{TH}$(set) | POR = High | Room | | 1.25 | | V |
| SET Pin Current Source | | $V_{SET} = 0$ V | Room | 0.75 | 1.25 | 1.75 | µA |

## SPECIFICATIONS

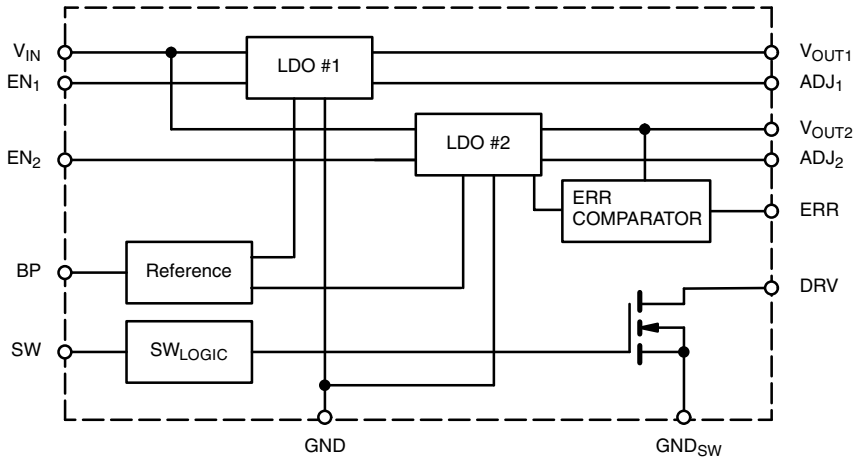
| Parameter | Symbol | Test Conditions Unless Specified<br>$V_{IN} = V_{OUT} + 1$ V[e], $C_{OUT} = 1$ µF, $I_{OUT} = 100$ µA, $T_A = 25$ °C | Temp[a] | Limits Min[b] | Limits Typ[c] | Limits Max[b] | Unit |
|---|---|---|---|---|---|---|---|
| **Error Flag Output (ERR)** | | | | | | | |
| Threshold | $V_{THL}$ | % of Nominal $V_{OUT2}$ | Room | 90 | | | % |
| | $V_{THH}$ | | Room | | | 96 | |
| Output Voltage | $V_{OL}$ | $I_L = 250$ µA | Room | | 0.02 | 0.1 | V |
| Leakage Current | $I_{ERR}$ | ERR = High | Room | –1 | 0.01 | 1 | µA |
| **Driver (DRV) Output** | | | | | | | |
| Output Voltage | $V_{OL}$ | $I_L = 150$ mA | Full | | 0.2 | 0.6 | V |
| Leakage Current | | $I_{DRV} = 0$ mA, $V_{DRV} = 5.5$ V, SW = 0 V | Room | –1 | 0.01 | 1 | µA |
| **Protection** | | | | | | | |
| Current Limit | $I_{IL}$ | $V_{OUT1} = 0$ V | Room | 150 | 280 | 460 | mA |
| | | $V_{OUT2} = 0$ V | Room | 300 | 450 | 700 | |
| Thermal Shutdown Temperature | | | Room | | 165 | | °C |
| Thermal Hysteresis | | | Room | | 25 | | |

Notes
a. Room = 25 °C, Full = –40 to 85 °C.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Timing is measured from 90 % of LDO #1's final value to 90 % of LDO #2's final value.
e. For higher output of the regulator pair.
f. Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2 % below the output voltage measured with a 1-V differential, provided that $V_{IN}$ does not drop below 2.25 V. When $V_{OUT(nom)}$ is less than 2.25 V, the output will be in regulation when 2.25 V – $V_{OUT(nom)}$ is greater than the dropout voltage specified.

## FUNCTIONAL BLOCK DIAGRAM



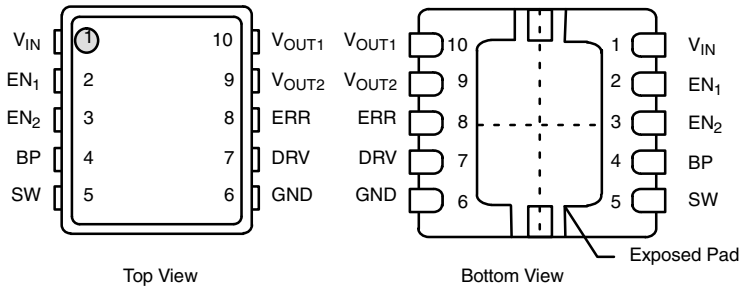

Fixed Voltage Version



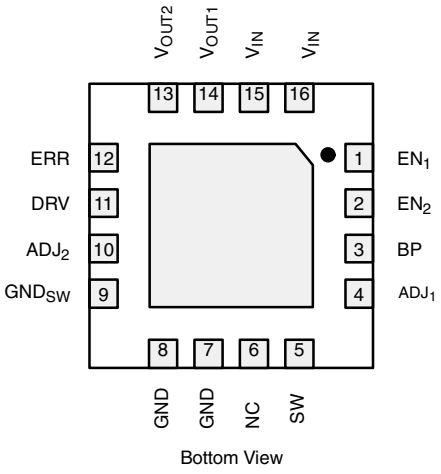

Adjustable Voltage Version

## PIN CONFIGURATIONS AND ORDERING INFORMATION

**PowerPAK MLP33–10 with Large Pad**




**PowerPAK MLP44–16**




| VOLTAGE OPTIONS | |
|---|---|
| **Voltage** | **Code (x,z)** |
| Adj | A |
| 1.5 | F |
| 1.6 | W |
| 1.8 | G |
| 1.85 | D |
| 1.9 | Y |
| 2.0 | H |
| 2.1 | E |
| 2.5 | J |
| 2.6 | K |
| 2.7 | L |
| 2.8 | M |
| 2.85 | N |
| 2.9 | O |
| 3.0 | P |
| 3.1 | Q |
| 3.2 | R |
| 3.3 | S |
| 3.4 | T |
| 3.5 | U |
| 3.6 | V |

| ORDERING INFORMATION | | | |
|---|---|---|---|
| **Part Number** | **Temp Range** | **Package** | **Marking** |
| SiP2210DMP-XZ-E3 | –40 to 85 °C | PowerPAK MLP33-10 | 10XZ |
| SiP2210DLP-AA-E3 | | PowerPAK MLP44-16 | 10AA |

X: Output 1 voltage code
Z: Output 2 voltage code

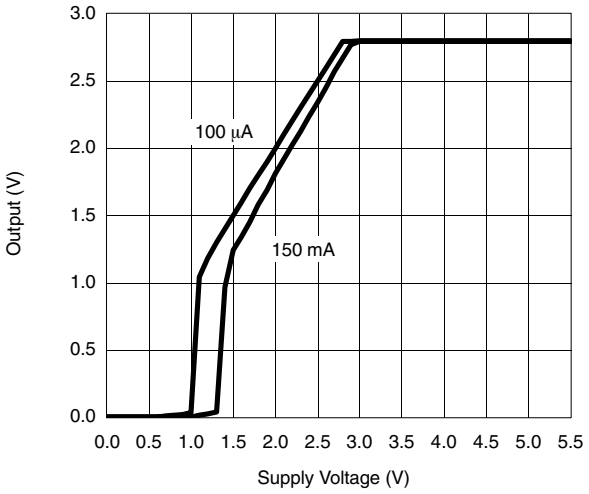
## PIN DESCRIPTION

| Pin Number | | | |
|---|---|---|---|
| **MLP33-10** | **MLP44-16** | **Name** | **Function** |
| 1 | 15, 16 | $V_{IN}$ | Input voltage for the power MOSFETs and their gate drive |
| 2 | 1 | $EN_1$ | Enables LDO #1 output. |
| | 6 | NC | No Connect |
| 3 | 2 | $EN_2$ | Enables LDO #2 output. |
| 4 | 3 | BP | Bypass for noise reduction |
| | 4 | $ADJ_1$ | Feedback connection for LDO #1 |
| 5 | 5 | SW | Control for open drain output |
| 6 | 7, 8 | GND | Ground |
| | 9 | $GND_{SW}$ | Ground for the internal n-channel MOSFET switch |
| | 10 | $ADJ_2$ | Feedback connection for LDO #2 |
| 7 | 11 | DRV | Open drain output |
| 8 | 12 | ERR | ERROR Flag Output |
| 9 | 13 | $V_{OUT2}$ | Output of LDO #2 – 300 mA |
| 10 | 14 | $V_{OUT1}$ | Output of LDO #1 – 150 mA |

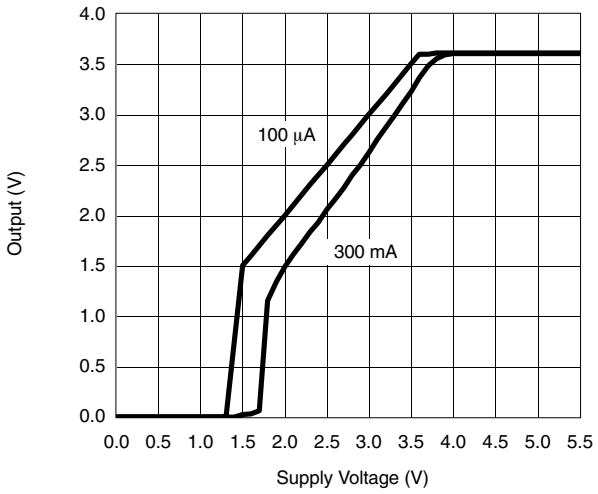
The exposed pad on both packages must be connected externally to the GND pin.

## TYPICAL CHARACTERISTICS

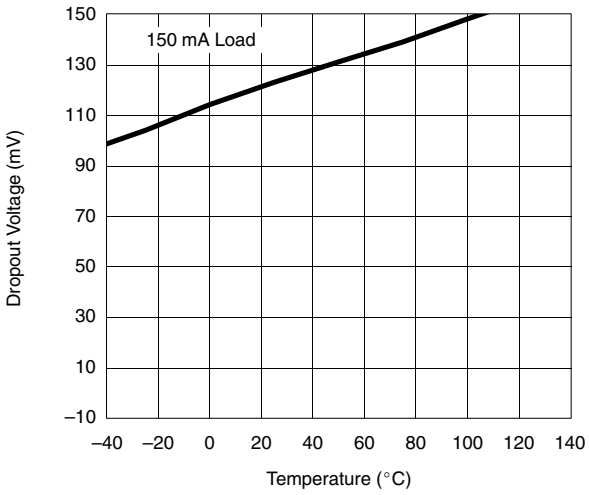
**Dropout Characteristics—Output 1**



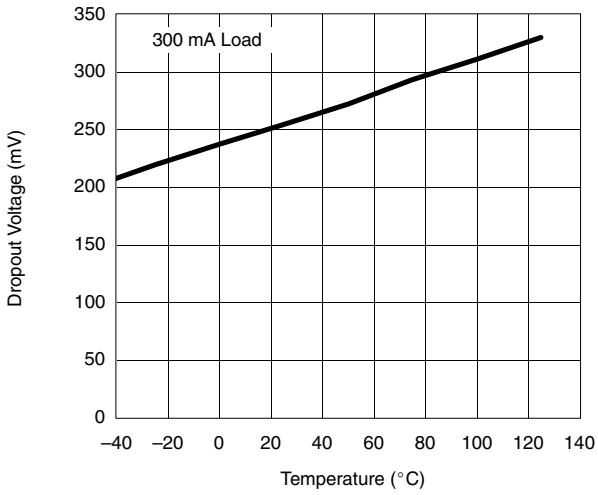

**Dropout Characteristics—Output 2**



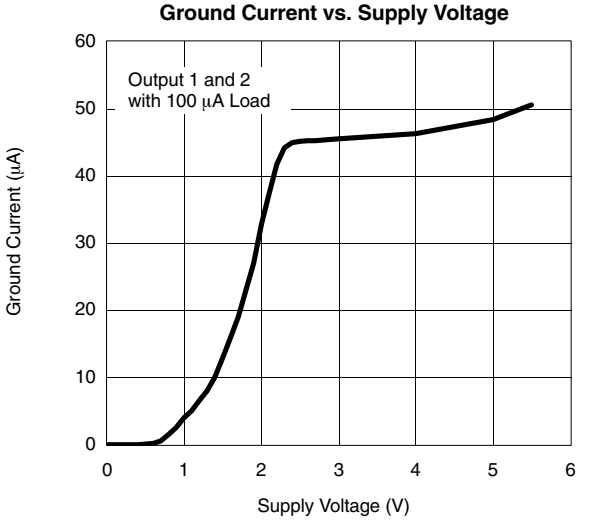

**Dropout Voltage—Output 1**



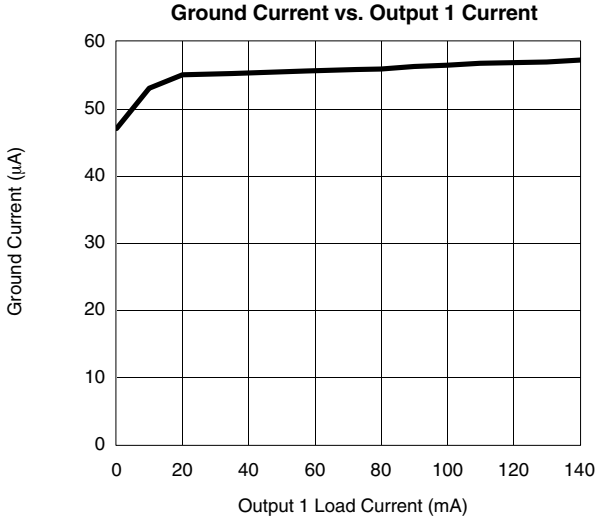

**Dropout Voltage—Output 2**




**Ground Current vs. Supply Voltage**

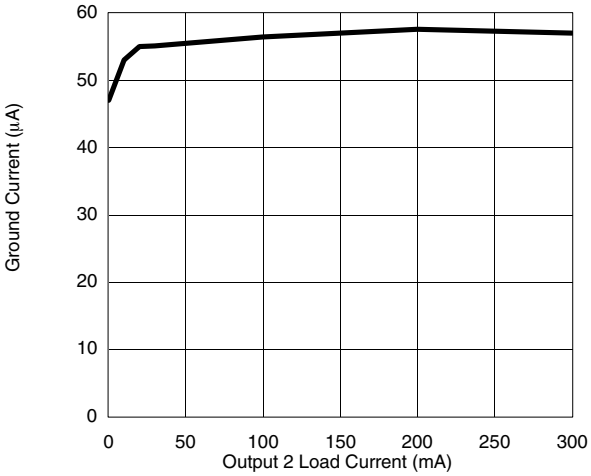



**Ground Current vs. Output 1 Current**

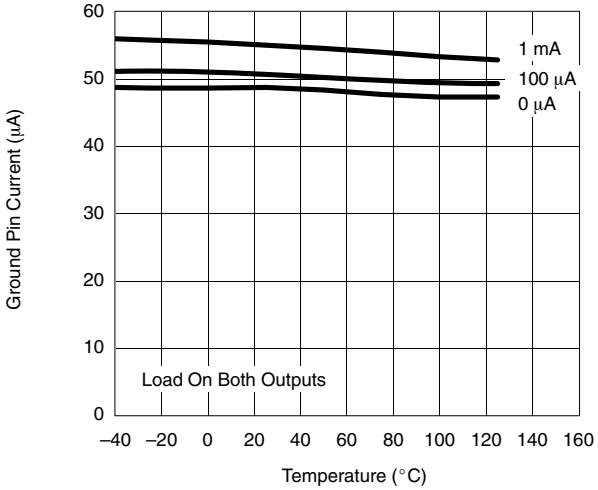


## TYPICAL CHARACTERISTICS

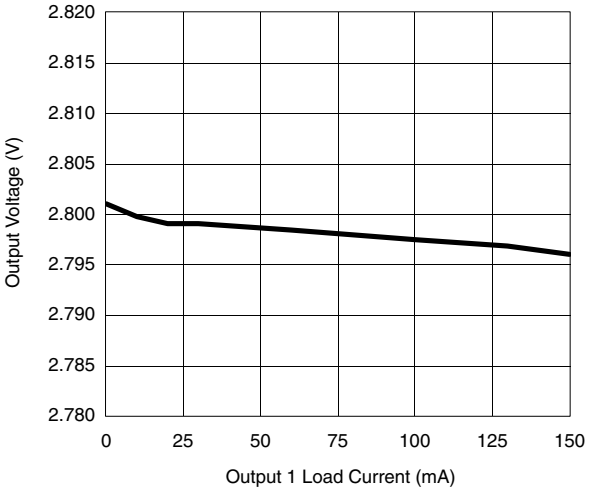
**Ground Current vs. Output 2 Current**



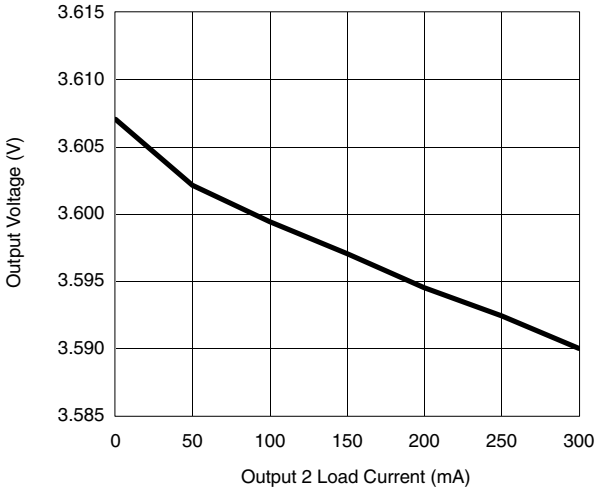

**Ground Pin Current**



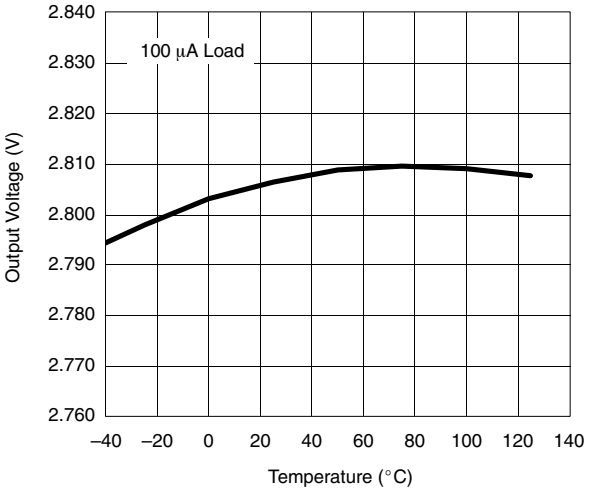

**Output Voltage vs. Load Current—Output 1**



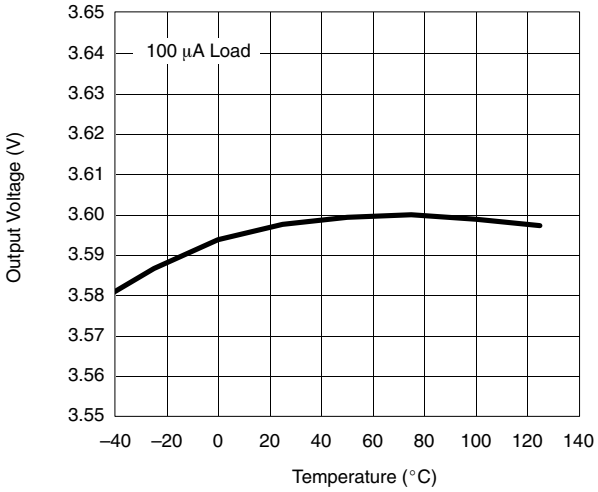

**Output Voltage vs. Load Current—Output 2**




**Output Voltage 1 vs. Temperature**

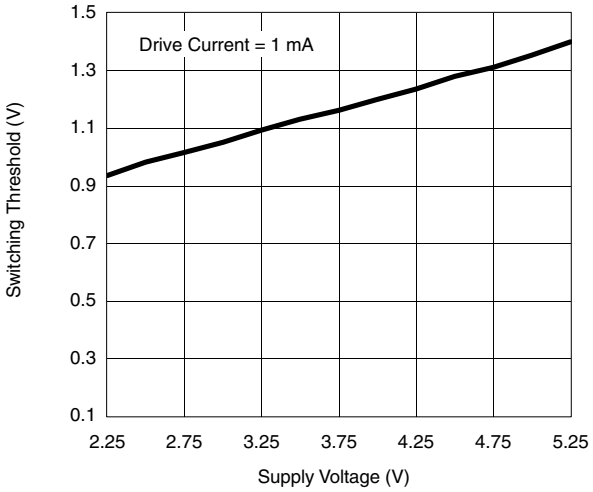



**Output Voltage 2 vs. Temperature**

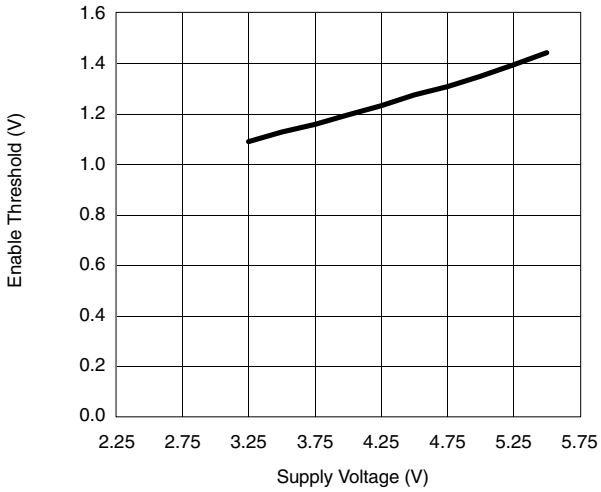


## TYPICAL CHARACTERISTICS

**Switch Threshold vs. Supply Voltage**

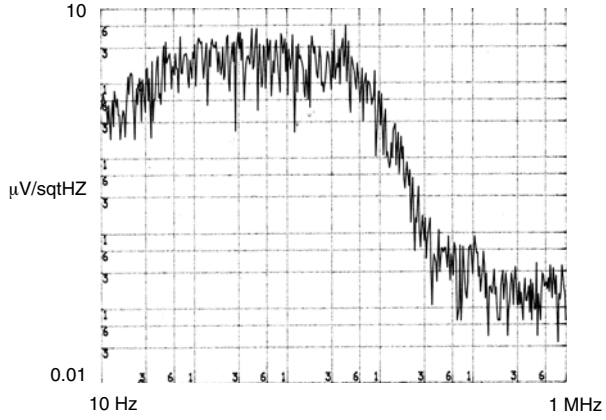



**Enable Voltage Threshold vs. Supply Voltage**

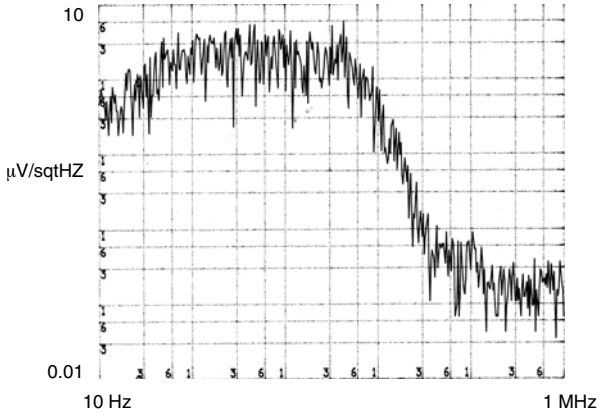


## TYPICAL WAVEFORMS

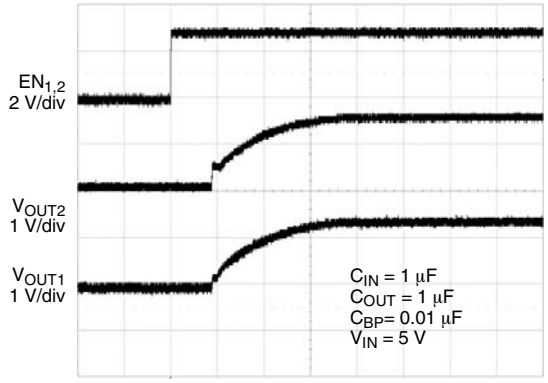
**Noise Spectrum Output 1**



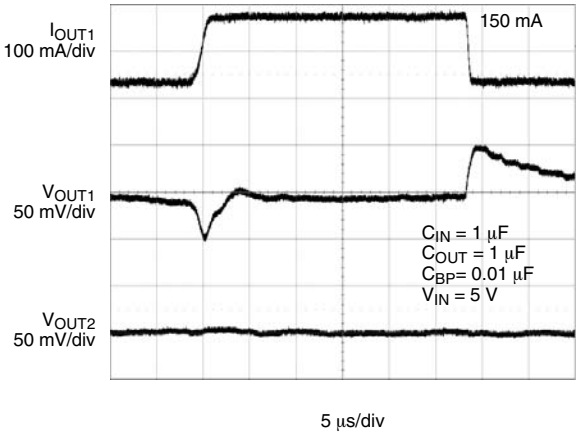

**Noise Spectrum Output 2**



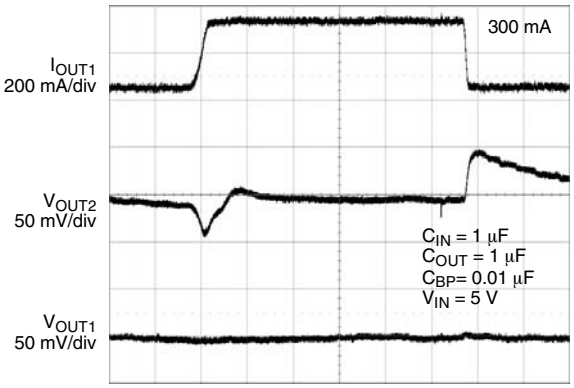

**Enable Sequence**




**Load Transient Response LDO 1**




**Load Transient Response LDO2**



## DETAILED OPERATION

The SiP2210 is a low dropout, low quiescent current monolithic dual linear regulator, with power-on reset and open drain driver output features. With output voltage range from 1.25 V to 5 V, the first regulator can source 150 mA and the second regulator can source 300 mA. The open drain driver has the capability to drive LED's for backlighting applications.

### $V_{IN}$

$V_{IN}$ is the input supply pin for both LDO's. The bypass capacitor for this pin is not critical as long as the input supply has low enough source impedance. For practical circuits, a 1.0-µF or larger ceramic capacitor is recommended. When the source impedance is not low enough and/or the source is several inches from the SiP2210, then a larger input bypass capacitor is needed. When the source impedance, wire and trace impedance are unknown, it is recommended that an input bypass capacitor be used of a value that is equal to or greater than the output capacitor.

### $V_{OUT1,2}$ (LDO Outputs)

The $V_{OUT}$ is the output voltage of the regulator. Connect a bypass capacitor from $V_{OUTx}$ to ground. The output capacitor can be any value from 1.0 µF to 10.0 µF. A ceramic capacitor with X5R or X7R dielectric type is recommended for best output noise, line transient, and load transient performance.

### Enable

The EN1 and EN2 pins control the turning on and off of their respective regulators in the SiP2210. $V_{OUT}$ of both outputs are guaranteed to be on when the Enable pin voltage is equal or greater than 1.8 V. $V_{OUT}$ is guaranteed to be off when the Enable pin voltage equals or is less than 0.6 V. To automatically turn on $V_{OUT}$ whenever the input is applied, tie the Enable pin to $V_{IN}$.

### ERROR Flag Output (ERR)

The ERR is an open drain output that goes low when $V_{OUT2}$ is less than 5 % of its nominal value. As with any open drain output, an external pull up resistor is needed. The ERR pin is disconnected if not used.

### OPEN-Drain Driver (DRV)

The SW pin a logic level input put that controls the DRV pin. The switch pin is an active high input and should not be left floating. The drive pin is an open drain output able to sink 150 mA of current.

### Bypass Capacitor

For low noise application and/or increase in power supply rejection ration (PSRR) connect a high frequency ceramic capacitor from BP to ground. A 0.01-µF X5R or X7R ceramic capacitor is recommended.

# Disclaimer

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